

PATENT SPECIFICATION

DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Angle Modulated Wave Demodulating Circuits

We, RADIO CORPORATION OF AMERICA, a Corporation organized under the laws of the State of Delaware, United States of America, of 30, Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to angle modulated wave demodulating circuits. More particularly, it relates to frequency modulation detector circuits which may be fabricated using integrated circuit techniques.

As used herein, the term "integrated circuit" refers to a unitary or monolithic semiconductor device or chip which is the equivalent of a network of interconnected active and passive circuit elements. At the present state of the art there is no satisfactory way of providing an inductor on an integrated circuit. In addition, capacitors require a large area of the integrated circuit chip even to provide a very small capacitance; and due to limitations of present fabrication techniques, capacitors may represent a potential source of trouble due to the incidence of shorting of the capacitor plates.

In considering the application of integrated circuit techniques to frequency discriminator circuits, it is apparent that the tuned phase-shift discriminator transformer will not be incorporated on the integrated circuit chip. In addition, the remainder of known discriminator circuits are not readily susceptible to fabrication using integrated circuit techniques. The reason for this is that known discriminator circuits employ peak rectification of applied signal voltages, and discriminator load networks having time constants greater than the period of the wave

to be demodulated are required for this type of operation. The values of the resistors and capacitors needed to obtain such time constants in these load networks would be too large for economical incorporation on the integrated circuit chip.

It is an object of the present invention, therefore to provide a frequency modulated detector circuit which may be fabricated using integrated circuit techniques.

As will become clear hereinafter such fabrication is made possible by constructing the circuit so that only a relatively small amount of capacitance is then required to filter the frequency modulated signal. This eliminates the necessity for the large capacitors conventionally used to obtain peak rectification. In the circuits disclosed the filtering capacitance for the signal frequency and its harmonics is provided by solely the distributed capacitance of resistors which may be integrated resistors.

In accordance with the invention an angle modulated wave demodulating system is discussed which includes a frequency discriminator transformer with a secondary winding a pair of rectifiers coupled to said winding, load resistance coupled to said rectifiers to form a series connected circuit therewith and with at least a portion of said secondary winding, and characterized in that the load network for said rectifier comprises said load resistance and principally the distributed capacity across said resistance.

In accordance with an embodiment of the invention an integrated form of frequency modulation detector or discriminator circuit is described which includes a tuned phase-shift discriminator transformer which is external to the integrated circuit chip. The discriminator transformer is connected to drive a first pair of rectifier devices formed on the

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integrated circuit chip. A pair of integrated load resistors also on the integrated circuit chip are coupled to the pair of rectifier devices to form a series circuit therewith and with the secondary winding of the discriminator transformer. The load resistors and solely their distributed capacitance comprise the load network for the detector circuit, with the distributed capacitance providing filtering of the frequency modulated signal applied to the primary winding of the transformer and of its harmonics. The time constant of the load network is relatively short, and may be, for example, of the order of the period of the modulated carrier wave applied to the discriminator transformer.

The sole figure is a schematic circuit diagram of an angle modulated wave processing channel embodying the invention.

The integrated circuit of the invention will be described in the context of a television receiver. It is to be understood, however, that the fundamental concepts to be described are more generally applicable. For example, the circuit may be used in broadcast or communication receivers.

The schematic circuit diagram of Figure 1 shows an example of specific circuitry embodying the invention. The dashed rectangle 10 schematically illustrates a monolithic semiconductor circuit chip. The chip has a plurality of contact areas about the periphery thereof through which connections to the circuit on the chip may be made. For example, the chip 10 has a pair of contact areas 12 and 14 which are coupled to a source of FM waves. The contact area 14 provides a common or ground potential contact area which is connected to the various circuit-ground connections shown on the chip. As to physical dimensions, the chip 10 may be of the order of 50 mils $\times$ 50 mils, or smaller.

FM signals from a suitable source, such as a video detector or video amplifier of a television receiver, are applied to a terminal 16 and coupled through a capacitor 18 to a resonant circuit 20 which is tuned to the 4.5 Mcs intercarrier beat between the video and sound carriers of a television signal. The resonant circuit 20 and the coupling capacitor 18 in the present example are external to the chip, but are coupled thereto through the contact areas 12 and 14.

The contact areas 12 and 14 are coupled to a limiter amplifier 22 which is of a design susceptible to integrated circuit fabrication processes. The limiter amplifier stage 22 is connected to drive an emitter coupled amplifier-limiter stage 24 including a pair of transistors 26 and 28. The emitter electrodes of the transistors 26 and 28 are connected in common through a resistor 29 to ground. The collector electrode of the transistor 26 is connected to an operating potential supply contact area 30 which is adapted to be con-

nected to a positive terminal of an operating potential supply source, not shown.

The collector electrode of the transistor 28 is connected through a contact area 32 to the primary winding 34 of a tuned phase-shift discriminator transformer 36. The secondary winding 38 of the discriminator transformer 36 is connected between a pair of contact areas 48 and 42, and a tertiary winding 44 is connected between a centertap on the secondary winding 38 and an operating potential supply terminal 46.

The secondary winding 38 of the discriminator transformer is connected to drive a pair of oppositely poled rectifier devices 50 and 52. A pair of load resistors 54 and 56 are connected in series between the anode of the rectifier 50 and the cathode of the rectifier 52 to form a series circuit therewith and with the secondary winding 38 of the transformer 36. The discriminator circuit demodulates applied frequency modulated signals, with the demodulated signals appearing at the junction of the resistors 54 and 56. The demodulated signals are applied to, and provide the base current drive for a transistor 58 which has equal valued emitter and collector resistors 60 and 62 respectively. The transistor 58 is connected as an audio frequency amplifier, and push-pull output signals may be derived at the contact areas 64 and 66. If desired, single-ended audio signals may be derived at one or the other of the contact areas 64 and 66.

Before describing the operation of the FM demodulator circuit, it will be noted that the operating potential supply provides two different voltages for application to the contact areas 30 and 76. As indicated in the Figure, these voltages are plus 7 volts and plus 2 volts, respectively, each being measured with respect to ground. In addition, a reference potential point for the operation potential supply is connected to the grounded contact area 14. It is to be understood that a single operating potential supply contact area and a ground contact area may be connected to the chip, and the various voltages may be derived from a suitable tapped resistive or rectifier voltage divider formed on the chip.

In the operation of the circuit, amplitude limited frequency modulated waves are applied between the base electrode of the transistor 26 and ground. The emitter coupled amplifier 24 provides further limiting of the wave so that the output current in the collector circuit of the transistor 28 is essentially a square wave or a limited wave of substantially constant amplitude. The limited wave is applied through the tuned primary and secondary windings of the discriminator transformer 36 to the rectifiers 50 and 52. The load circuit for these two rectifiers comprises the resistors 54 and 56 and the distributed capacity of the load resistors 54 and 56 of the chip and capa-

city between the closely spaced leads of the chip. Accordingly, the distributed capacity of the load resistors 54 and 56 of the chip and the capacity between the closely spaced leads of the chip function as the required small filter capacity.

By returning the tertiary winding 44 of the discriminator transformer 36 to a positive voltage, for example, plus 2 volts with respect to ground at terminal 46, the input electrodes of the rectifiers 50 and 52 are also raised to this voltage. When a signal is applied, this voltage causes current to flow through the load resistors 54 and 56 so that the same plus 2 volts appears at the junction of resistors 54 and 56 at the center signal frequency. Thus, bias voltage is provided through the discriminator network for the output amplifier transistor 58 in a balanced fashion.

In the circuit shown, average detection is employed with a substantially resistive load. Filtering of the signal frequency and of its harmonics is provided by the distributed capacitances of the load resistors 54 and 56, and this filtering is further augmented by the capacitances between the leads of the chip.

The detection can be analyzed in terms of a switching action, wherein the junction of the resistors 54 and 56 is periodically connected to the tertiary signal voltage at the centertap of the transformer secondary winding 38.

If E_1 = peak value of the tertiary voltage;
 2Φ = angle during which the rectifiers 50 and 52 are conducting; and

θ = phase shift with frequency deviation from the center frequency (resonant frequency of the tuned circuit of winding 38)

Then the demodulated output voltage E_{AF} is given by

$$E_{AF} = \frac{1}{2\Phi} \int_{-\Phi}^{+\Phi} E_1 \sin(\omega t + \theta) d(\omega t)$$

$$= \frac{E_1}{2\Phi} [-\cos(\omega t + \theta)]_{-\Phi}^{+\Phi}$$

$$= E_1 \left(\frac{\sin \Phi}{\Phi} \right) \sin \theta$$

If the secondary voltage is large enough with respect to the rectifier "contact" potential to switch over 180 degrees,

$$\Phi = \frac{\pi}{2} \text{ and } \frac{\sin \Phi}{\Phi} = \frac{2}{\pi}, \text{ so that}$$

$$E_{AF} = \frac{2}{\pi} E_1 \sin \theta$$

Under these conditions the circuit has the advantage that the demodulated output E_{AF} is independent of the amplitude of the secondary voltage.

Where the secondary voltage is not large enough to overcome the rectifier "contact" potential, the switching angle is reduced and $\sin \Phi$

increases. Thus, the demodulated output also increases, as shown in the following table:

Switching Angle	Sin Φ	
	Φ	Φ
180°	π	0.64
	2	
90°	π	0.90
	4	
45°	π	0.98
	8	
0°	0	1.0

The effective sensitivity of the average or sampling detector described above is increased over that of the conventional peak detector variety by virtue of its reduced loading. For an average rectifier type of detector operating into a load R , the equivalent loading reflected to the driving source is determined as follows:

$$P = \frac{1}{2} \frac{E^2}{R} = \frac{E^2}{(2R)} \text{ where } E = \text{rms input signal}$$

$$\therefore \text{loading} = 2R$$

In the case of a peak rectifier type of detector working into a load R shunted with a capacitor C ,

$$P = \frac{(\sqrt{2} E)^2}{R} = \frac{E^2}{(R/2)}$$

$$\therefore \text{loading} = R/2$$

Accordingly, the loading on the discriminator transformer driving source in an average detector is reduced below that of a conventional peak detector by a factor of 4 to 1.

This reduced loading is an important advantage because it can be used to make the discriminator slope sensitivity and the peak-to-peak separation substantially independent of variations in the integrated load resistors. The latter tend to vary as much as $\pm 20\%$ in resistance value because of variations in the present process of making the diffused resistors used in monolithic integrated circuits. In the average detector of the figure, however, the loading reflected by the diffused resistors

is reduced to such a low level that it plays a negligible role in determining the discriminator characteristics. Thus, linearity and peak-to-peak separation can be maintained over the full range of resistance values. The decreased loading, in addition, makes possible higher efficiency, reduced power consumption, and greater immunity to impulse noise.

Desirable operating characteristics have been obtained in the chip circuit of the figure with the distributed capacity of the load resistors 54 and 56 and the capacity between the leads of the chip. The 0.1μ second time constant formed with the 10K resistors 54 and 56 is less than the 2μ second period of the applied signal. For a 4.5 Mc/s FM wave, the 0.1μ second time constant is of the order of the 0.2μ second signal. In the figure, this includes the input capacitance of the audio amplifier transistor 58.

This use of relatively short time constant discriminator load network provides several important advantages as applied to integrated circuits. First, the very small value of capacitance required (as compared with prior art discriminator circuits) reduces or eliminates the amount of area required for capacitors on the integrated circuit chip and makes it practical to integrate the discriminator load network. Second, the reduction in reflected loading makes it possible to obtain a uniformly linear discriminator characteristic of desired peak-to-peak separation despite large production variations in the values of the diffused load resistors. Third, the large pulses of current characteristic of peak rectifier discriminator circuits can be eliminated and the harmonic radio-frequency interference which they would otherwise cause in television and communications receivers can be suppressed.

The discriminator rectifiers 50 and 52 should be fabricated in a manner to provide a relatively small junction area to prevent unbalance of the discriminator. There is more capacitance from the cathodes of the various rectifiers to the integrated circuit chip substrate than from their anodes. Accordingly, there is effectively more capacitance-to-ground from the cathode of the rectifier 52 than from the anode of the rectifier 50. This inequality may be overcome by making the relative sizes of the junctions of the rectifiers such that the total mean capacitances from the anode of the rectifier 50 to ground; and from the cathode of the rectifier 52 to ground are of the same value. The same principle may be used to balance the load network capacitances of the discriminator circuit.

In the circuit shown, the plus 2 volt bias voltage is applied to the tertiary winding 44 and the demodulated output is taken off at the

junction of the two load resistors 54 and 56. Because of the series nature of the circuit, these two positions can be interchanged so that the bias voltage is applied at the junction of the two load resistors and the demodulated output is taken off at a point on the tertiary winding 44.

Although the circuit shown shows transformer 36 as having a separate tertiary winding 44, it will be readily apparent to one skilled in the art that this winding can be eliminated by connecting the "hot" side of the primary winding 34, or a tap thereon, directly to the centertap on the secondary winding 38. The positive voltage for the discriminator network is then obtained directly from the winding 34.

WHAT WE CLAIM IS:—

1. An angle modulated wave demodulating system having a frequency discriminator transformer with a secondary winding, a pair of rectifiers coupled to said winding, load resistance coupled to said rectifiers to form a series connected circuit therewith and with at least a portion of said secondary winding, and characterized in that the load network for said rectifier comprises said load resistance and principally the distributed capacity across said resistance.

2. An angle modulated wave demodulating system according to claim 1, characterized in that said pair of rectifiers and said load resistance are disposed in an integrated circuit.

3. An angle modulated wave demodulating system according to claim 1, characterized in that the time constant of said load resistance and distributed capacity is substantially no greater than the period of an applied angle modulated wave.

4. An integrated circuit useful in a discriminator circuit comprising a load resistance in series with a pair of rectifiers, said circuit also having contacts for series connection to a discriminator transformer, the load resistance and principally its distributive capacitance comprising the load network for the discriminator circuit.

5. An angle modulated wave demodulating system substantially as described and illustrated in the accompanying specification and drawings.

6. An integrated circuit useful in a discriminator circuit substantially as described and illustrated in the accompanying specification and drawings.

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Desirable operating characteristics have been obtained in the chip circuit of the figure with the distributed capacity of the load resistors 54 and 56 and the capacity between the leads of the chip. The 0.1μ second time constant formed with the 10K resistors 54 and 56 is less than the 2μ second period of the applied signal. For a 4.5 Mc/s FM wave, the 0.1μ second time constant is of the order of the 0.2μ second signal. In the figure, this includes the input capacitance of the audio amplifier transistor 58.

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2. An angle modulated wave demodulating system according to claim 1, characterized in that said pair of rectifiers and said load resistance are disposed in an integrated circuit.
3. An angle modulated wave demodulating system according to claim 1, characterized in that the time constant of said load resistance and distributed capacity is substantially no greater than the period of an applied angle modulated wave.
4. An integrated circuit useful in a discriminator circuit comprising a load resistance in series with a pair of rectifiers, said circuit also having contacts for series connection to a discriminator transformer, the load resistance and principally its distributive capacitance comprising the load network for the discriminator circuit.
5. An angle modulated wave demodulating system substantially as described and illustrated in the accompanying specification and drawings.
6. An integrated circuit useful in a discriminator circuit substantially as described and illustrated in the accompanying specification and drawings.

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