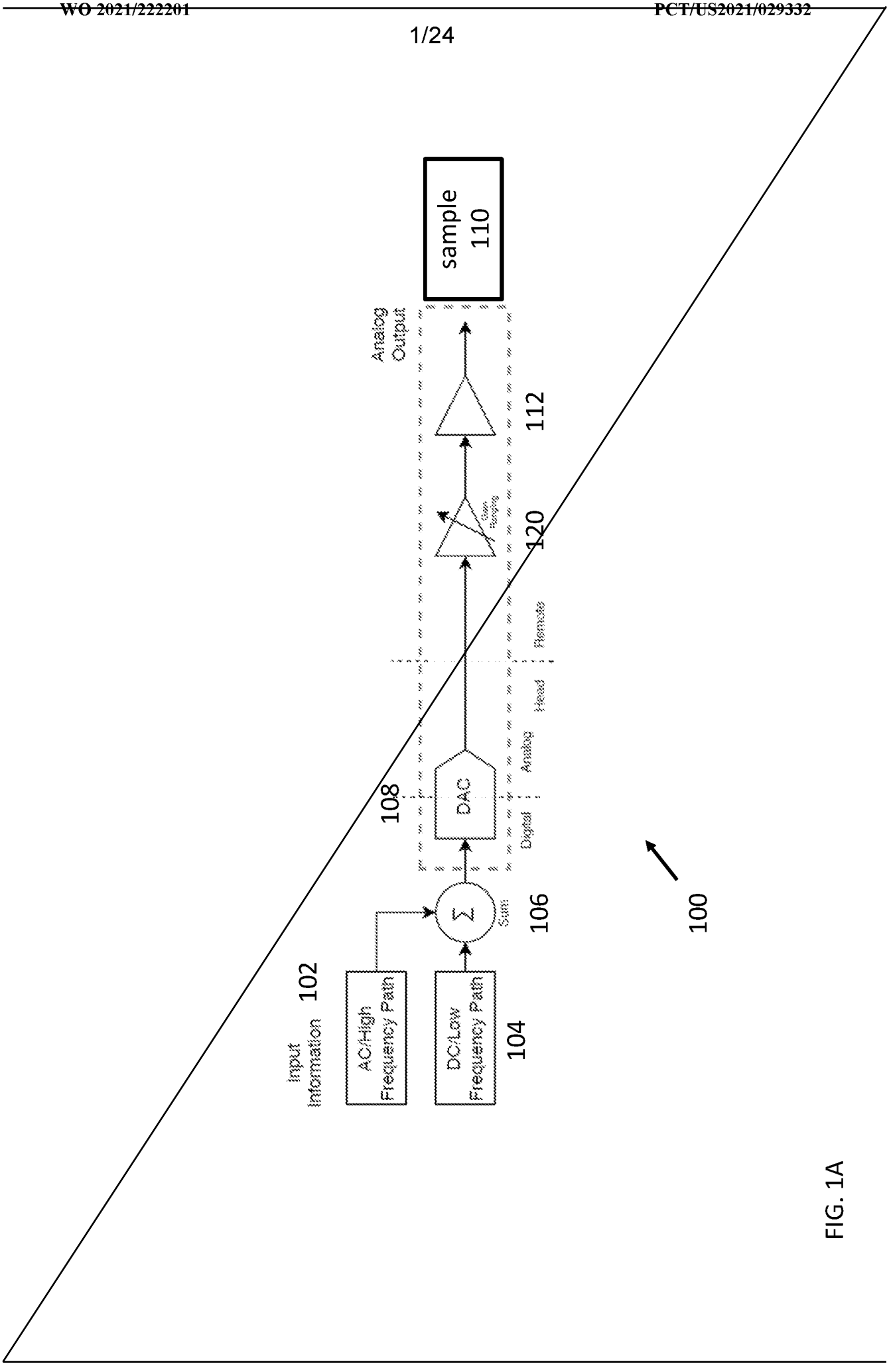

sample
110
Analog
Output
112
120
Gain
Tuning
Remote
Head
Analog
Digital
DAC
108
Sum
106
Σ
AC/High
Frequency Path
DC/Low
Frequency Path
104
Input
Information
102
100

FIG. 1A

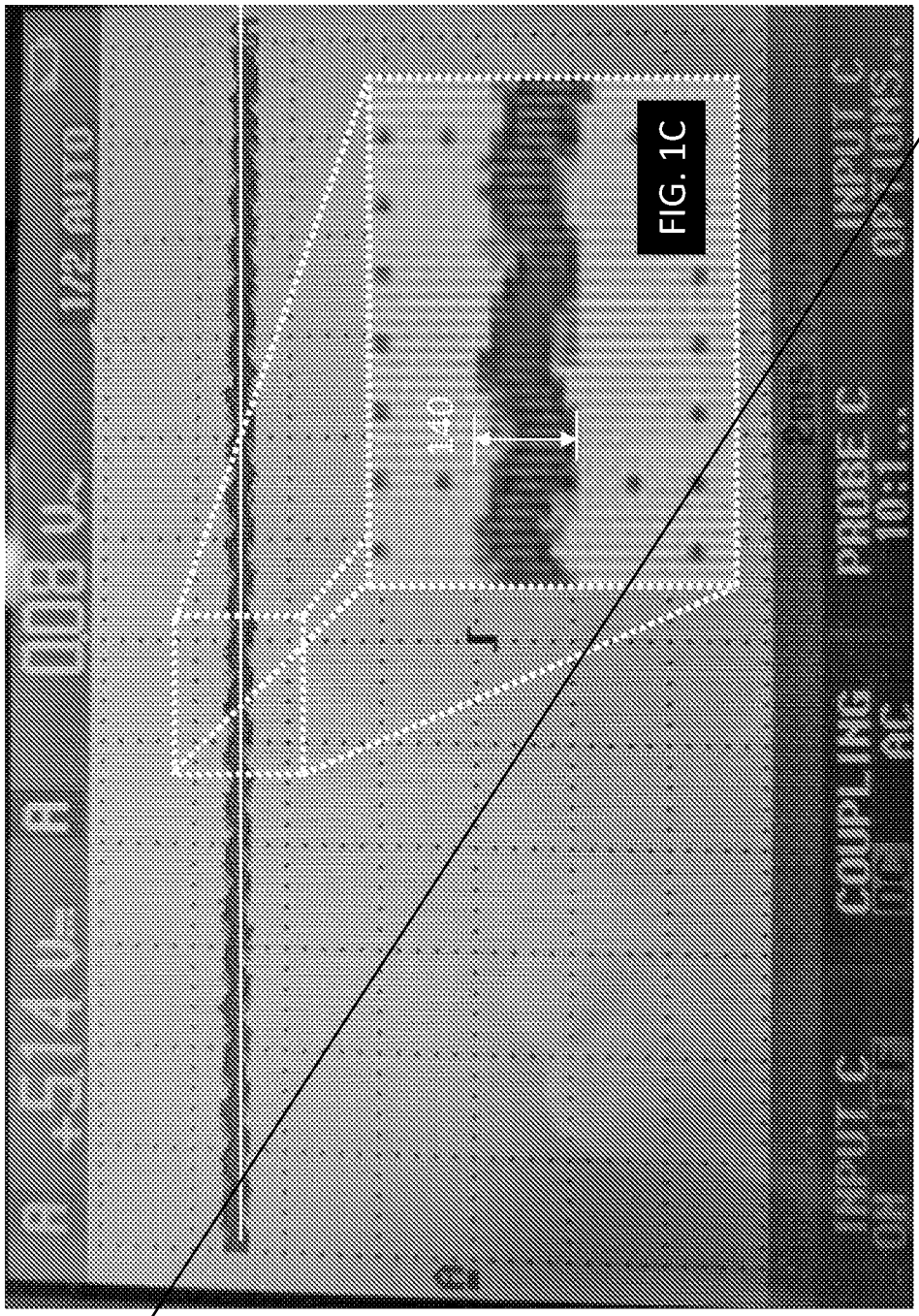


FIG. 1B

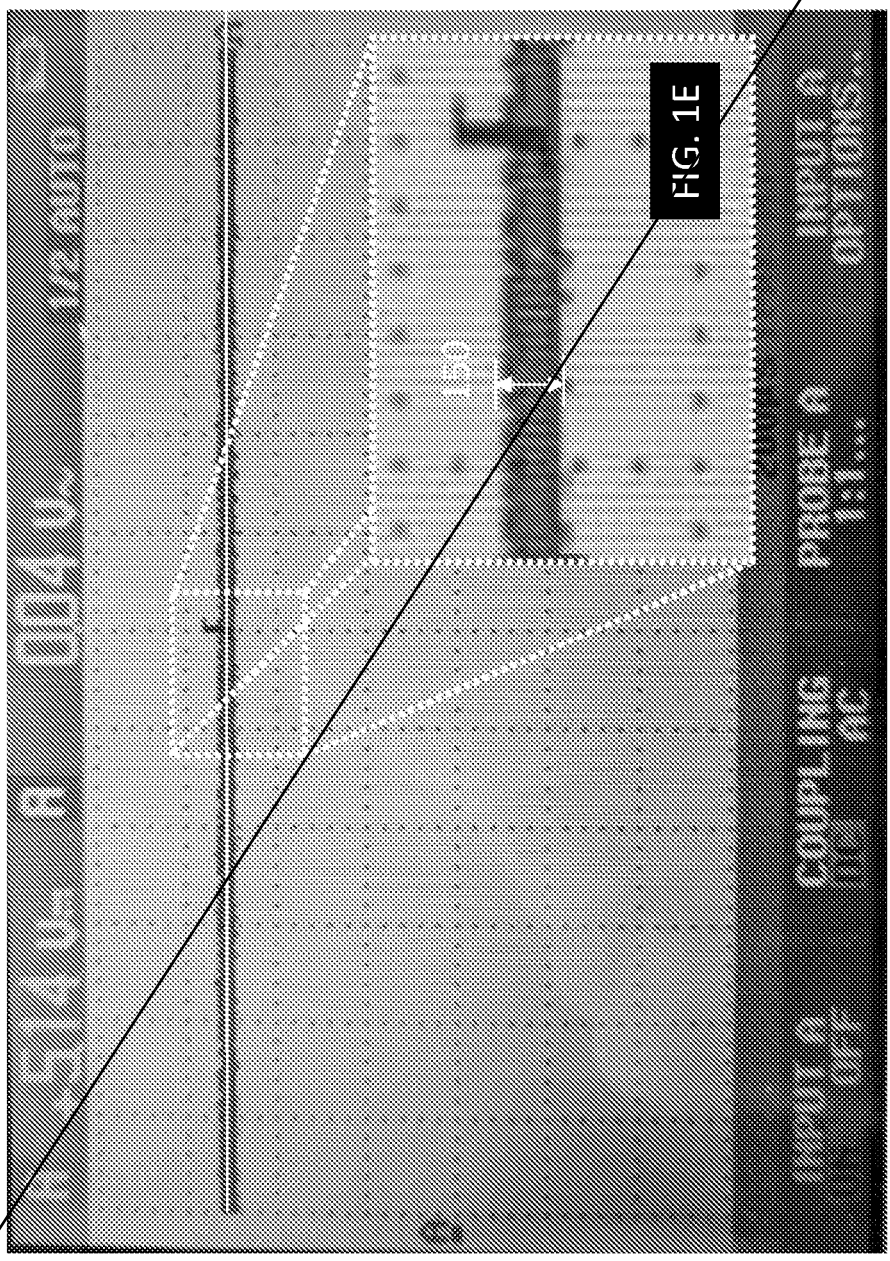


FIG. 1D

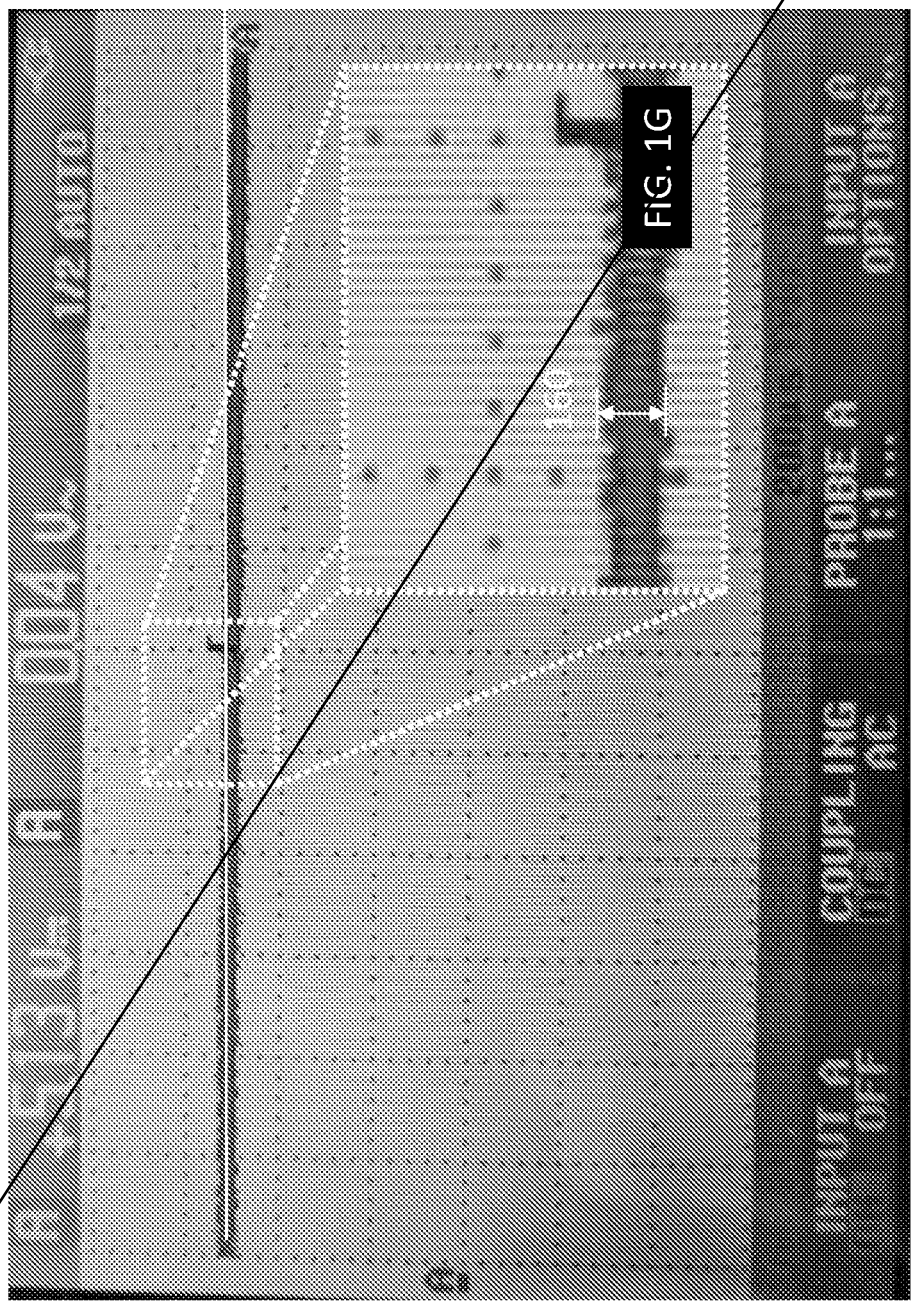


FIG. 1F

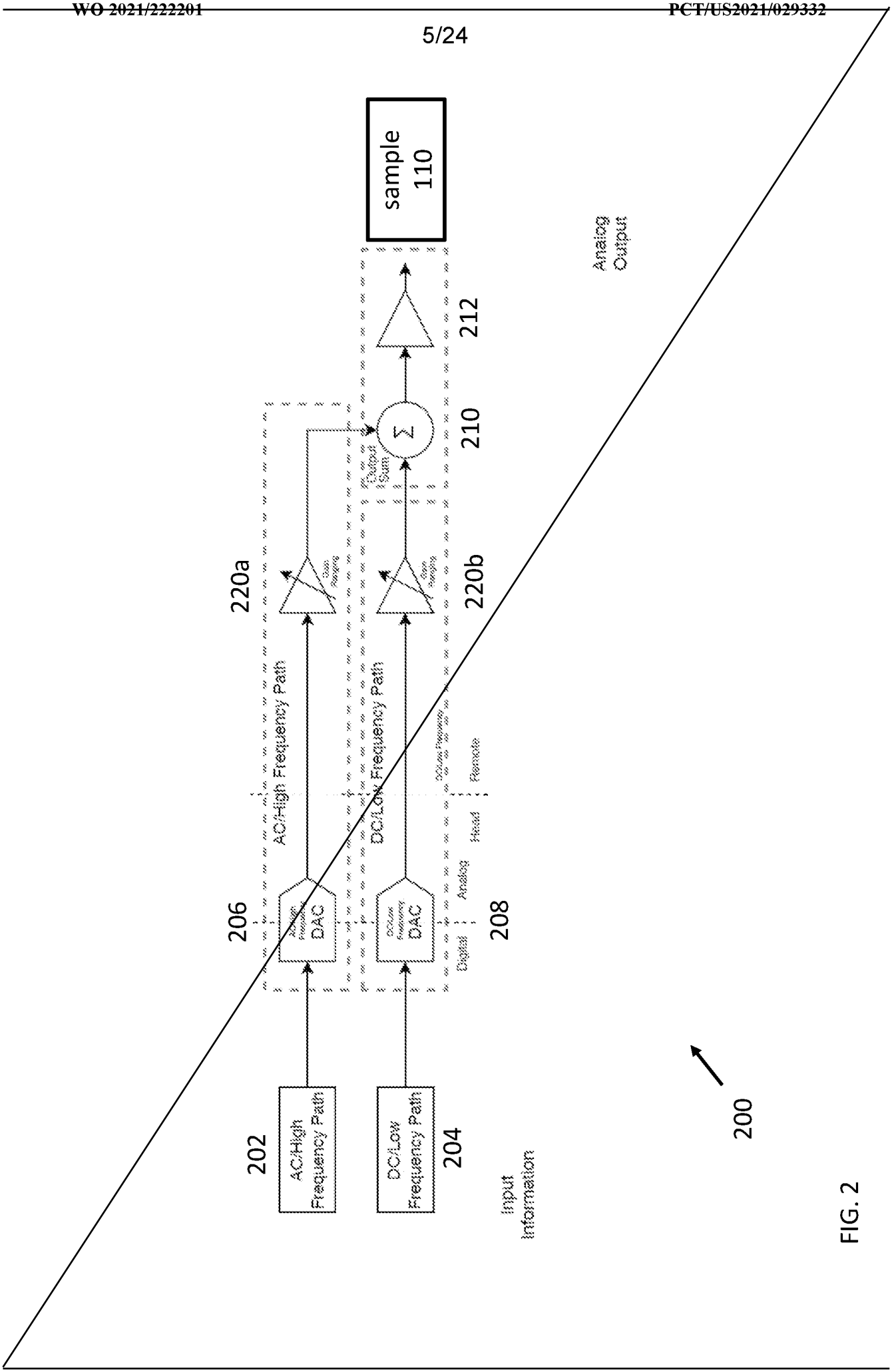

sample 110
Analog Output
212
210
220a
220b
206
208
AC/High Frequency Path
DC/Low Frequency Path
DAC
DAC
Digital
Analog
Remote
Head
202
204
AC/High Frequency Path
DC/Low Frequency Path
Input Information
200

FIG. 2

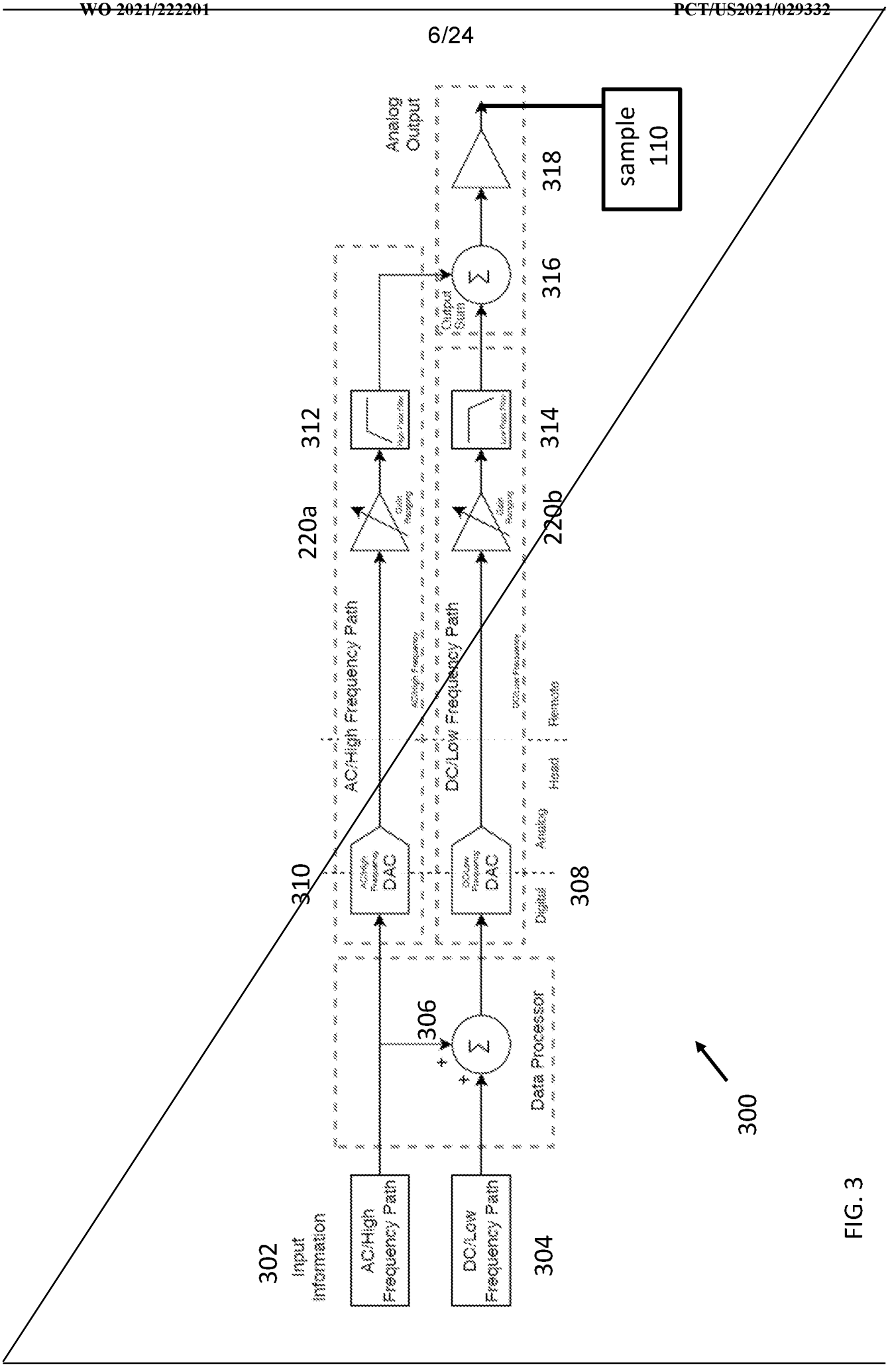

302
Input Information
AC/High Frequency Path
DC/Low Frequency Path
304
Data Processor
306
Σ
310
AC/High Frequency Path
DC/Low Frequency Path
DAC
DAC
Digital
Analog
Host
Remote
308
220a
220b
312
314
316
Σ
318
Analog Output
sample 110
300

FIG. 3

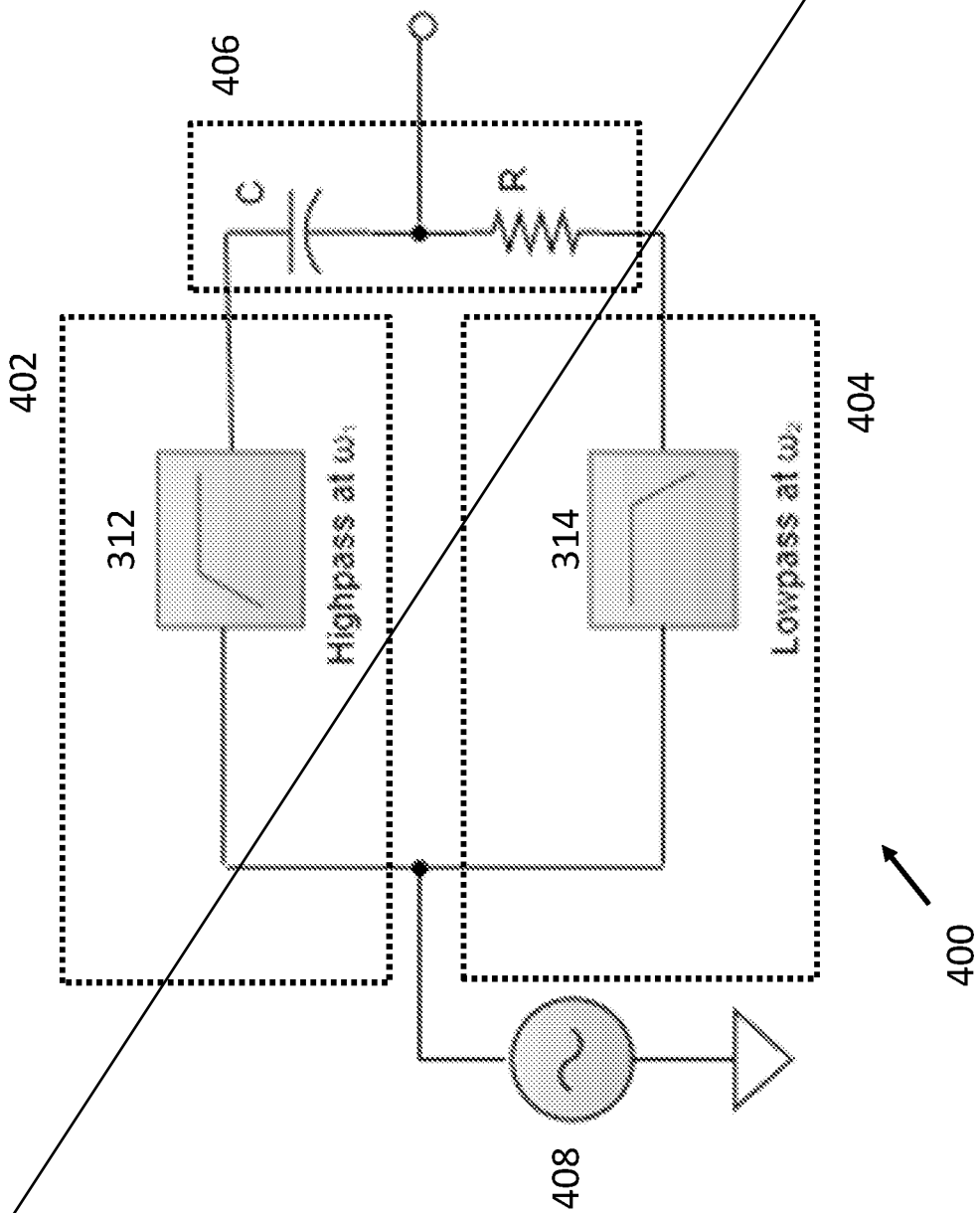

406
C
R
402
312
Highpass at ω_1
404
314
Lowpass at ω_2
400
408

FIG. 4

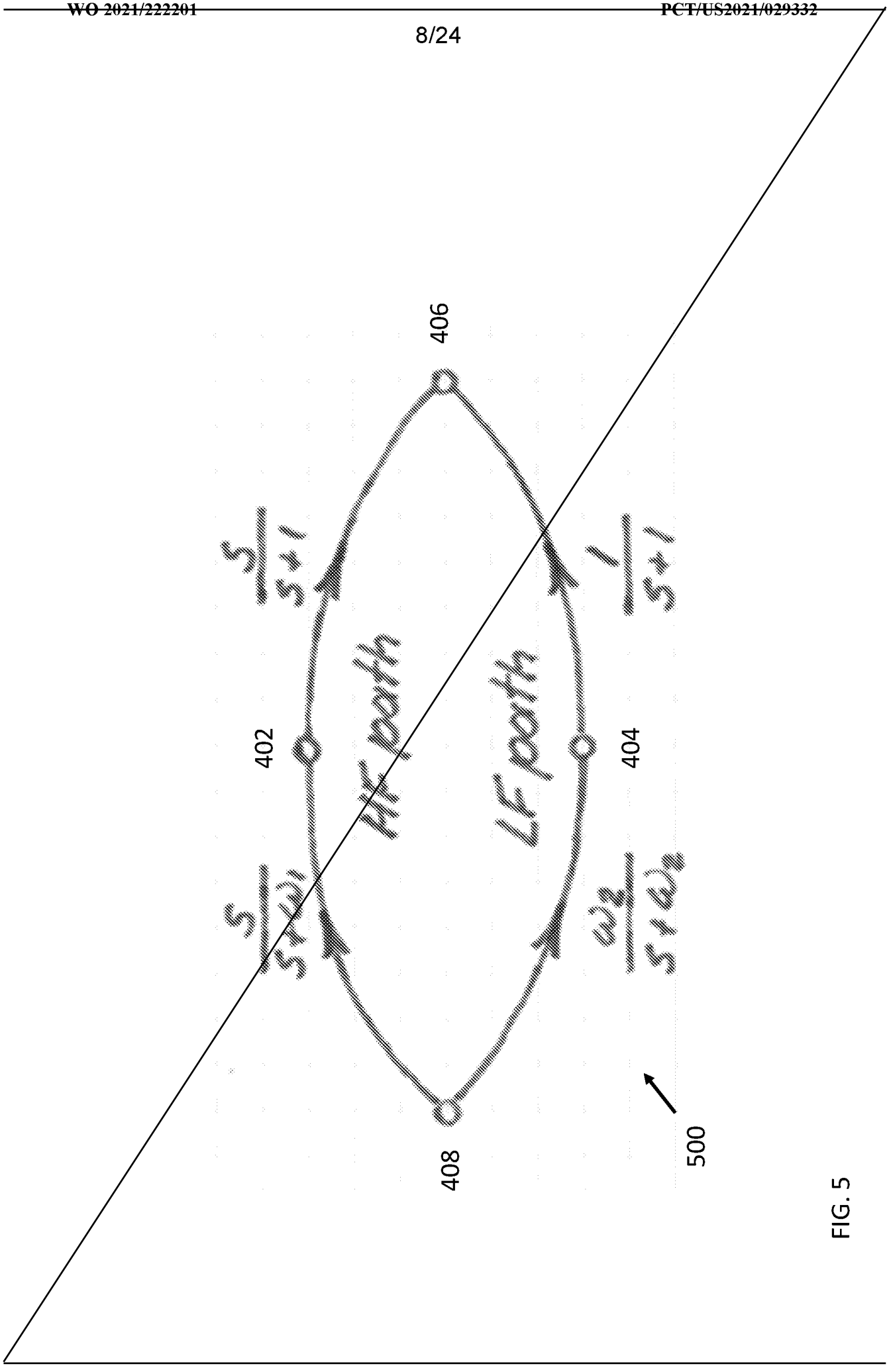


FIG. 5

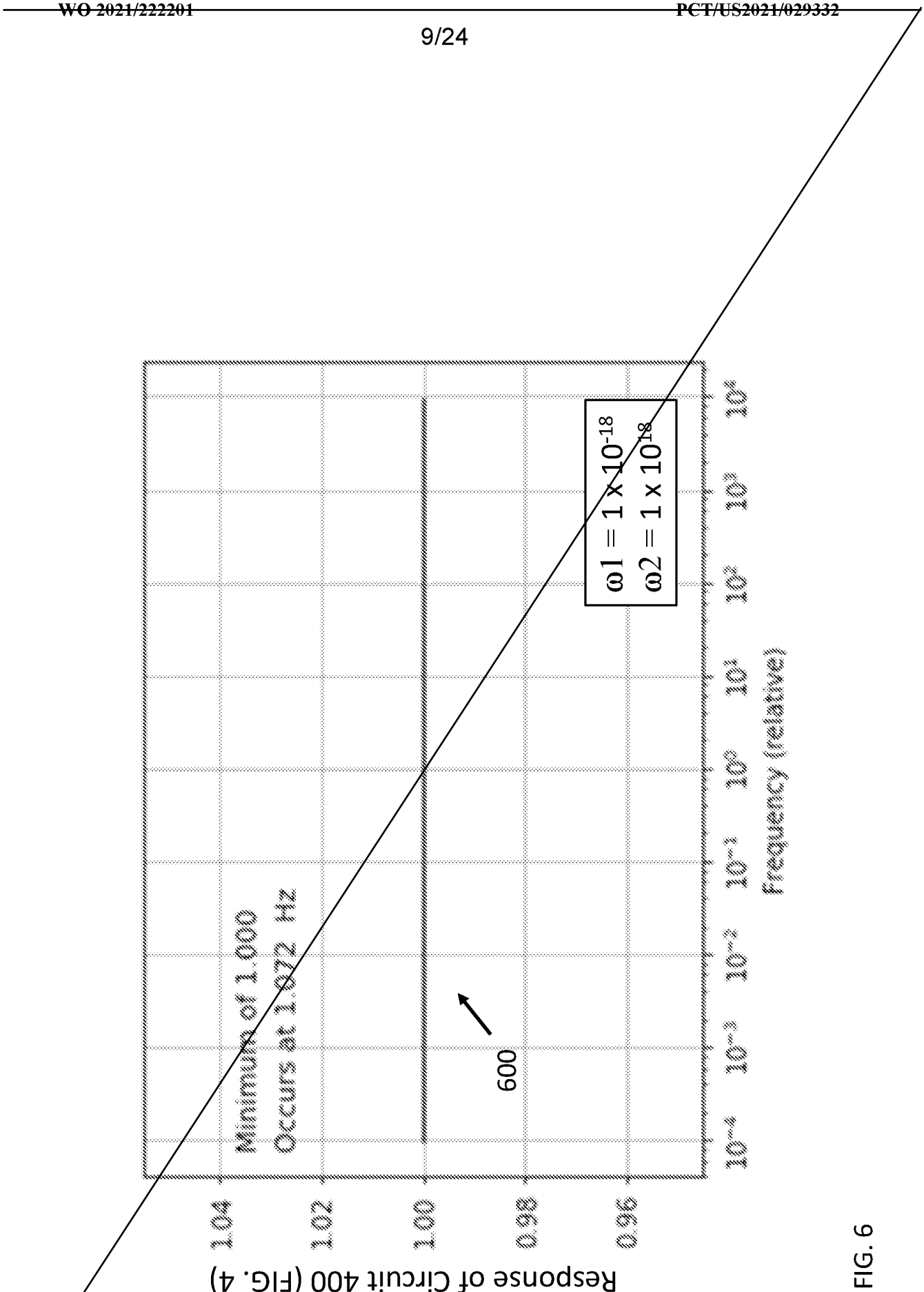

Response of Circuit 400 (FIG. 4)
1.04
1.02
1.00
0.98
0.96
Minimum of 1.000
Occurs at 1.072 Hz
600
ω1 = 1 x 10-18
ω2 = 1 x 10-18
10-4
10-3
10-2
10-1
100
101
102
103
104
Frequency (relative)

FIG. 6

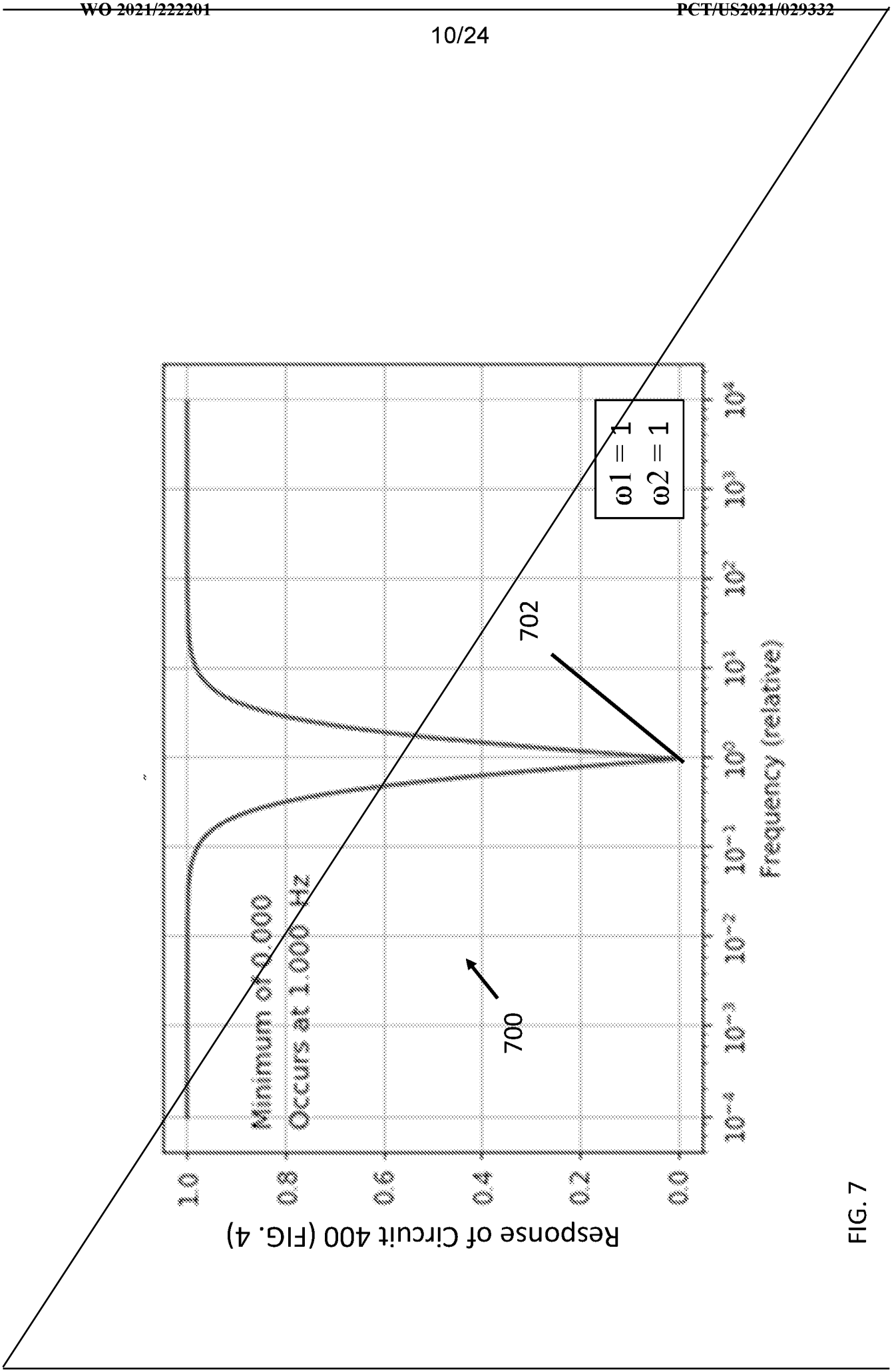

Response of Circuit 400 (FIG. 4)
1.0
0.8
0.6
0.4
0.2
0.0
Minimum of 0.000
Occurs at 1.000 Hz
700
702
ω1 = 1
ω2 = 1
10⁻⁴
10⁻³
10⁻²
10⁻¹
10⁰
10¹
10²
10³
10⁴
Frequency (relative)

FIG. 7

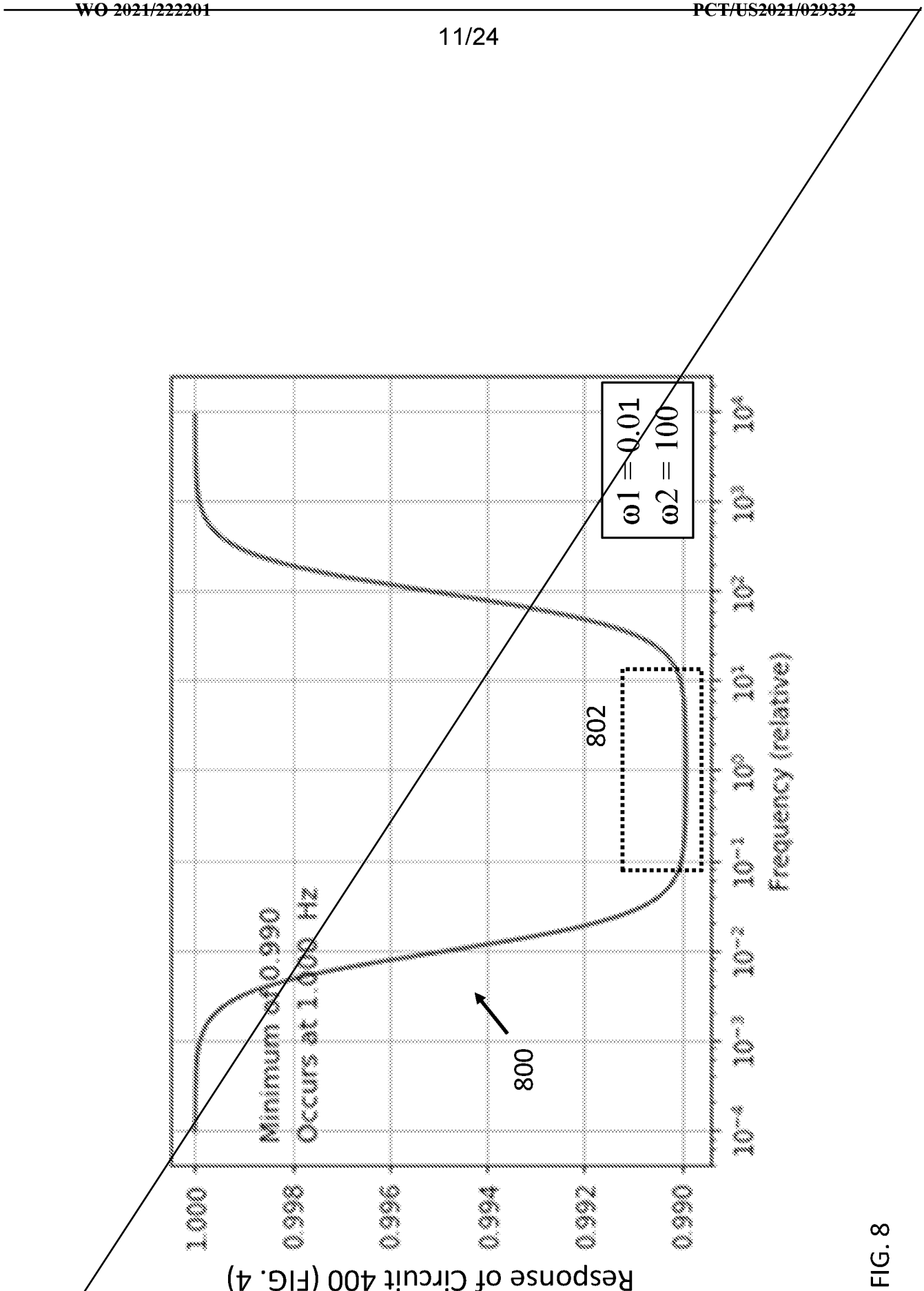

Response of Circuit 400 (FIG. 4)
1.000
0.998
0.996
0.994
0.992
0.990
Minimum of 0.990
Occurs at 1.000 Hz
800
802
ω1 = 0.01
ω2 = 100
10⁻⁴ 10⁻³ 10⁻² 10⁻¹ 10⁰ 10¹ 10² 10³ 10⁴
Frequency (relative)

FIG. 8

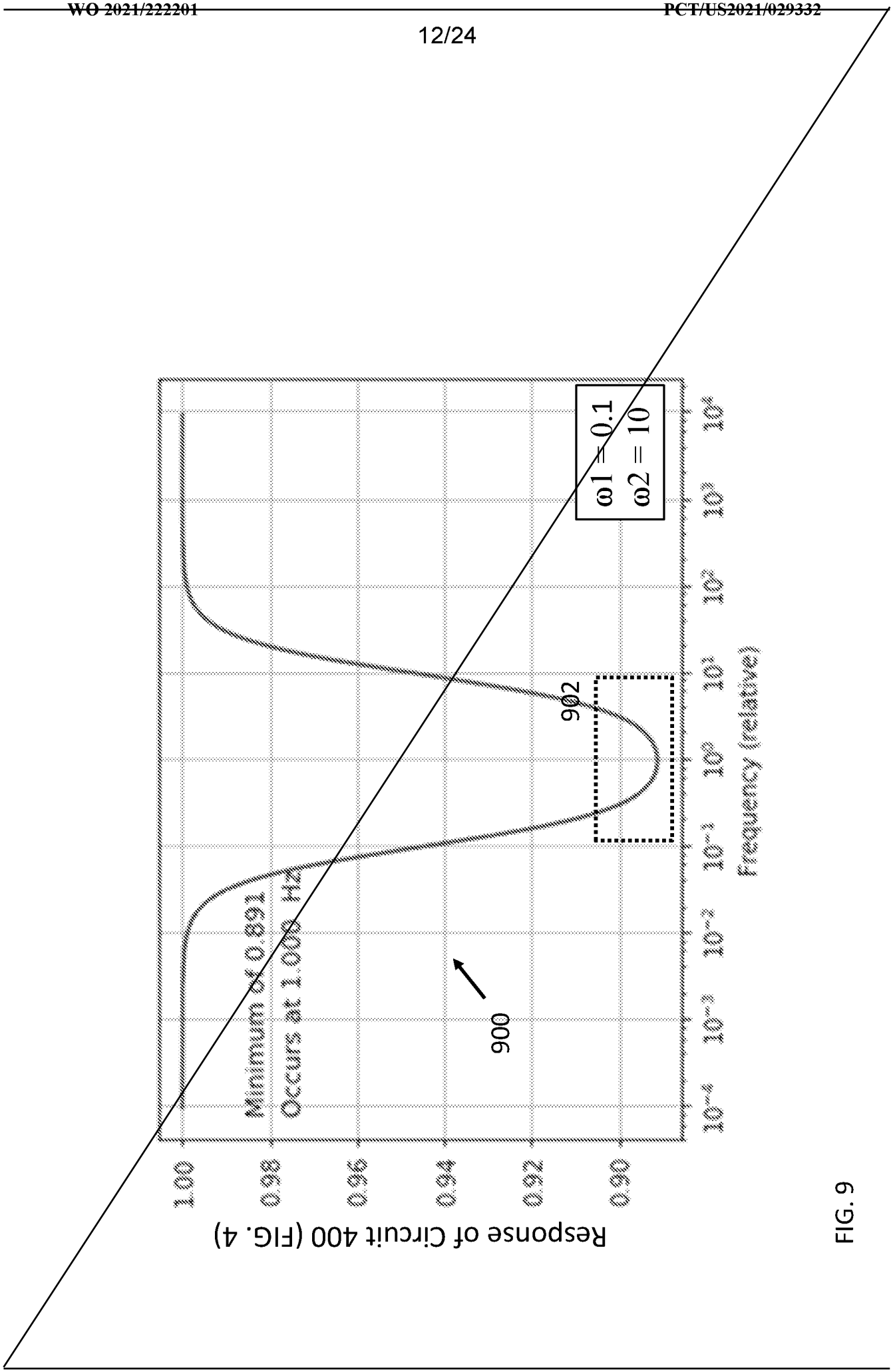

Response of Circuit 400 (FIG. 4)
1.00
0.98
0.96
0.94
0.92
0.90
Minimum of 0.691
Occurs at 1.000 Hz
900
902
ω1 = 0.1
ω2 = 10
10⁻⁴
10⁻³
10⁻²
10⁻¹
10⁰
10¹
10²
10³
10⁴
Frequency (relative)

FIG. 9

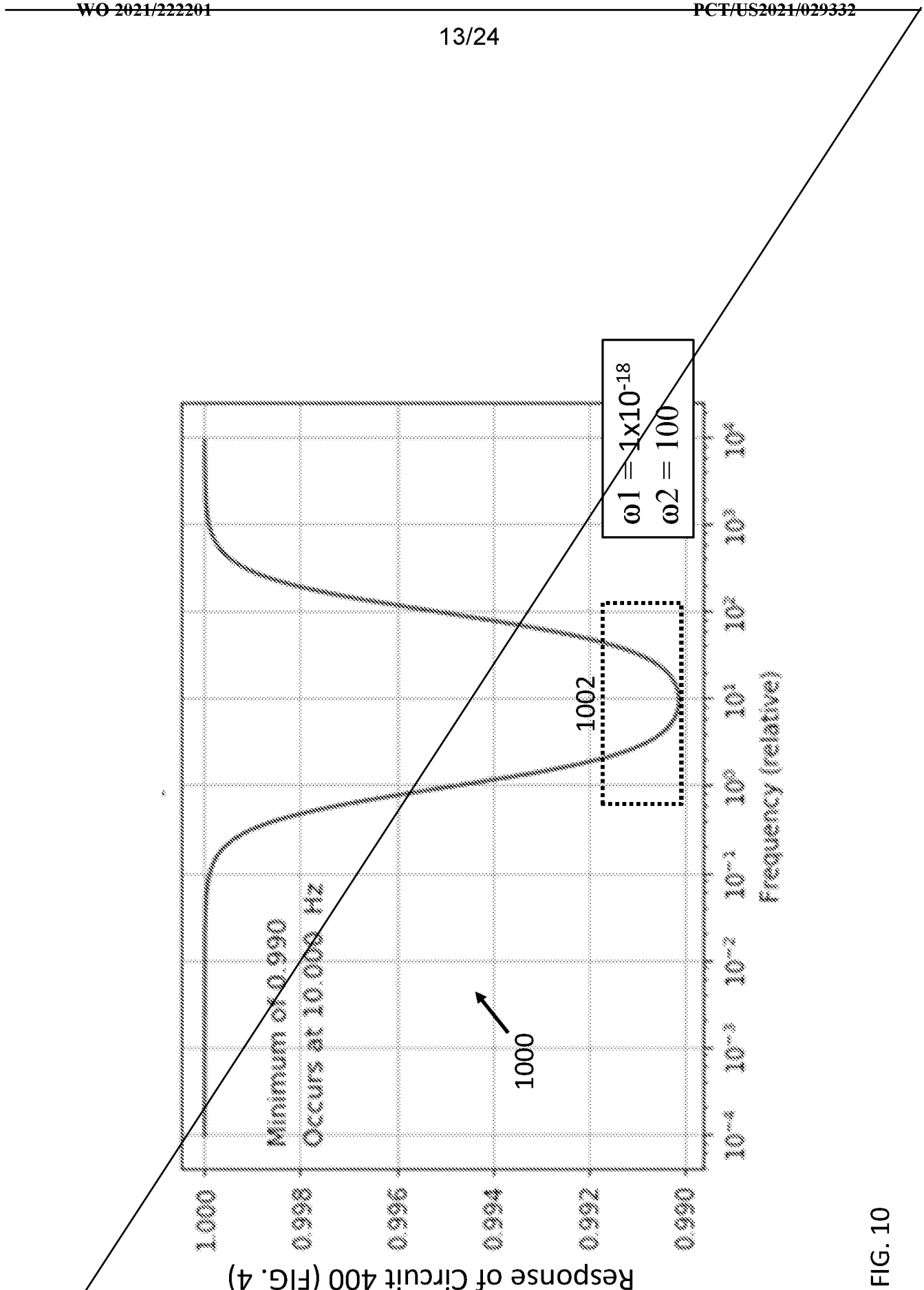

Response of Circuit 400 (FIG. 4)
1.000
0.998
0.996
0.994
0.992
0.990
Minimum of 0.990
Occurs at 10,000 Hz
1000
1002
ω1 = 1x10-18
ω2 = 100
10-4
10-3
10-2
10-1
100
101
102
103
104
Frequency (relative)

FIG. 10

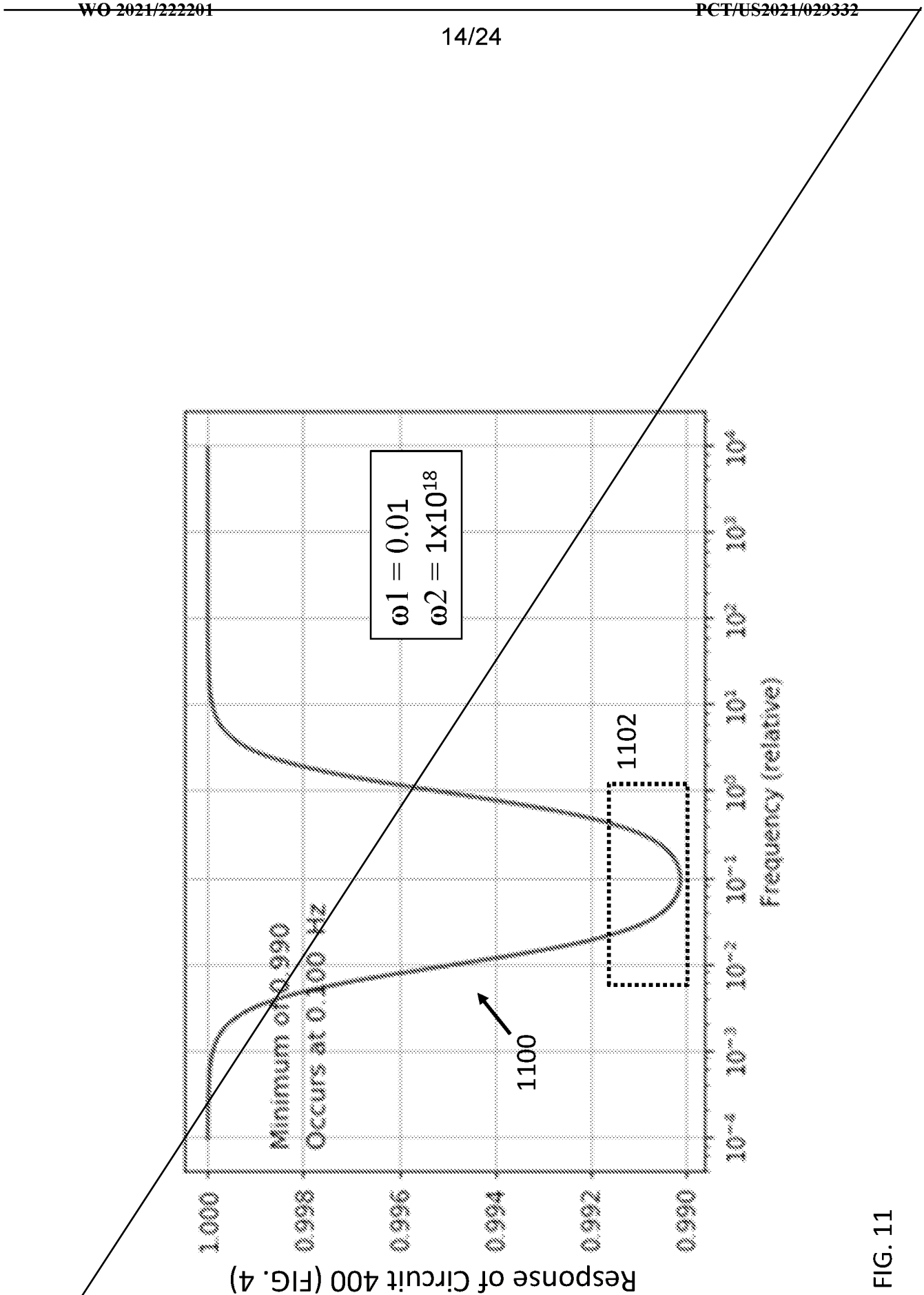

Response of Circuit 400 (FIG. 4)
1.000
0.998
0.996
0.994
0.992
0.990
Minimum of 0.990
Occurs at 0.100 Hz
ω1 = 0.01
ω2 = 1x10^18
1100
1102
10^-4
10^-3
10^-2
10^-1
10^0
10^1
10^2
10^3
10^4
Frequency (relative)

FIG. 11

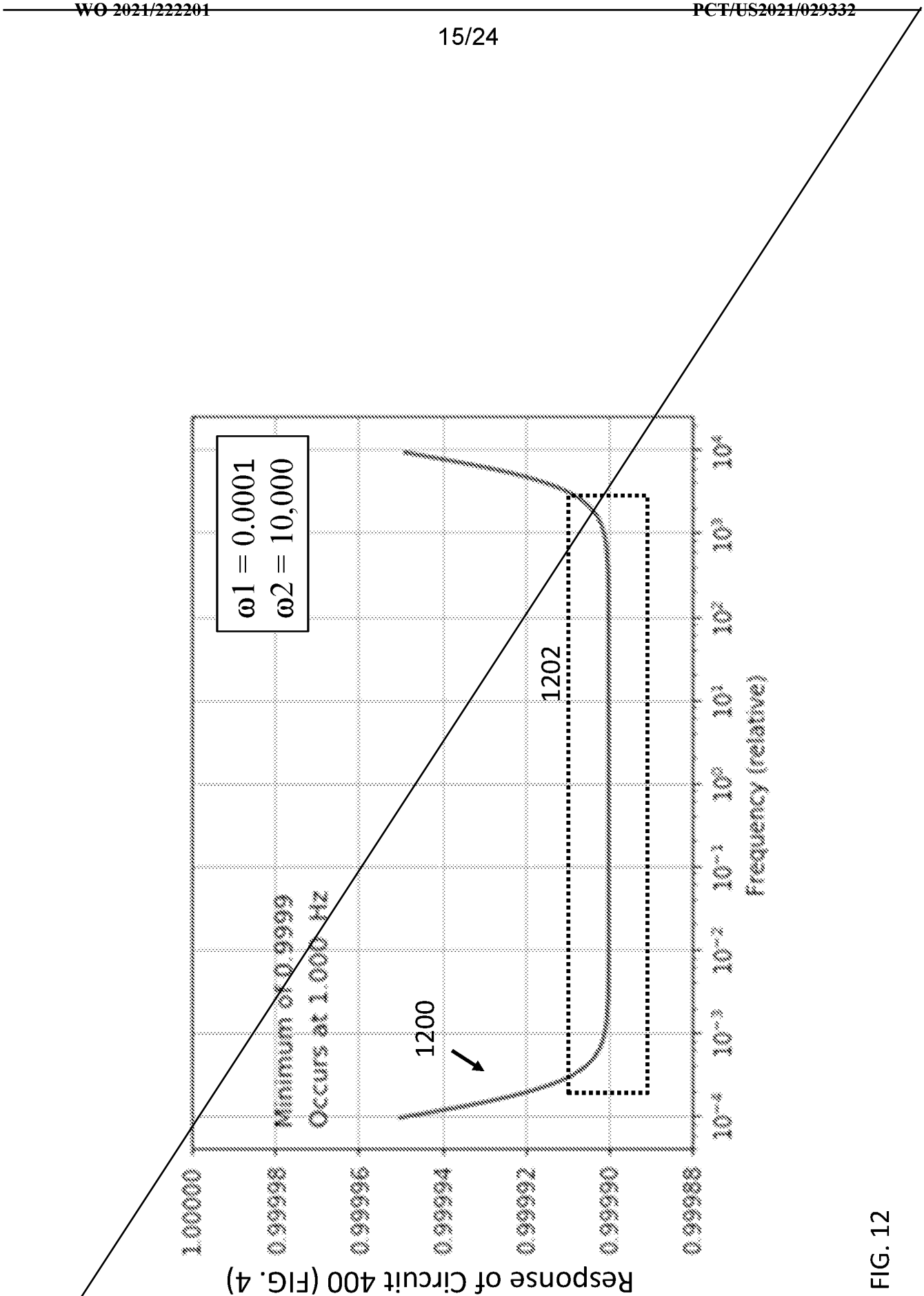

Response of Circuit 400 (FIG. 4)
1.00000
0.99998
0.99996
0.99994
0.99992
0.99990
0.99988
Minimum of 0.9999
Occurs at 1.000 Hz
1200
1202
ω1 = 0.0001
ω2 = 10,000
Frequency (relative)
10⁻⁴
10⁻³
10⁻²
10⁻¹
10⁰
10¹
10²
10³
10⁴

FIG. 12

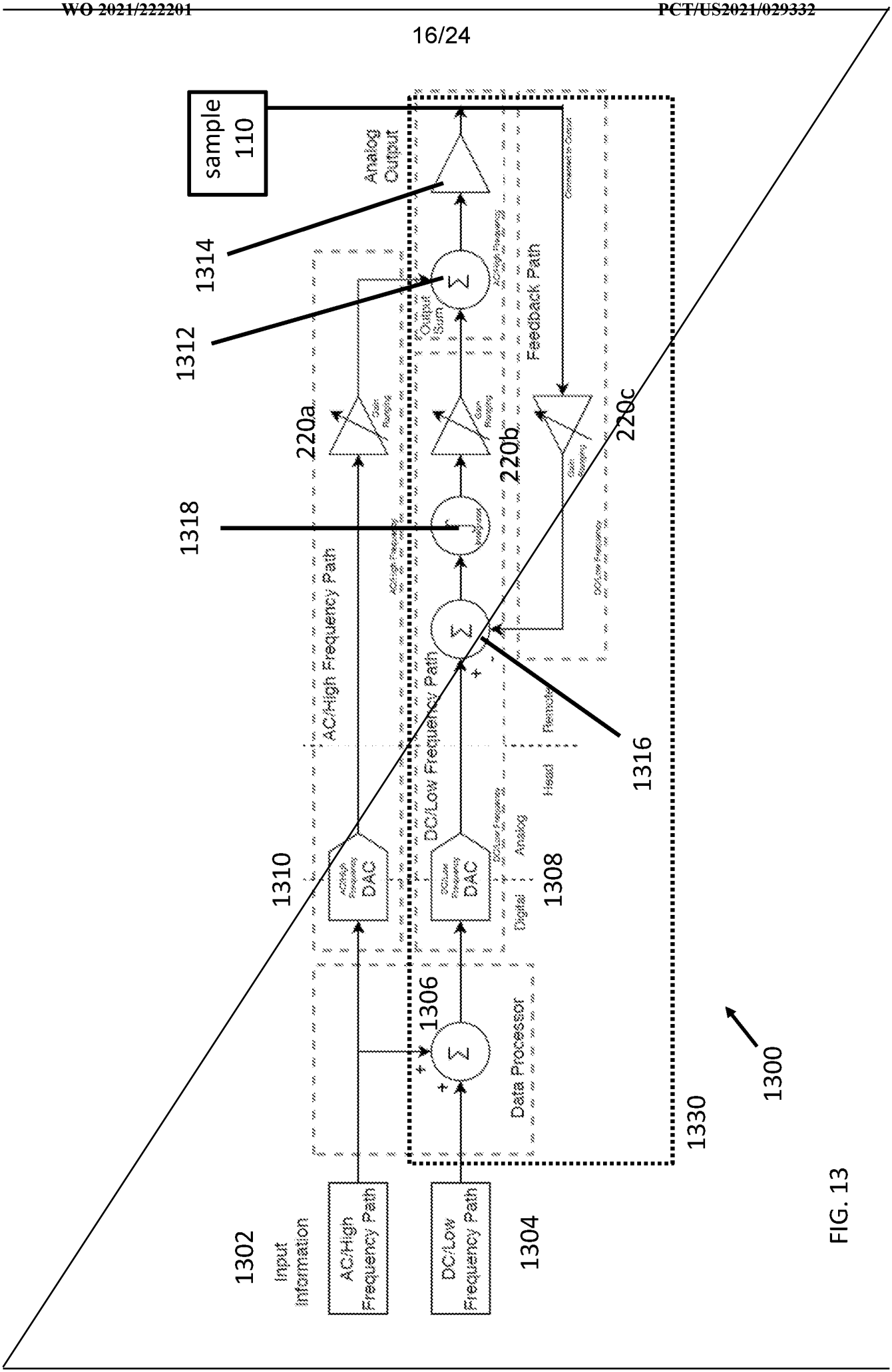

sample 110
1314
1312
1318
1316
1310
1308
1306
1330
1300
1302
1304
220a
220b
220c
Input Information
AC/High Frequency Path
DC/Low Frequency Path
Data Processor
Digital
Analog
DAC
Analog Output
Feedback Path
Output Sum
Gain
Adjust
Connection Cable
Remote
Head

FIG. 13

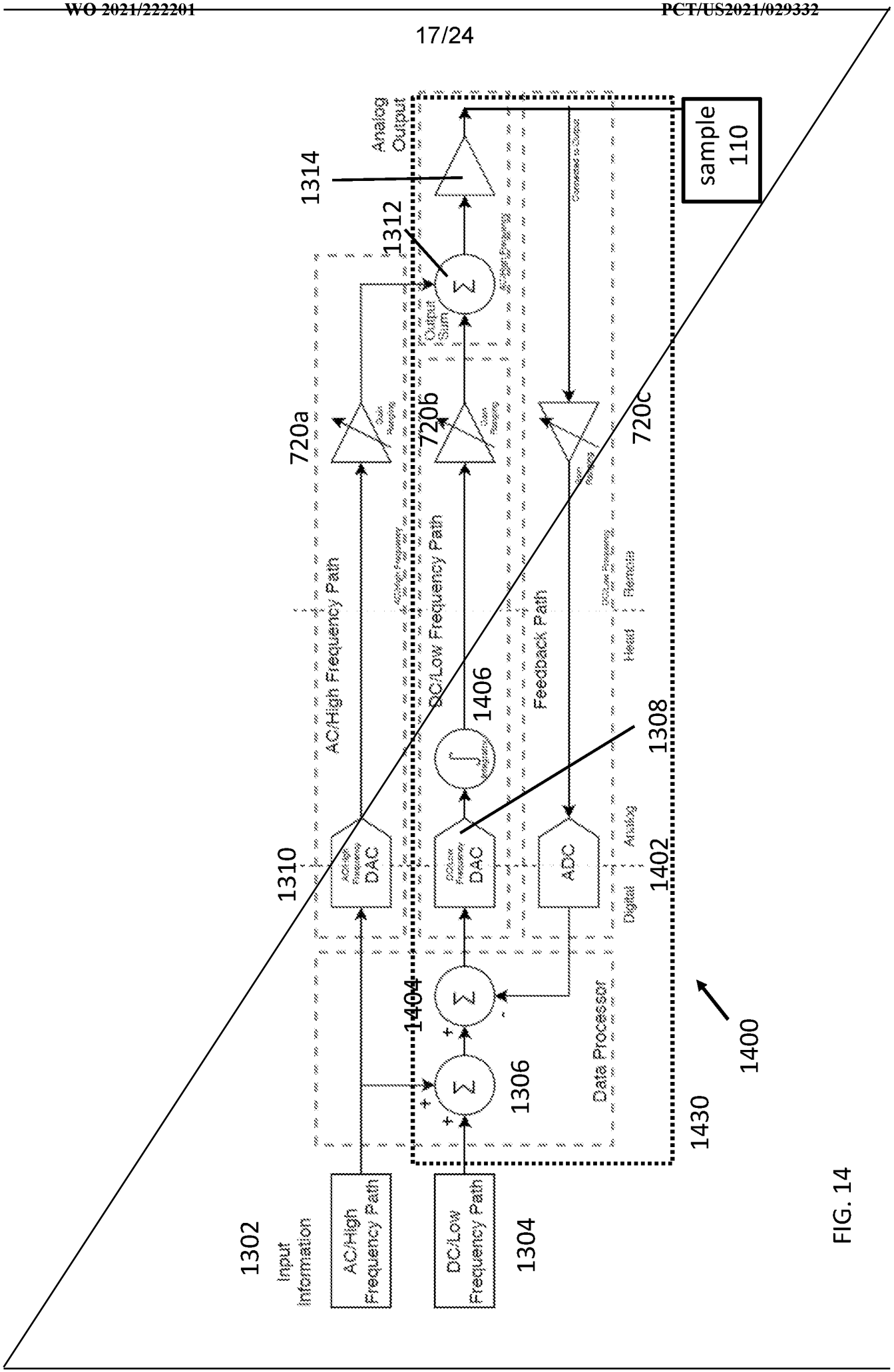

1302
Input Information
AC/High Frequency Path
DC/Low Frequency Path
1304
1306
1404
1430
1400
Data Processor
1310
1402
1308
DAC
DAC
ADC
Digital
Analog
1406
AC/High Frequency Path
DC/Low Frequency Path
Feedback Path
Head
Remote
720a
720b
720c
1312
1314
Analog Output
sample 110

FIG. 14

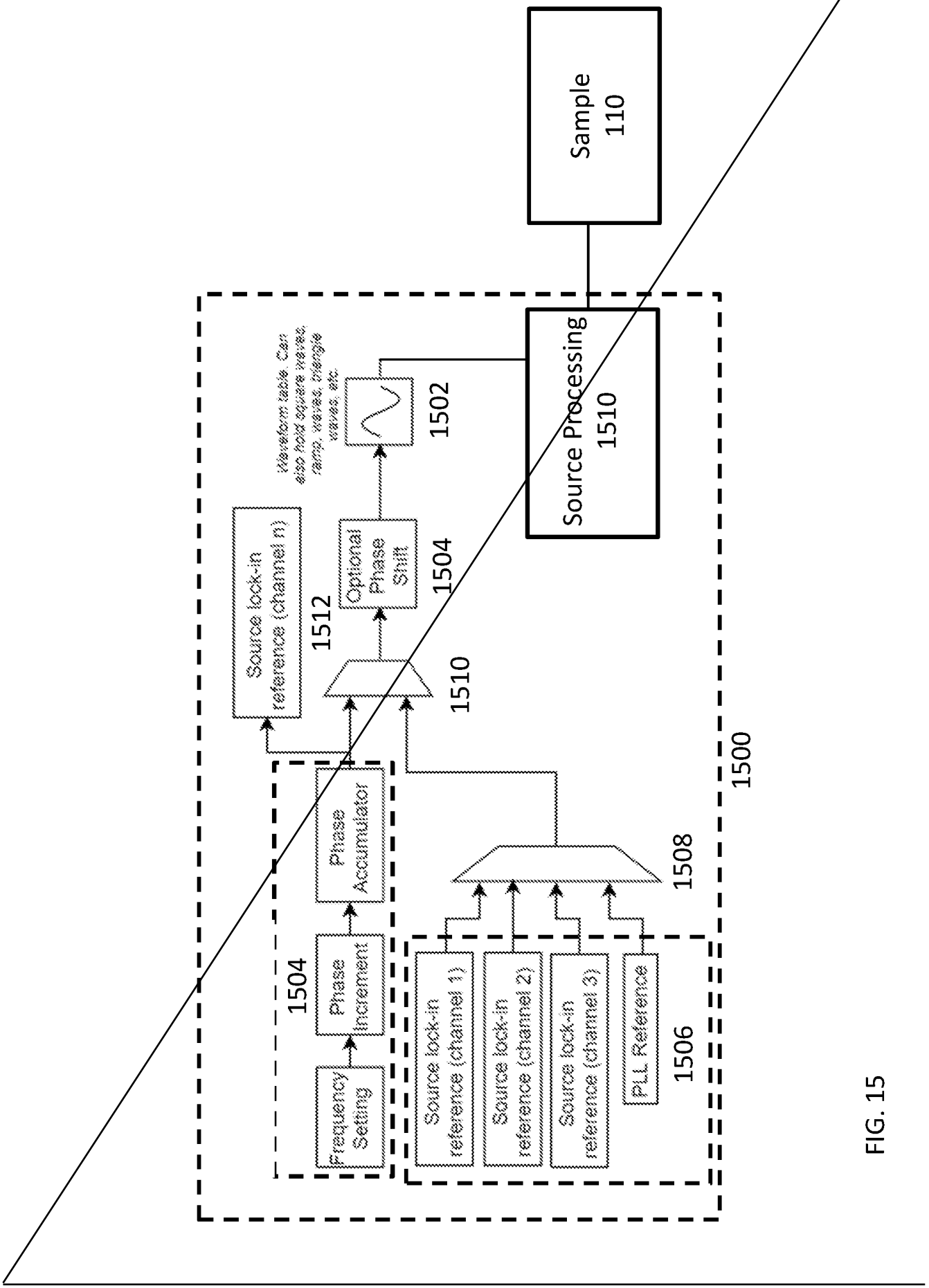

Sample
110
Source Processing
1510
1500
Waveform table. Can also hold square waves, ramp, waves, triangle waves, etc.
1502
Optional Phase Shift
1504
1512
Source lock-in reference (channel n)
1510
1504
Phase Accumulator
Phase Increment
Frequency Setting
1508
Source lock-in reference (channel 1)
Source lock-in reference (channel 2)
Source lock-in reference (channel 3)
PLL Reference
1506

FIG. 15

Position	Output
0	0.000
1	0.500
2	0.866
3	1.000
4	0.866
5	0.500
6	0.000
7	-0.500
8	-0.866
9	-1.000
10	-0.866
11	-0.500

1600

FIG. 16

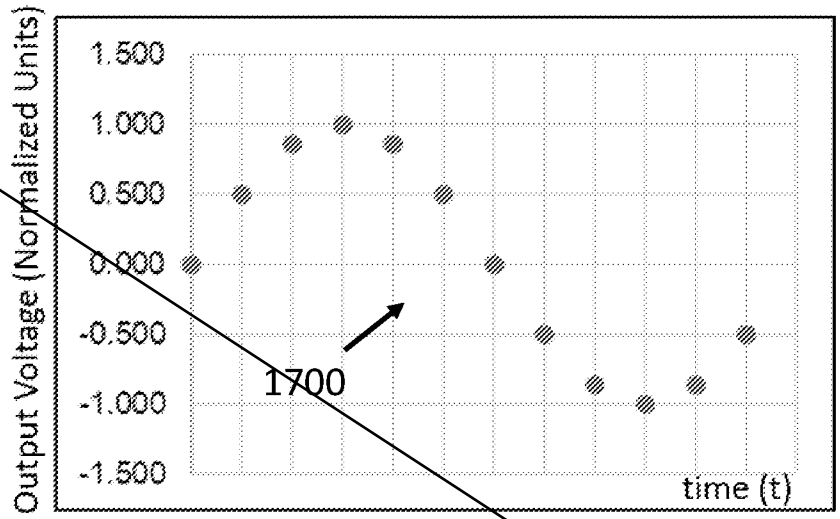


FIG. 17

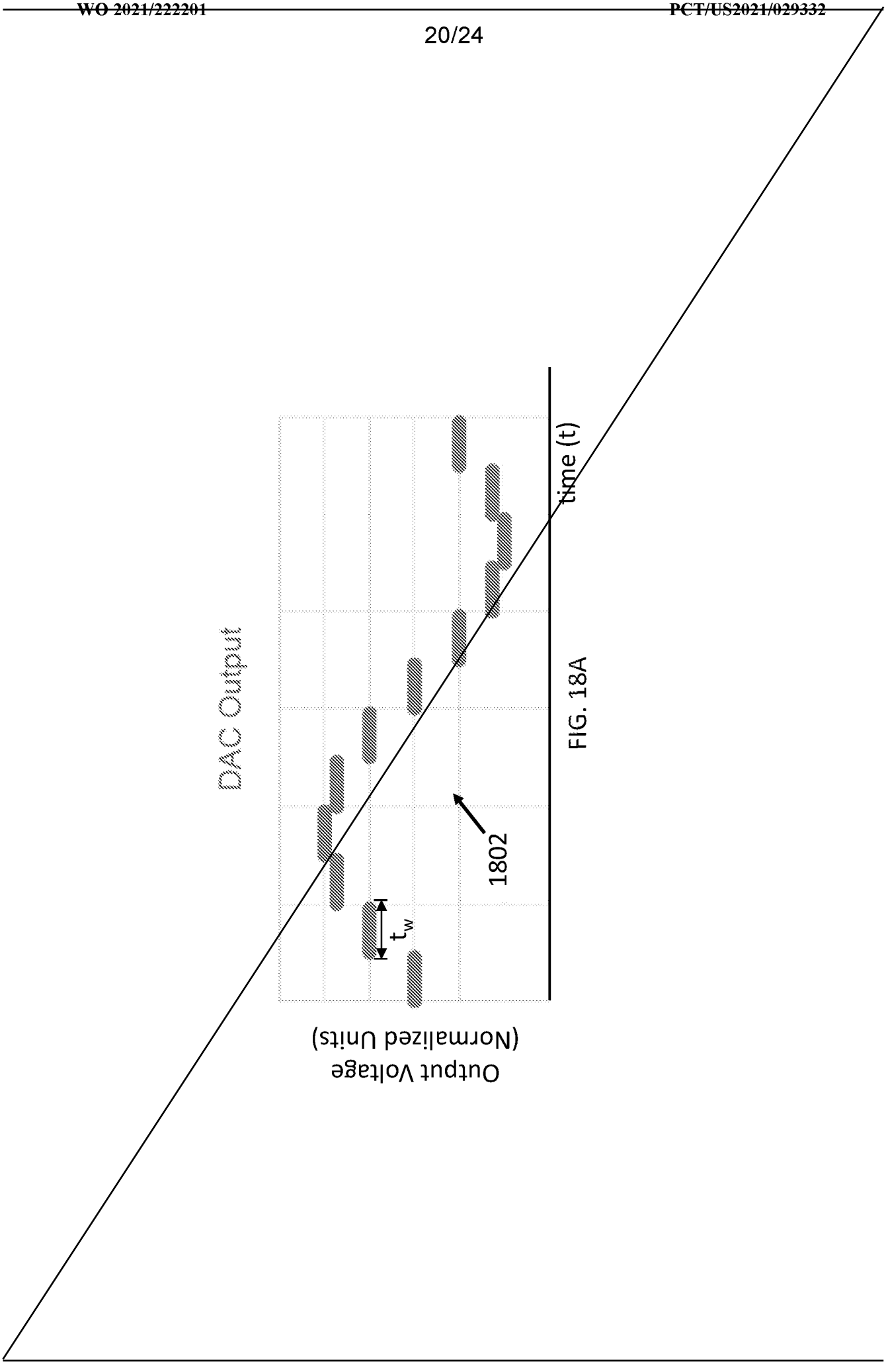


FIG. 18A

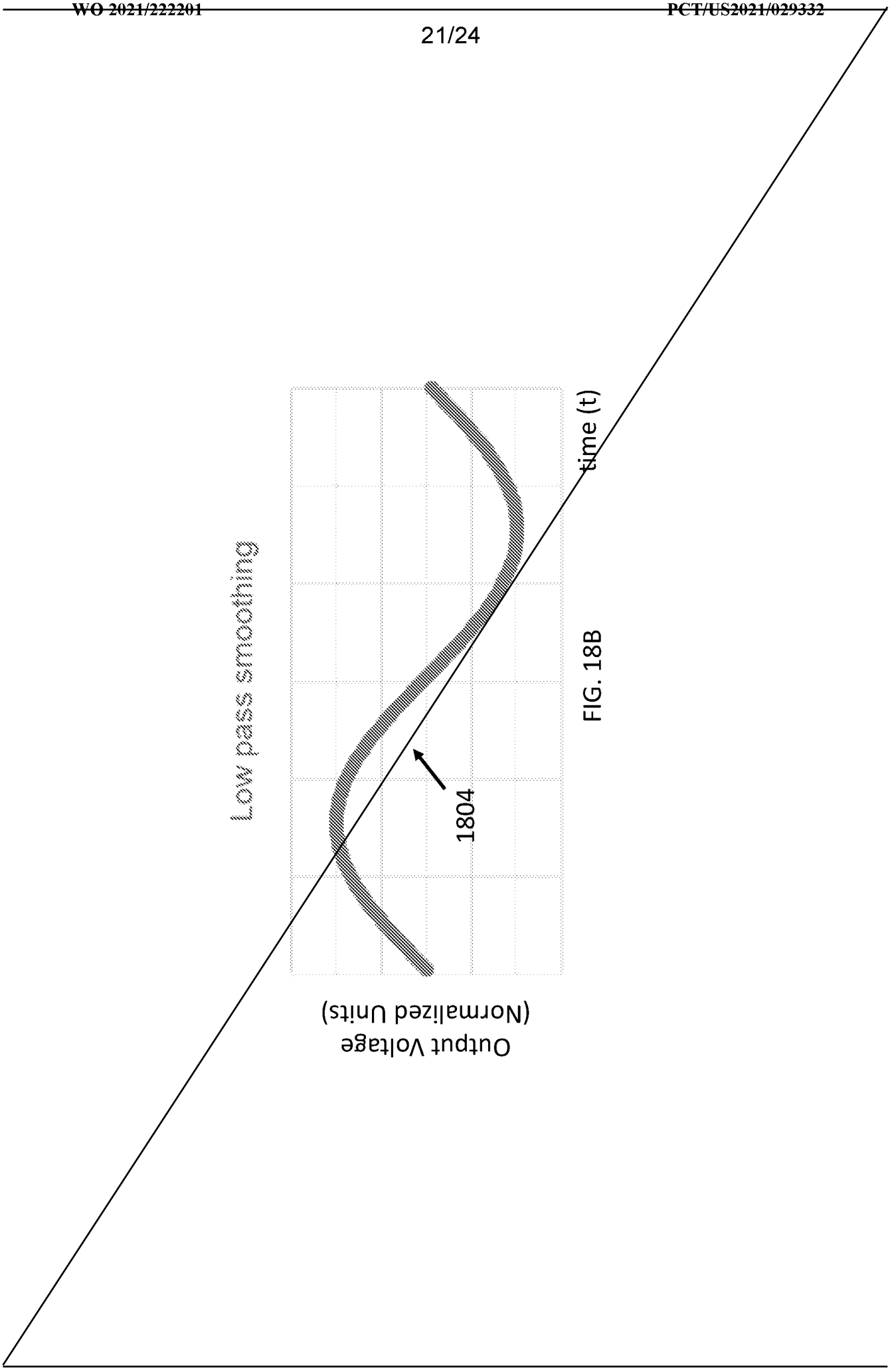

Low pass smoothing
1804
time (t)
Output Voltage
(Normalized Units)

FIG. 18B

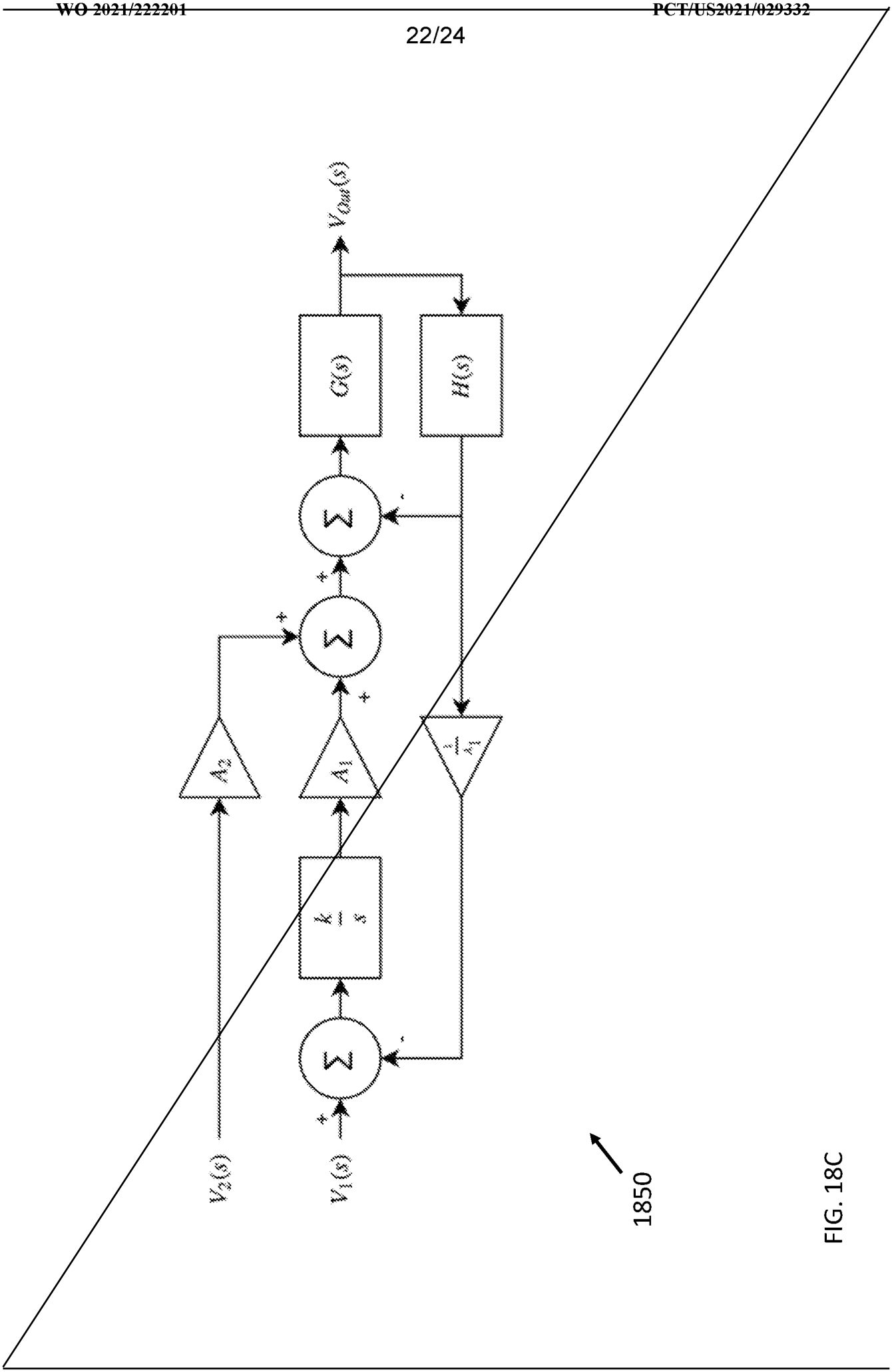


FIG. 18C

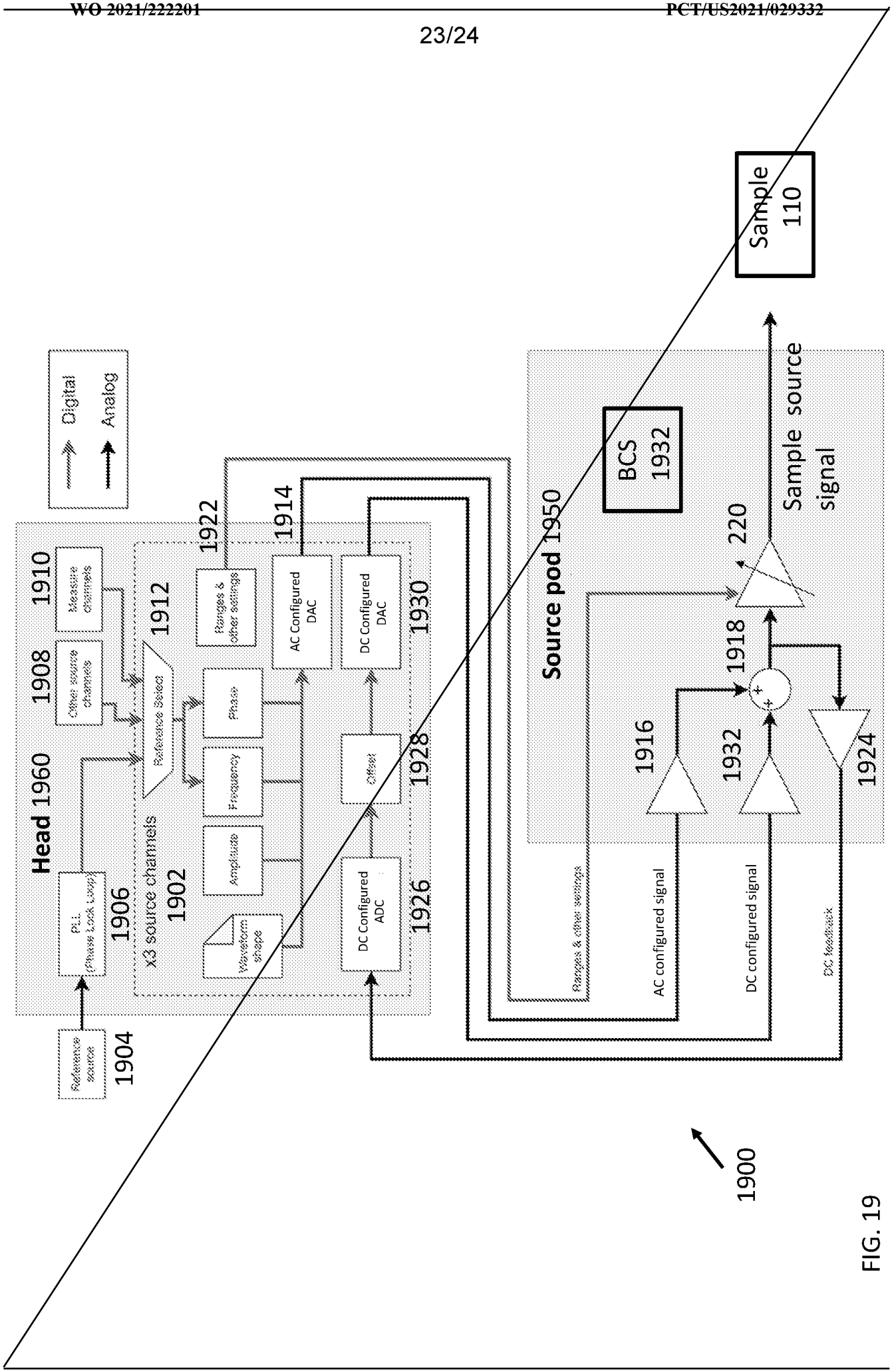

Digital
Analog
Head 1960
1908
Other source channels
1910
Measure channels
1912
Reference Select
1922
Ranges & other settings
1914
AC Configured DAC
DC Configured DAC
1930
Phase
Frequency
Amplitude
Waveform shape
Offset
1928
DC Configured ADC
1926
x3 source channels
1902
PLL Phase Lock Loop
1906
Reference source
1904
Source pod 1950
BCS 1932
Sample 110
Sample source signal
220
1918
1916
1932
1924
Ranges & other settings
AC configured signal
DC configured signal
DC feedback
1900

FIG. 19

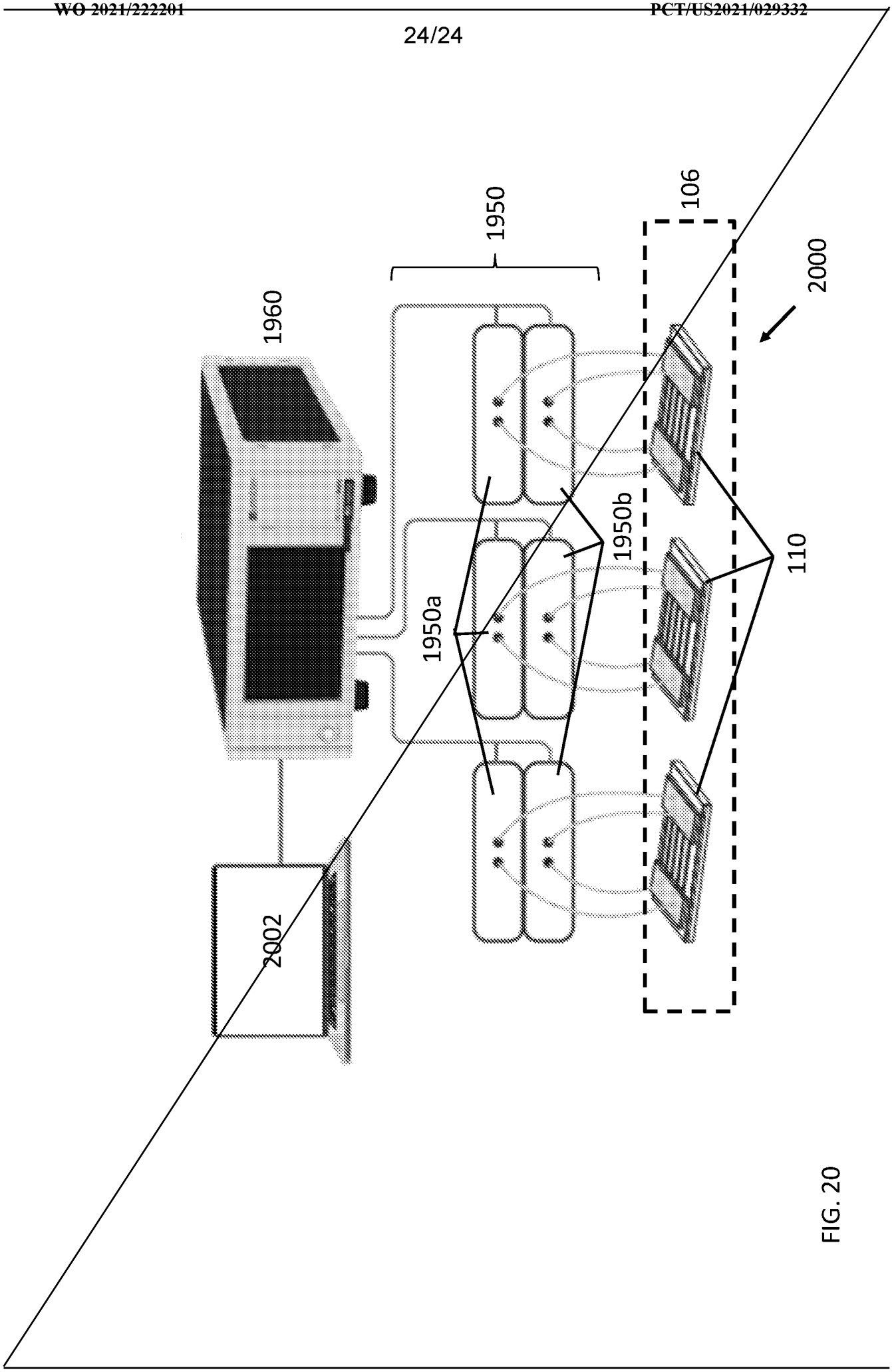


FIG. 20

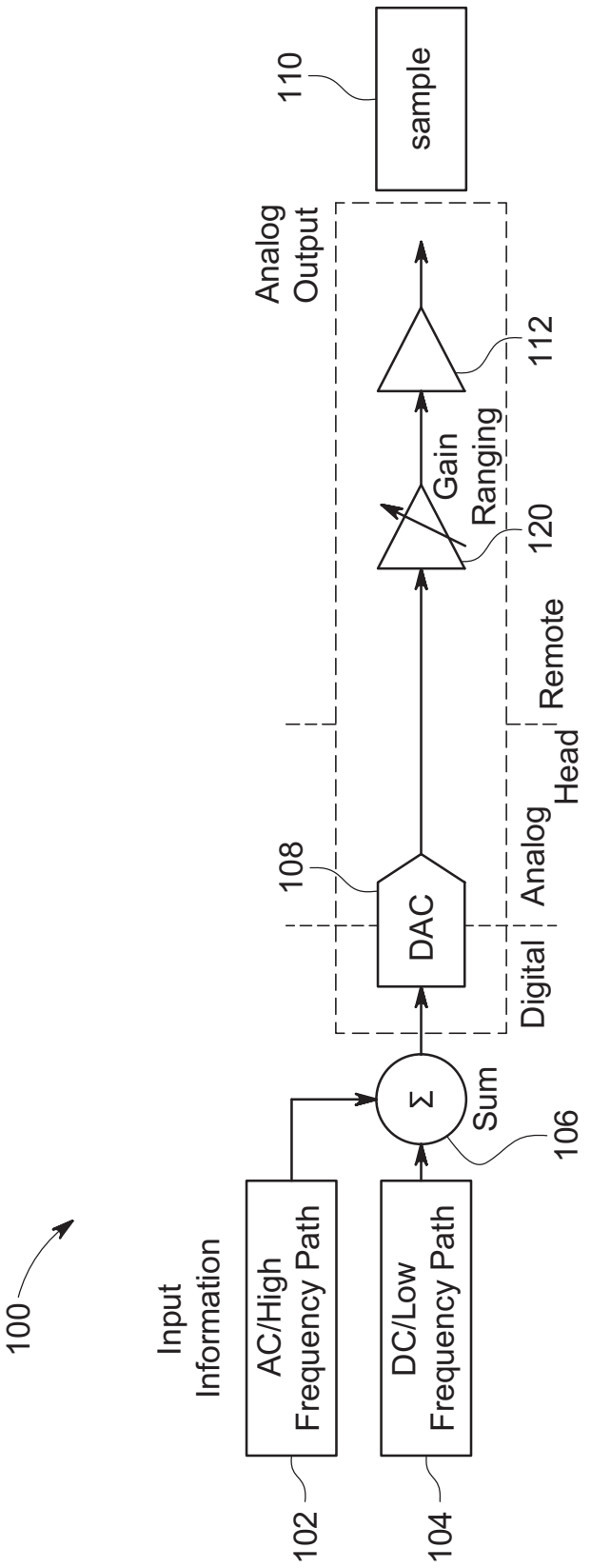

100
Input Information
AC/High Frequency Path
DC/Low Frequency Path
102
104
Σ
Sum
106
DAC
108
Digital
Analog
Gain Ranging
120
112
Analog Output
Remote Head
sample
110

FIG. 1A

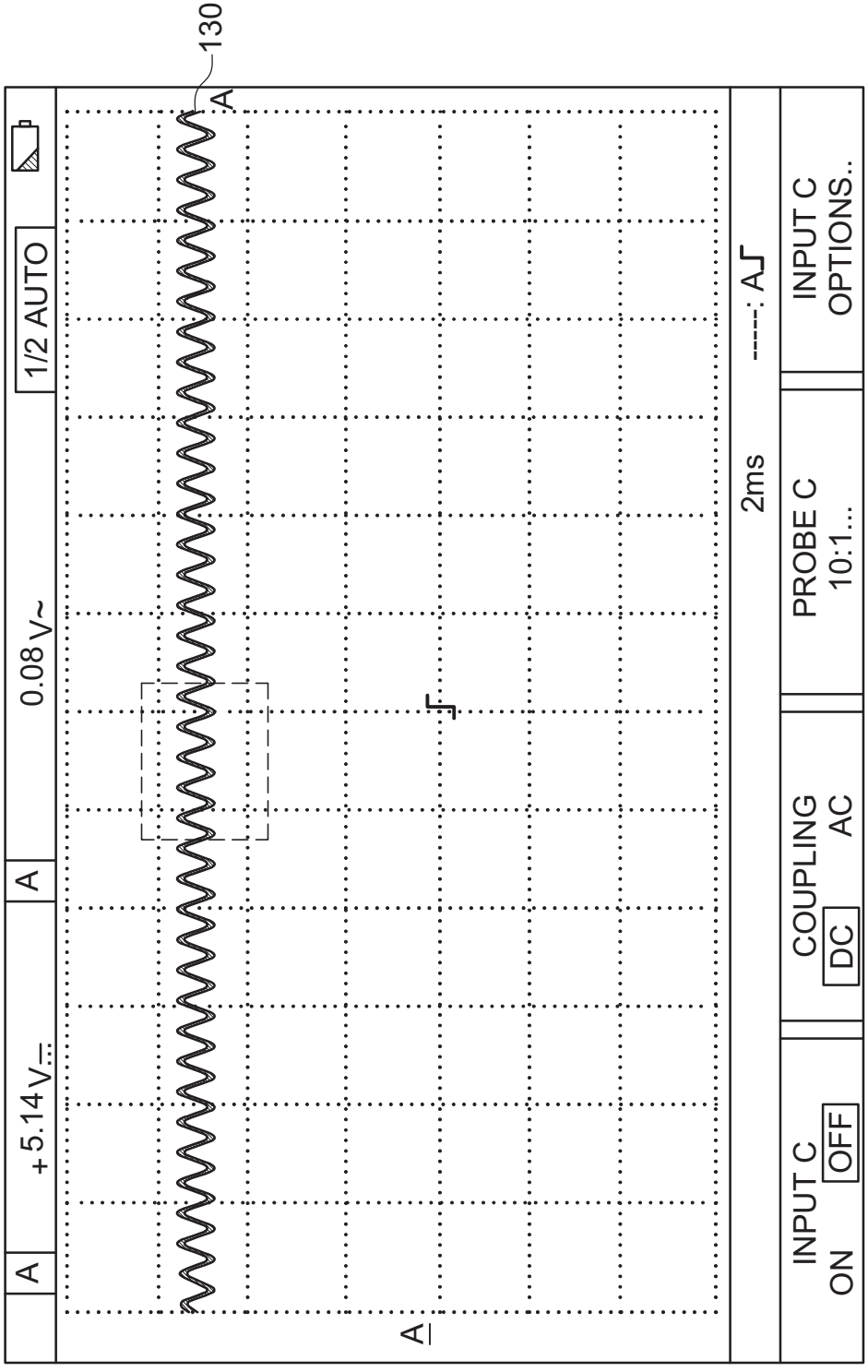

130
A
A
+5.14 V⎓
A
0.08 V~
1/2 AUTO
2ms
----: A
INPUT C
ON OFF
COUPLING
DC AC
PROBE C
10:1...
INPUT C
OPTIONS..

FIG. 1B

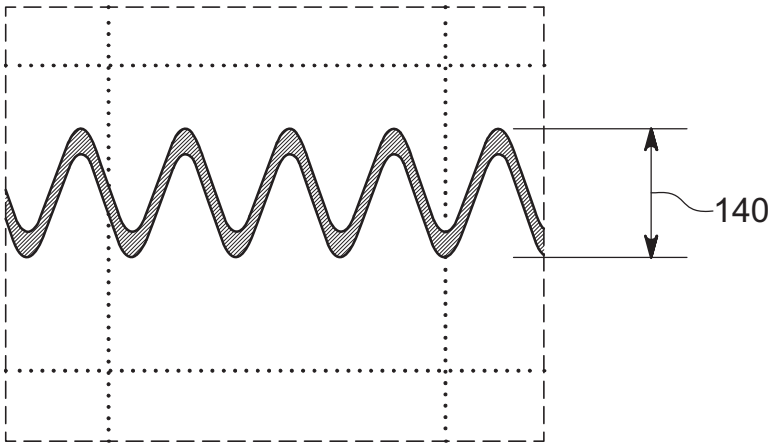


FIG. 1C

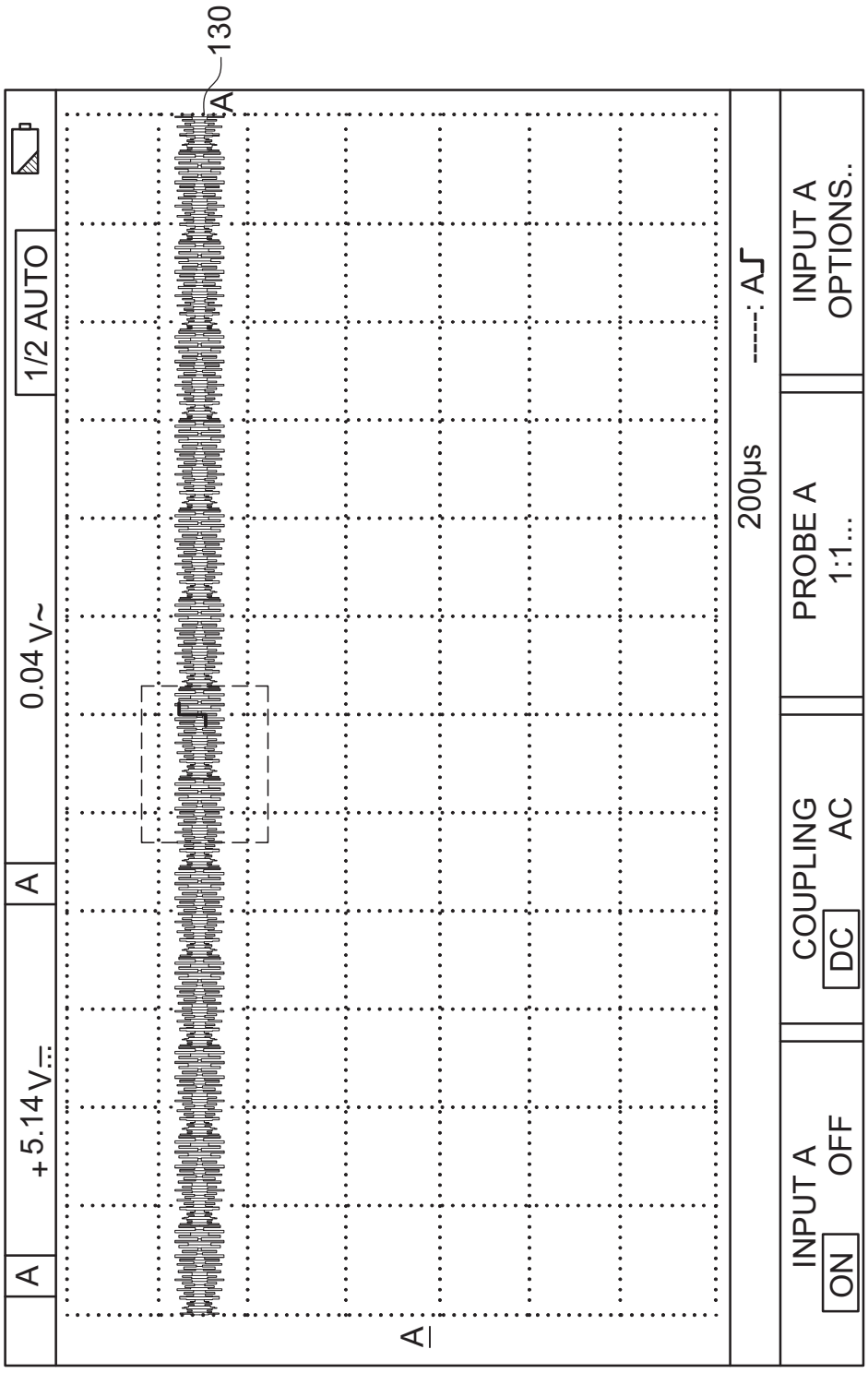

130
A
A
+5.14 V⎓
A
0.04 V~
1/2 AUTO
200µs
----: A⌐
INPUT A
ON OFF
COUPLING
DC AC
PROBE A
1:1...
INPUT A
OPTIONS..

FIG. 1D

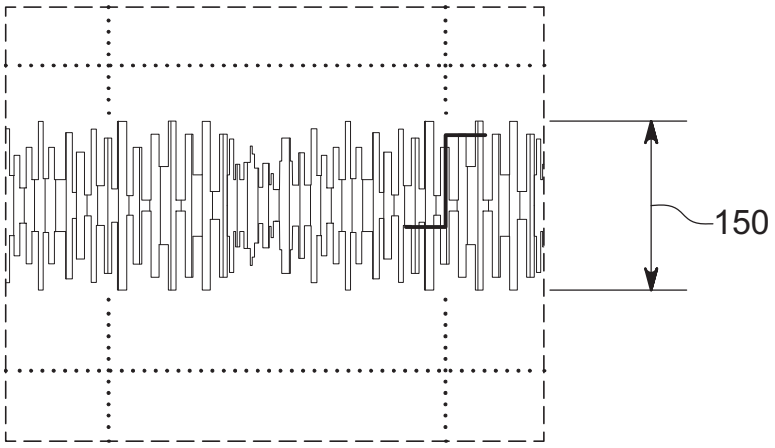


FIG. 1E

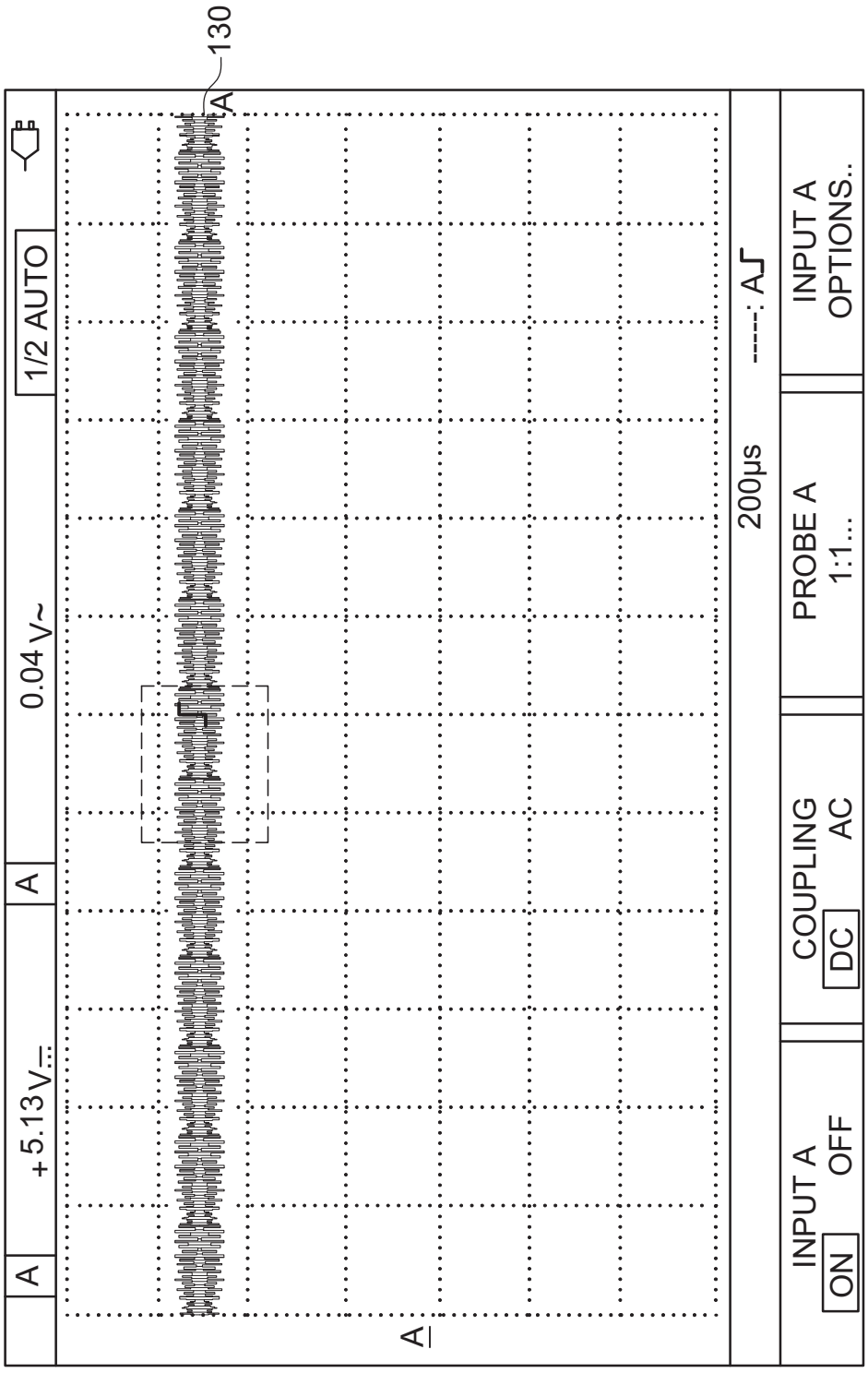

130
A
A
+5.13V⎓
A
0.04V~
1/2 AUTO
200µs
----: AJ
INPUT A
ON OFF
COUPLING
DC AC
PROBE A
1:1...
INPUT A
OPTIONS..

FIG. 1F

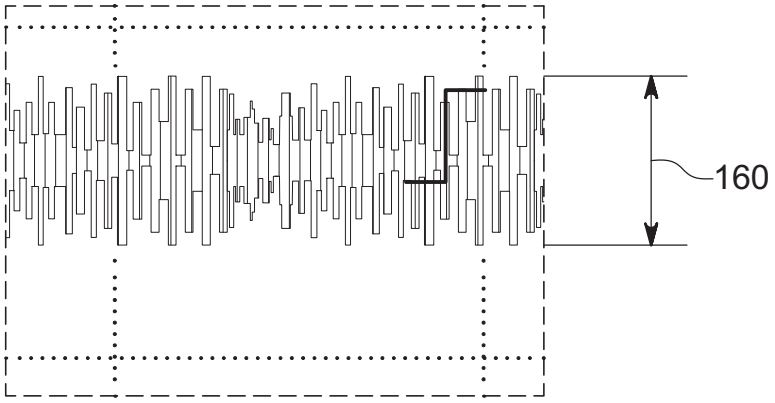


FIG. 1G

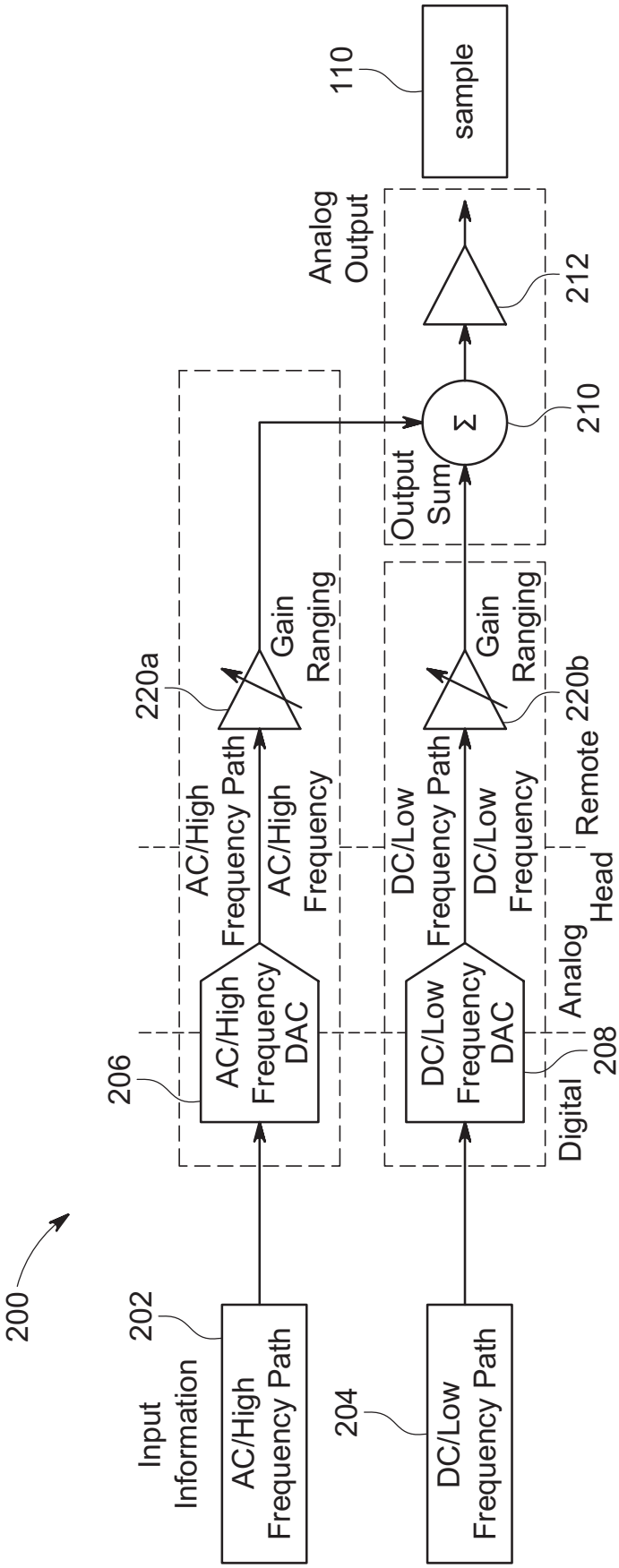

200
202
Input Information
AC/High Frequency Path
204
DC/Low Frequency Path
206
AC/High Frequency DAC
DC/Low Frequency DAC
Digital
Analog
Head
Remote
208
AC/High Frequency Path
AC/High Frequency
DC/Low Frequency Path
DC/Low Frequency
220a
220b
Gain Ranging
Gain Ranging
Output Sum
Σ
210
Analog Output
212
110
sample

FIG. 2

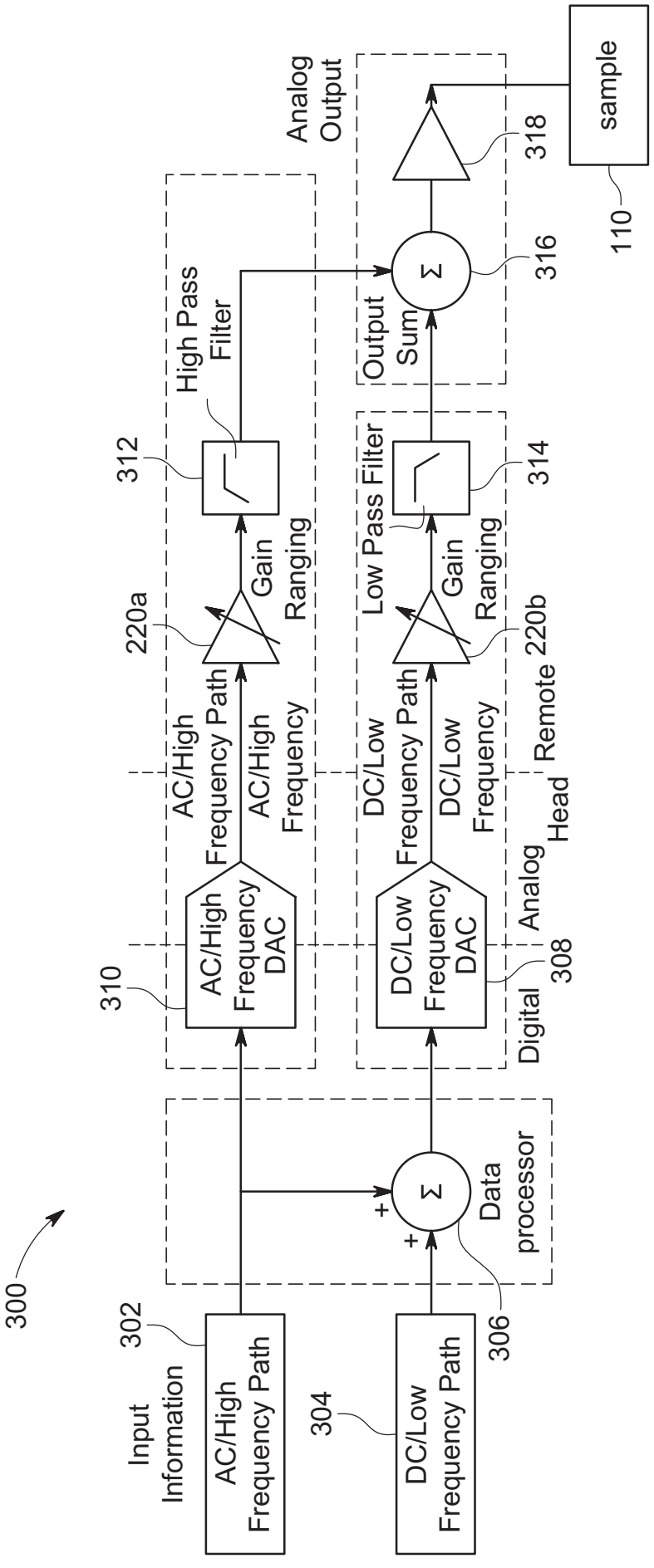

300
Input Information
302
AC/High Frequency Path
304
DC/Low Frequency Path
306
Data processor
+
+
Σ
310
AC/High Frequency DAC
AC/High Frequency Path
AC/High Frequency
220a
Gain Ranging
312
High Pass Filter
DC/Low Frequency DAC
DC/Low Frequency Path
DC/Low Frequency
220b
Gain Ranging
314
Low Pass Filter
Digital
Analog
Remote Head
308
Analog Output
Output Sum
Σ
316
318
sample
110

FIG. 3

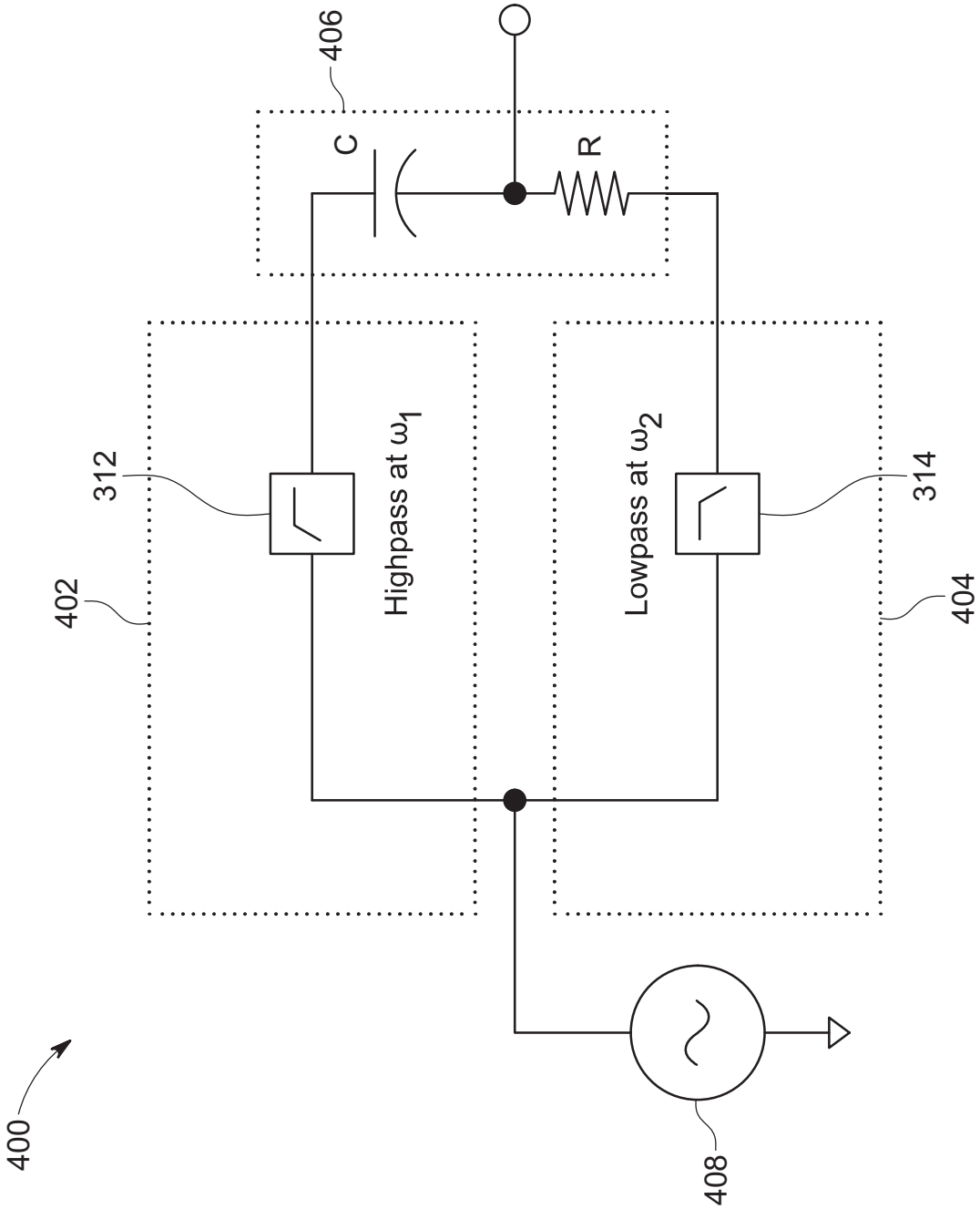

406
C
R
312
Highpass at ω_1
Lowpass at ω_2
314
402
404
400
408

FIG. 4

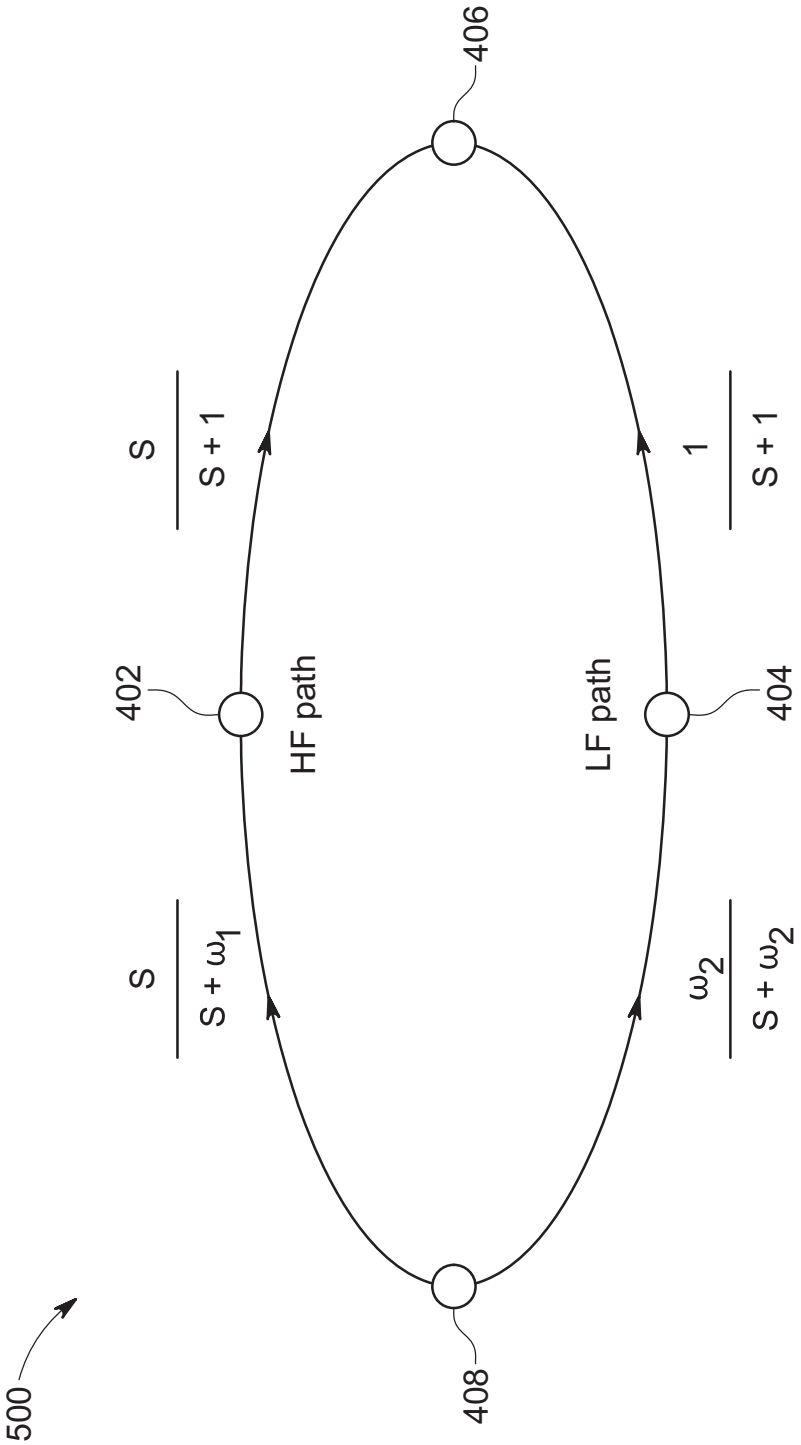


FIG. 5

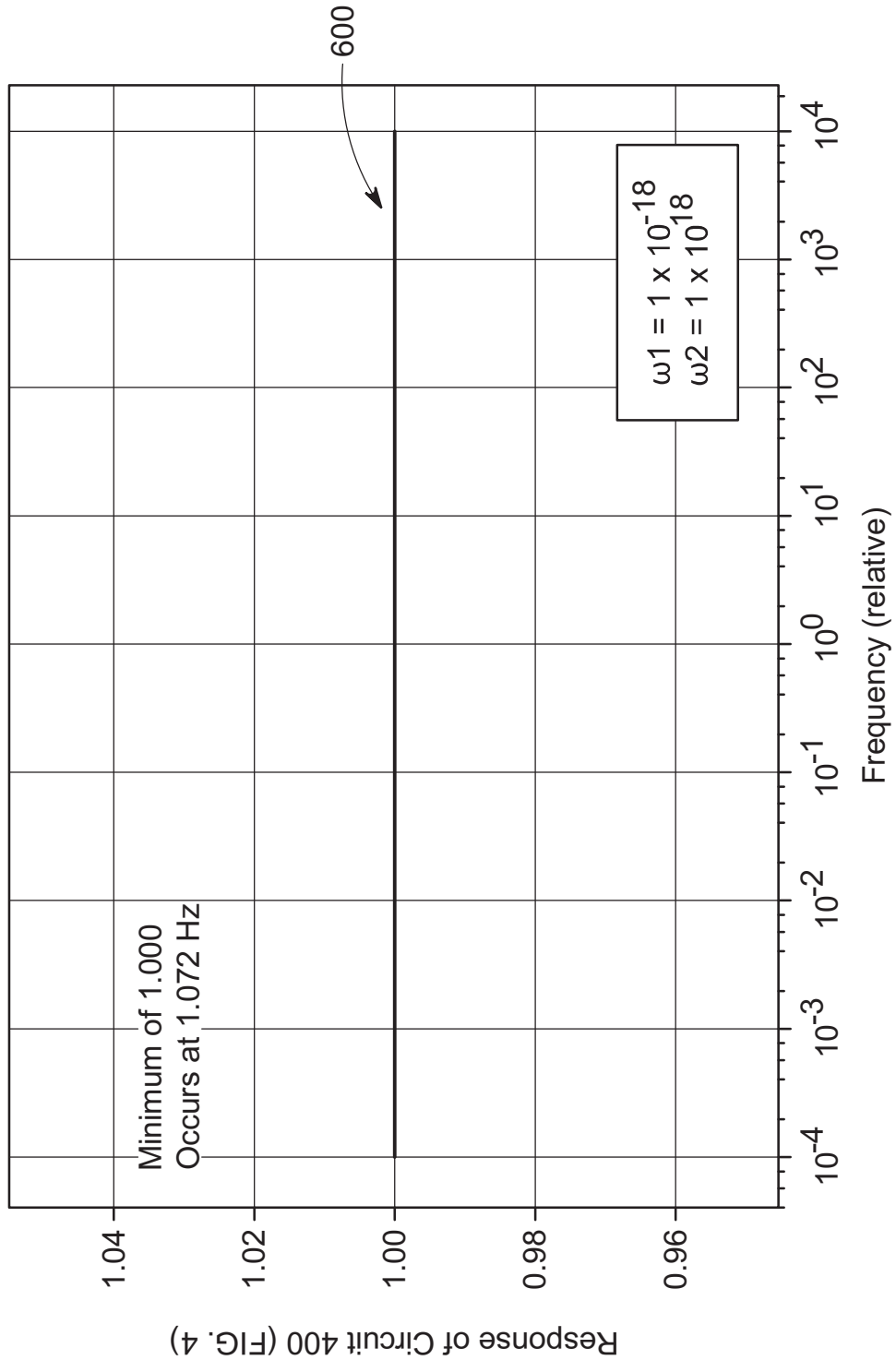

600
Minimum of 1.000
Occurs at 1.072 Hz
ω1 = 1 x 10^-18
ω2 = 1 x 10^18
1.04
1.02
1.00
0.98
0.96
10^-4
10^-3
10^-2
10^-1
10^0
10^1
10^2
10^3
10^4
Frequency (relative)
Response of Circuit 400 (FIG. 4)

FIG. 6

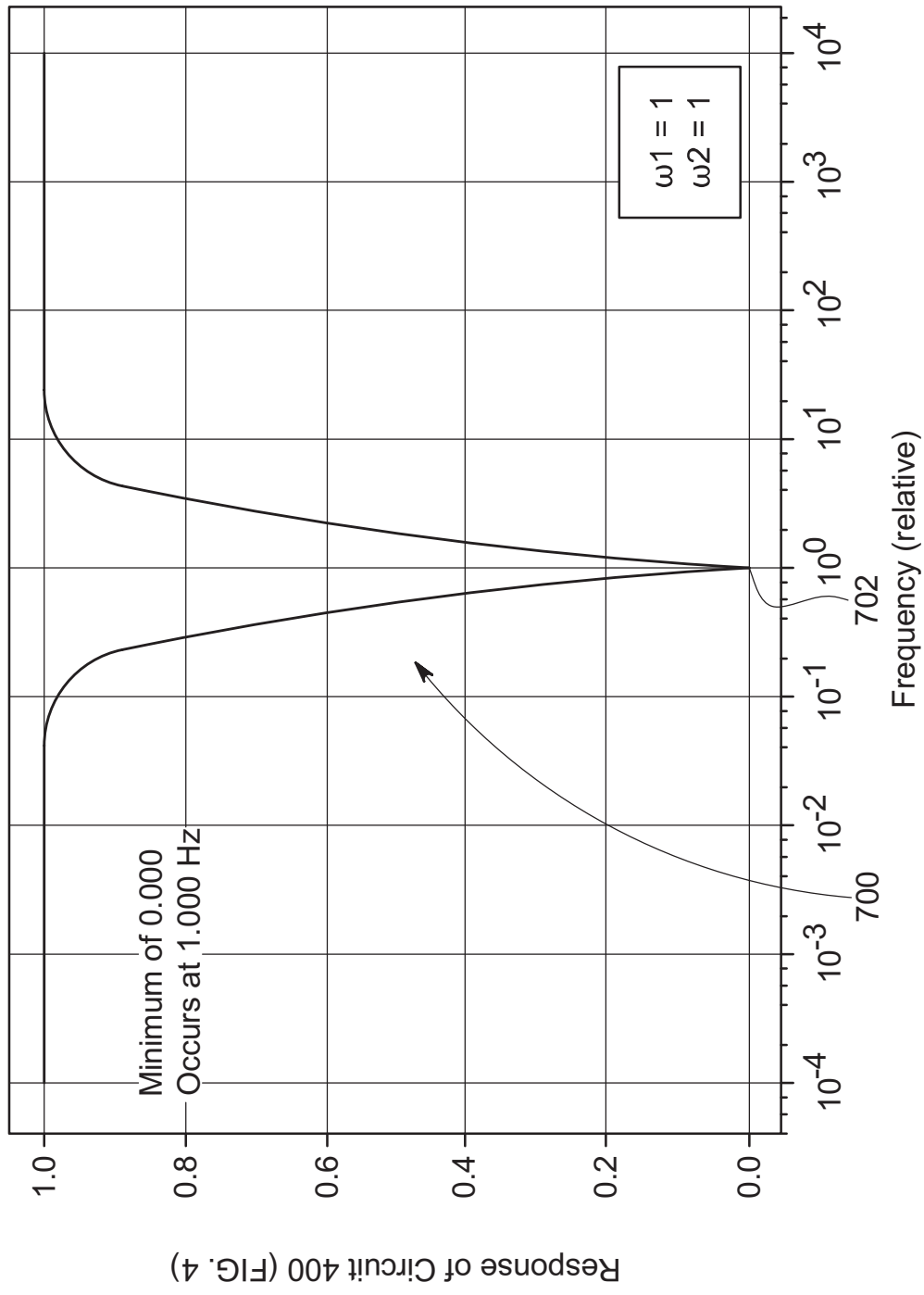

Response of Circuit 400 (FIG. 4)
1.0
0.8
0.6
0.4
0.2
0.0
Minimum of 0.000
Occurs at 1.000 Hz
ω1 = 1
ω2 = 1
700
702
Frequency (relative)
10^-4
10^-3
10^-2
10^-1
10^0
10^1
10^2
10^3
10^4

FIG. 7

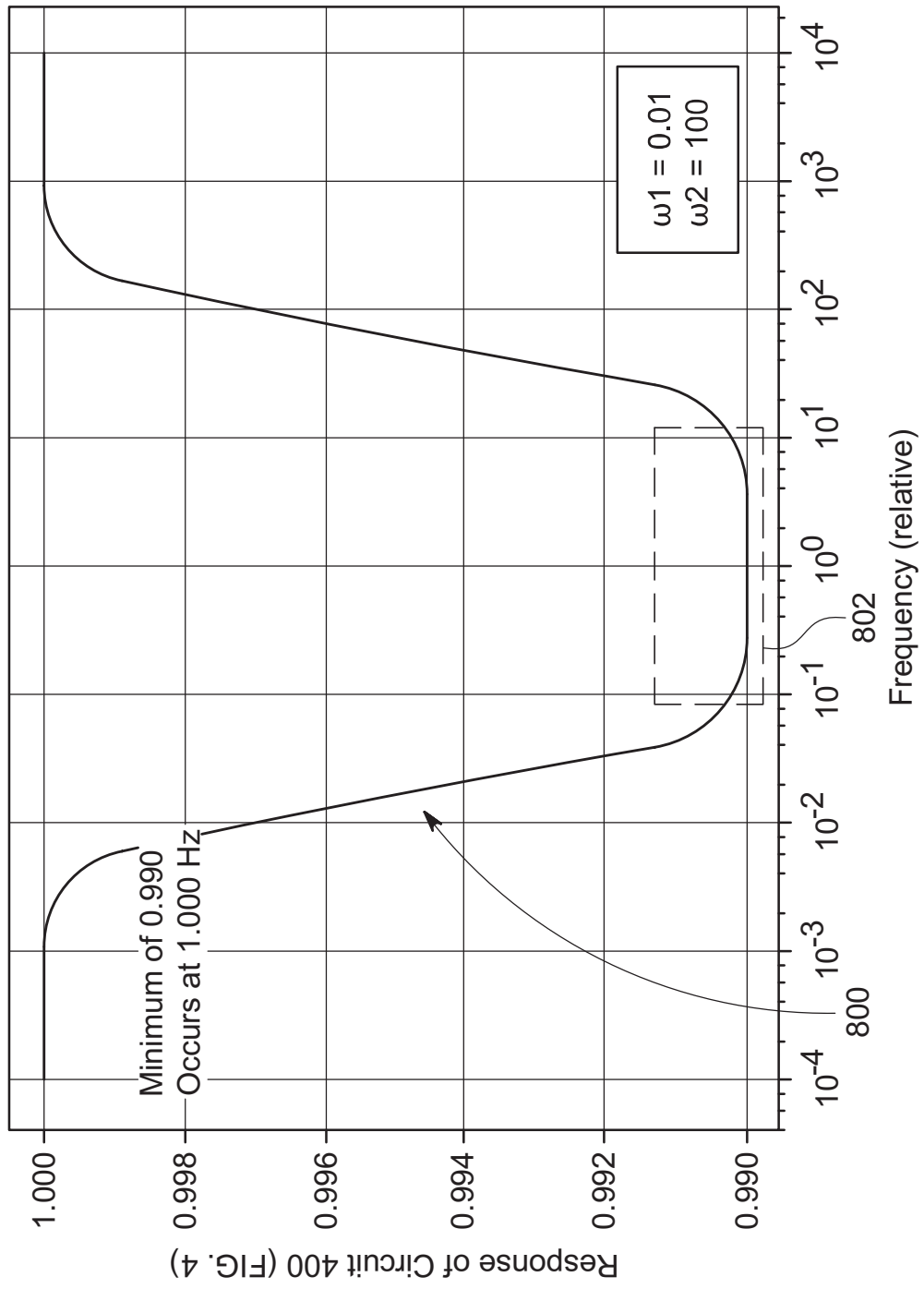

Response of Circuit 400 (FIG. 4)
1.000
0.998
0.996
0.994
0.992
0.990
Minimum of 0.990
Occurs at 1.000 Hz
ω1 = 0.01
ω2 = 100
800
802
10^{-4}
10^{-3}
10^{-2}
10^{-1}
10^{0}
10^{1}
10^{2}
10^{3}
10^{4}
Frequency (relative)

FIG. 8

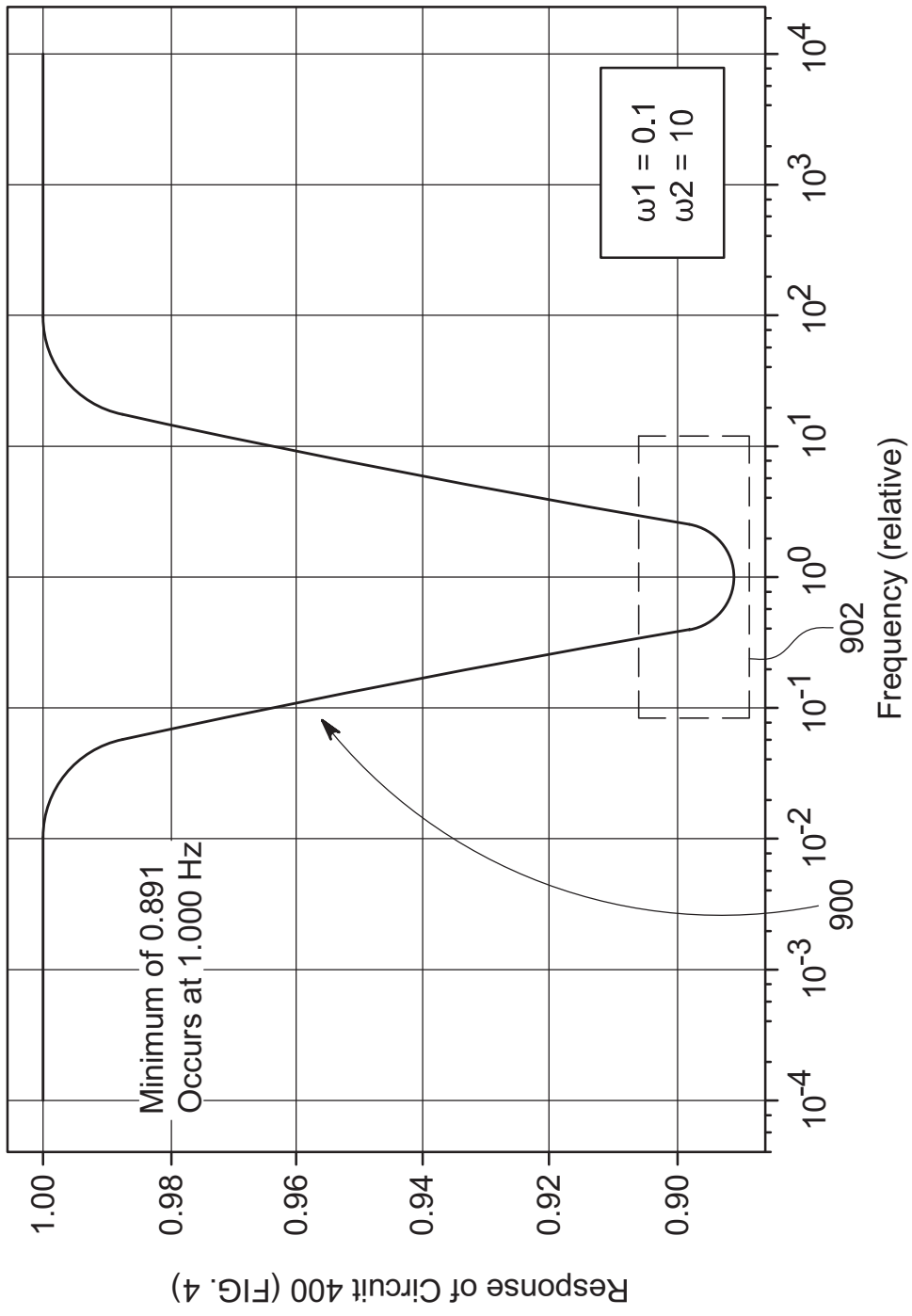

Response of Circuit 400 (FIG. 4)
1.00
0.98
0.96
0.94
0.92
0.90
Minimum of 0.891
Occurs at 1.000 Hz
ω1 = 0.1
ω2 = 10
900
902
Frequency (relative)
10^-4
10^-3
10^-2
10^-1
10^0
10^1
10^2
10^3
10^4

FIG. 9

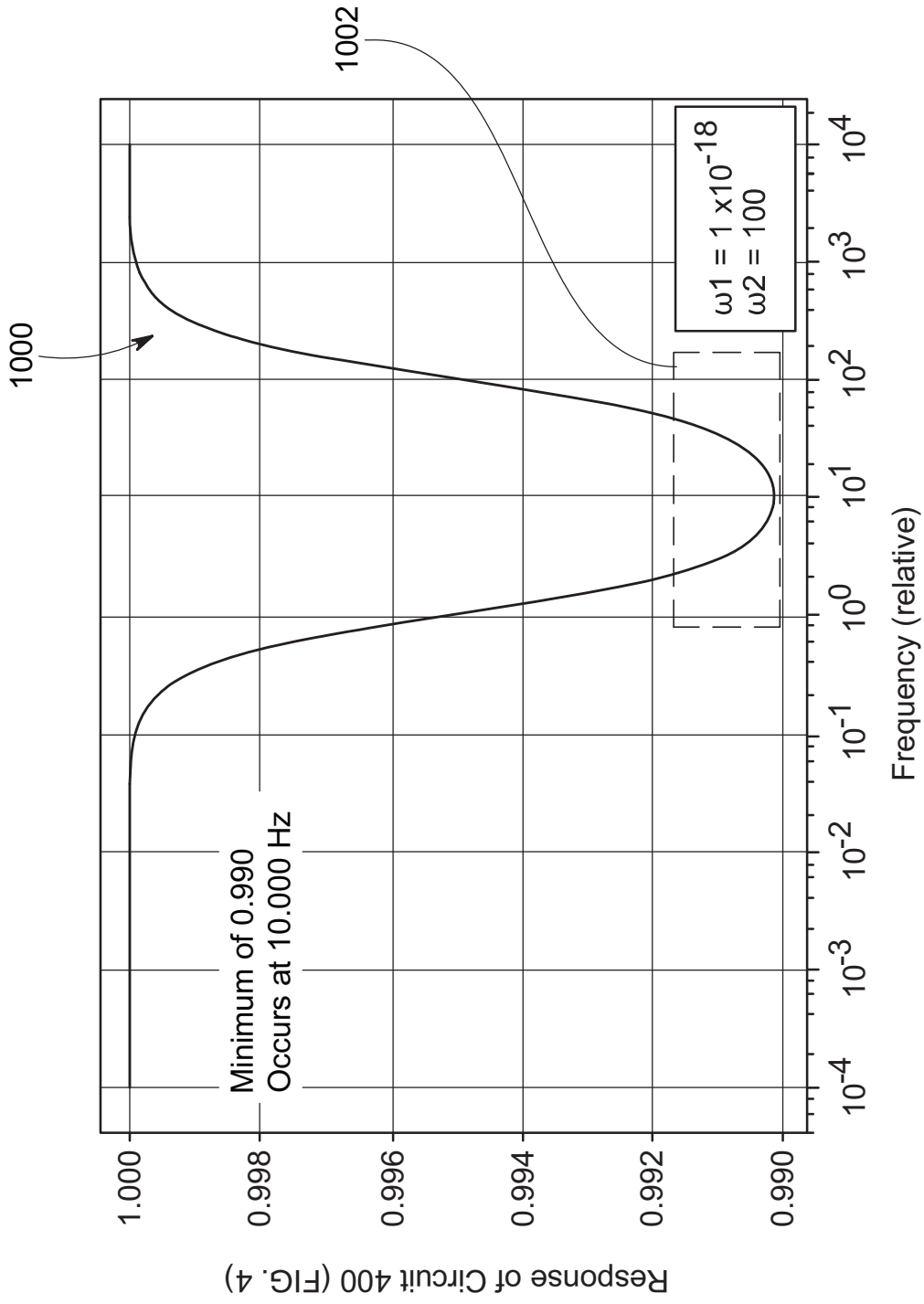

1000
1002
Minimum of 0.990
Occurs at 10.000 Hz
ω1 = 1 x10-18
ω2 = 100
Response of Circuit 400 (FIG. 4)
1.000
0.998
0.996
0.994
0.992
0.990
10-4
10-3
10-2
10-1
100
101
102
103
104
Frequency (relative)

FIG. 10

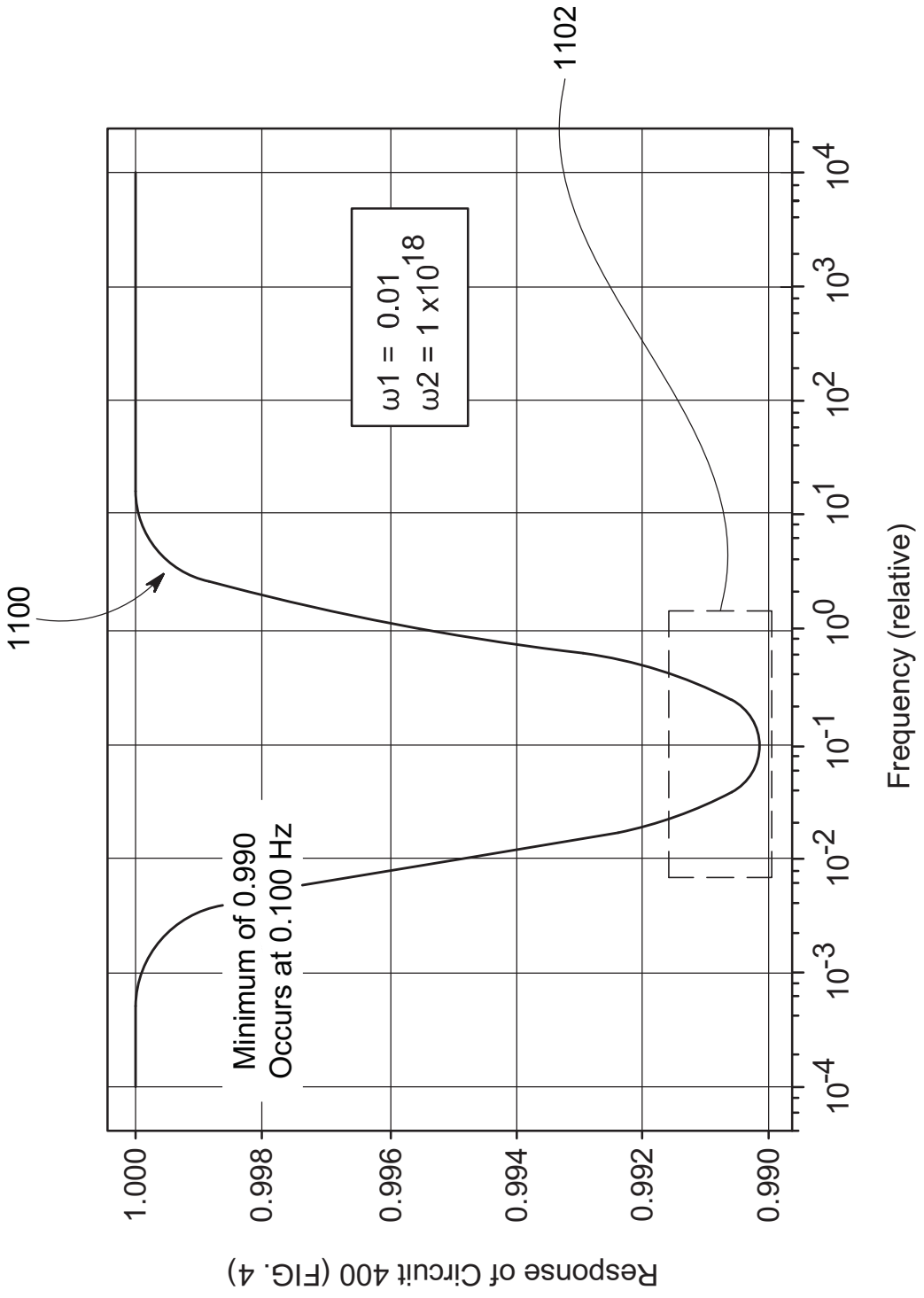

1100
1102
Minimum of 0.990
Occurs at 0.100 Hz
ω1 = 0.01
ω2 = 1 x10^18
Response of Circuit 400 (FIG. 4)
1.000
0.998
0.996
0.994
0.992
0.990
10^-4
10^-3
10^-2
10^-1
10^0
10^1
10^2
10^3
10^4
Frequency (relative)

FIG. 11

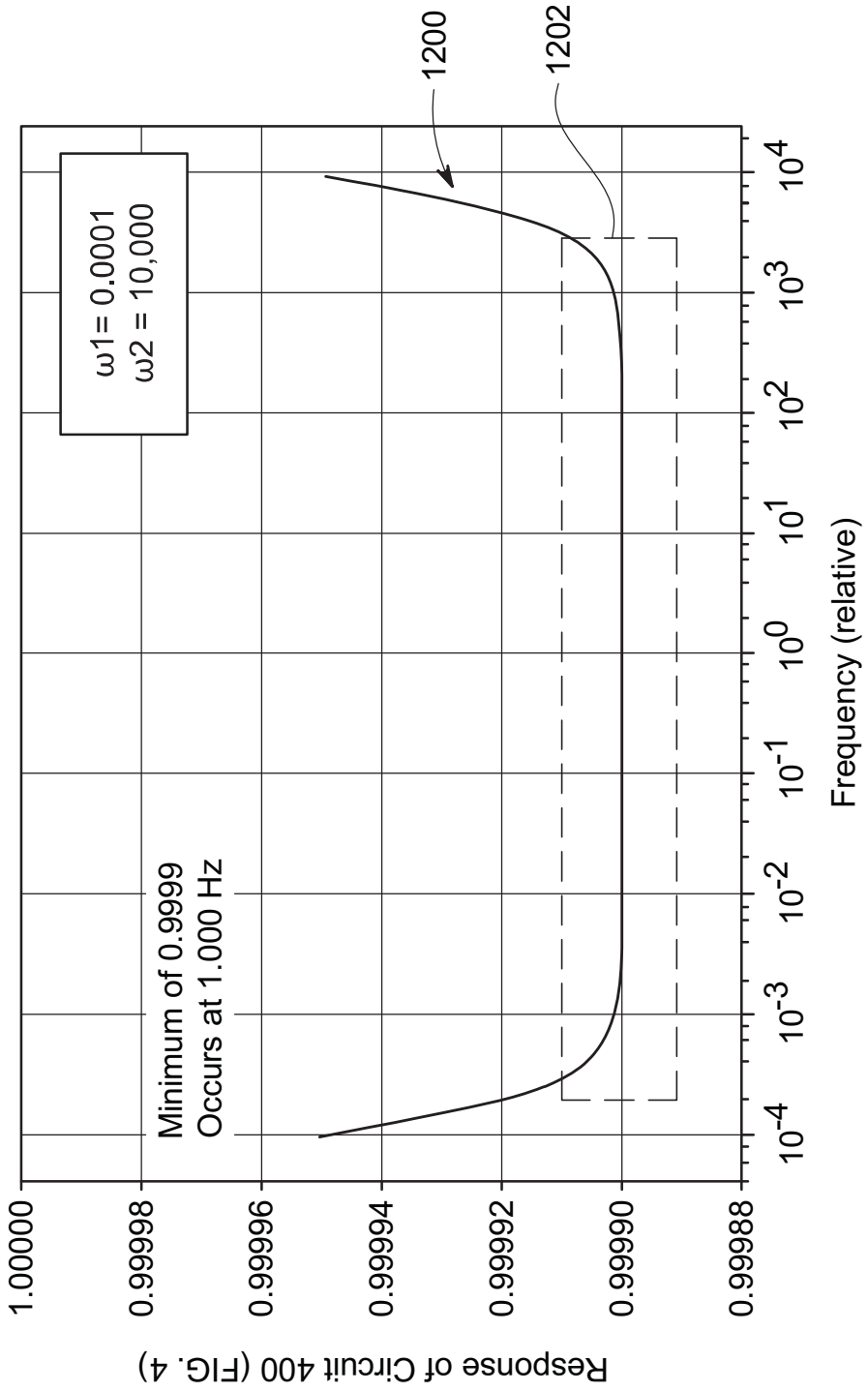

1200
1202
ω1= 0.0001
ω2 = 10,000
Minimum of 0.9999
Occurs at 1.000 Hz
1.00000
0.99998
0.99996
0.99994
0.99992
0.99990
0.99988
Response of Circuit 400 (FIG. 4)
10-4
10-3
10-2
10-1
100
101
102
103
104
Frequency (relative)

FIG. 12

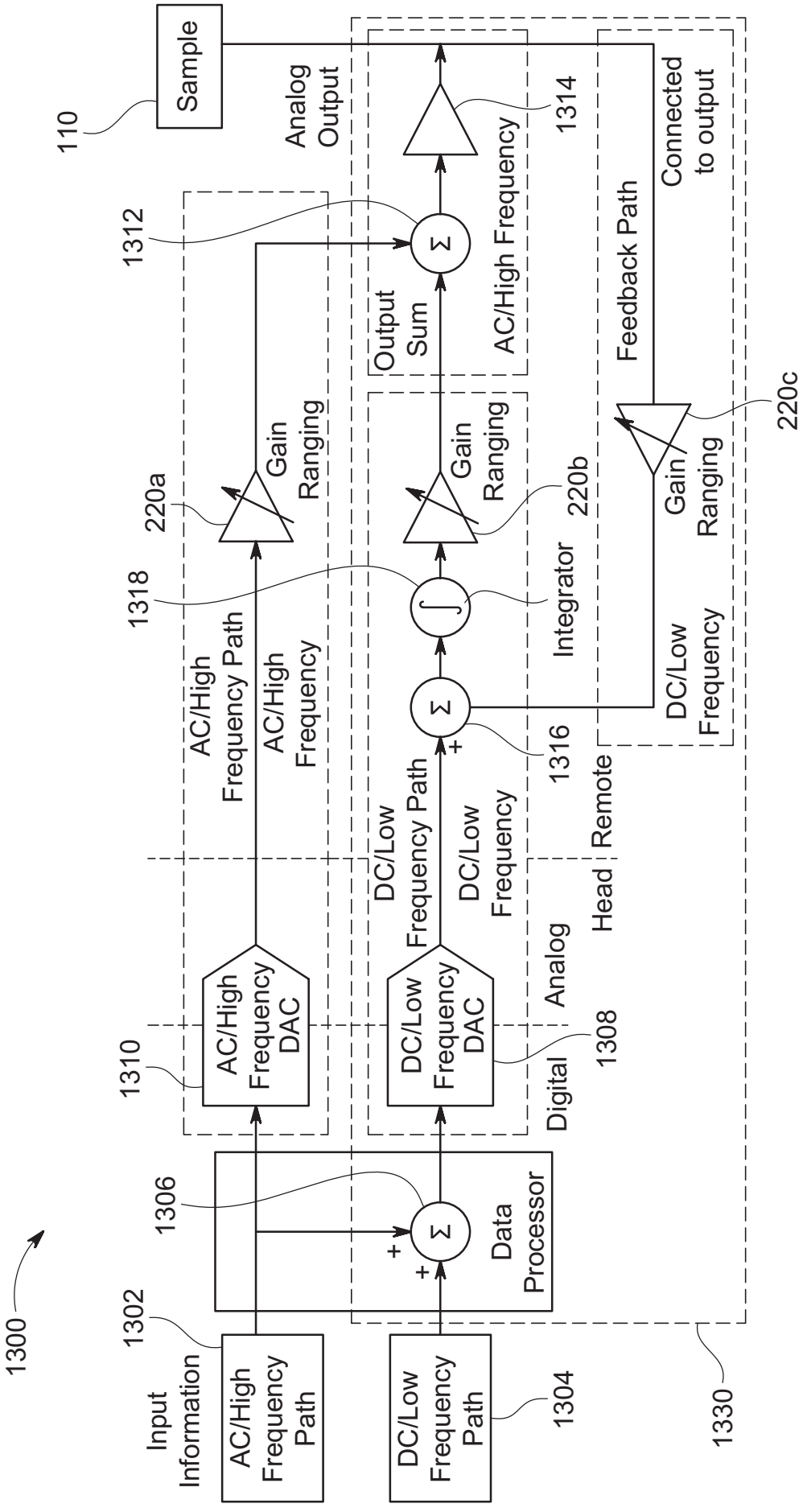

1300
1302
Input Information
AC/High Frequency Path
DC/Low Frequency Path
1304
1306
Data Processor
1308
Digital
Analog
Head
Remote
1310
AC/High Frequency DAC
DC/Low Frequency DAC
AC/High Frequency Path
AC/High Frequency
DC/Low Frequency Path
DC/Low Frequency
1312
1314
AC/High Frequency
Output Sum
1316
1318
Integrator
220a
220b
220c
Gain Ranging
Feedback Path
Connected to output
DC/Low Frequency
1330
110
Sample
Analog Output

FIG. 13

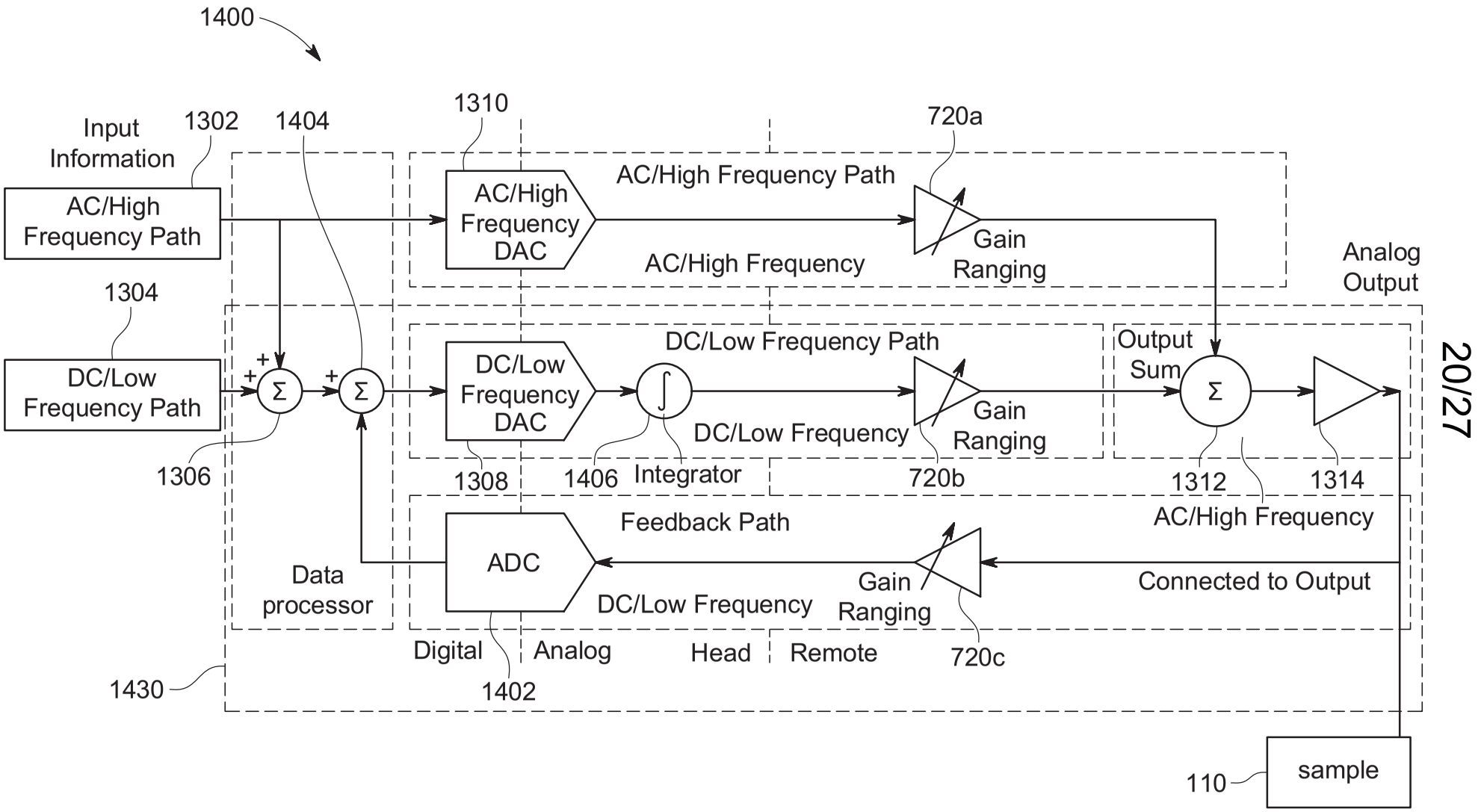

1400
Input Information
1302
1404
1310
720a
AC/High Frequency Path
AC/High Frequency DAC
AC/High Frequency Path
AC/High Frequency
Gain Ranging
Analog Output
1304
DC/Low Frequency Path
DC/Low Frequency Path
DC/Low Frequency DAC
Output Sum
Σ
Integrator
DC/Low Frequency
Gain Ranging
1306
1308
1406
720b
1312
1314
AC/High Frequency
Feedback Path
ADC
Data processor
Gain Ranging
Connected to Output
DC/Low Frequency
Digital
Analog
Head
Remote
720c
1430
1402
110
sample
20/27

FIG. 14

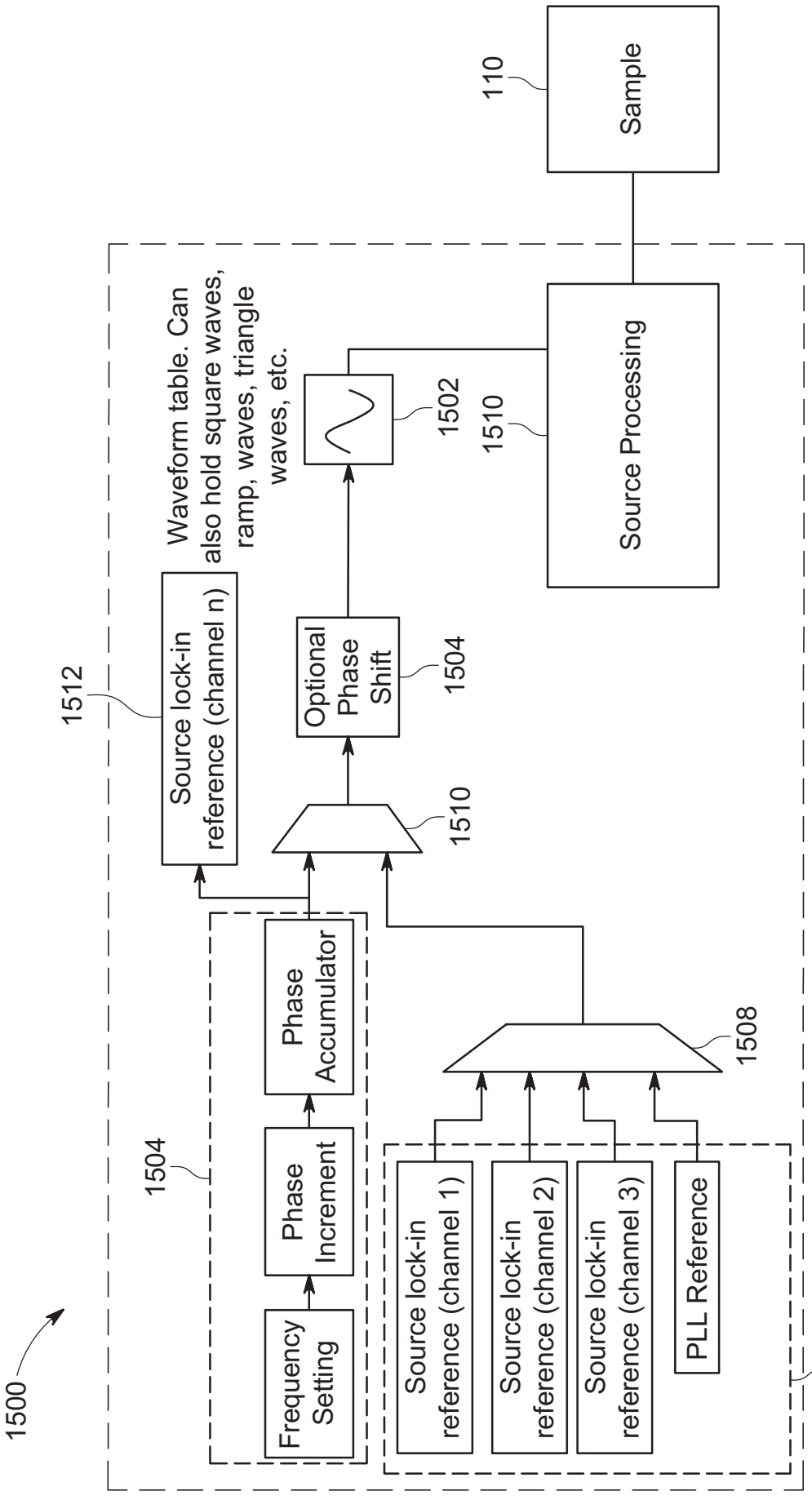

1500
Frequency Setting
Phase Increment
Phase Accumulator
1504
Source lock-in reference (channel 1)
Source lock-in reference (channel 2)
Source lock-in reference (channel 3)
PLL Reference
1506
1508
1510
Optional Phase Shift
1504
Source lock-in reference (channel n)
1512
Waveform table. Can also hold square waves, ramp, waves, triangle waves, etc.
1502
1510
Source Processing
110
Sample

FIG. 15

1600

Position	Output
0	0.000
1	0.500
2	0.866
3	1.000
4	0.866
5	0.500
6	0.000
7	-0.500
8	-8.666
9	-1.000
10	-0.866
11	-0.500

FIG. 16

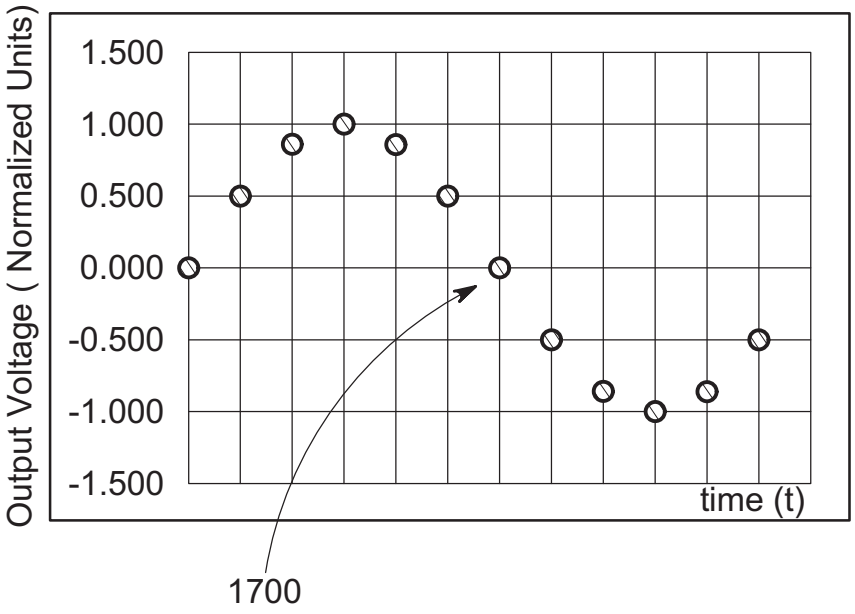


FIG. 17

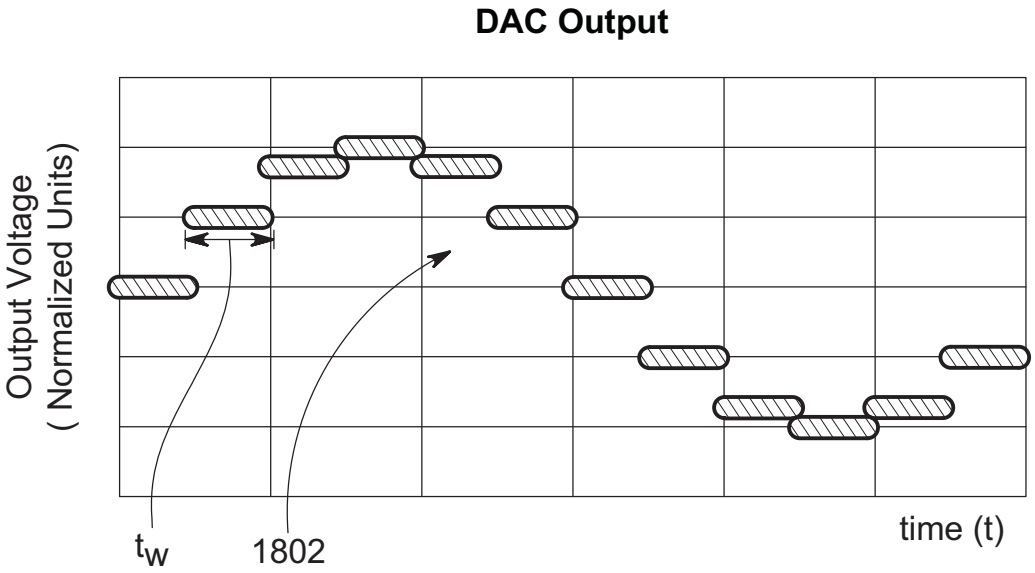


FIG. 18A

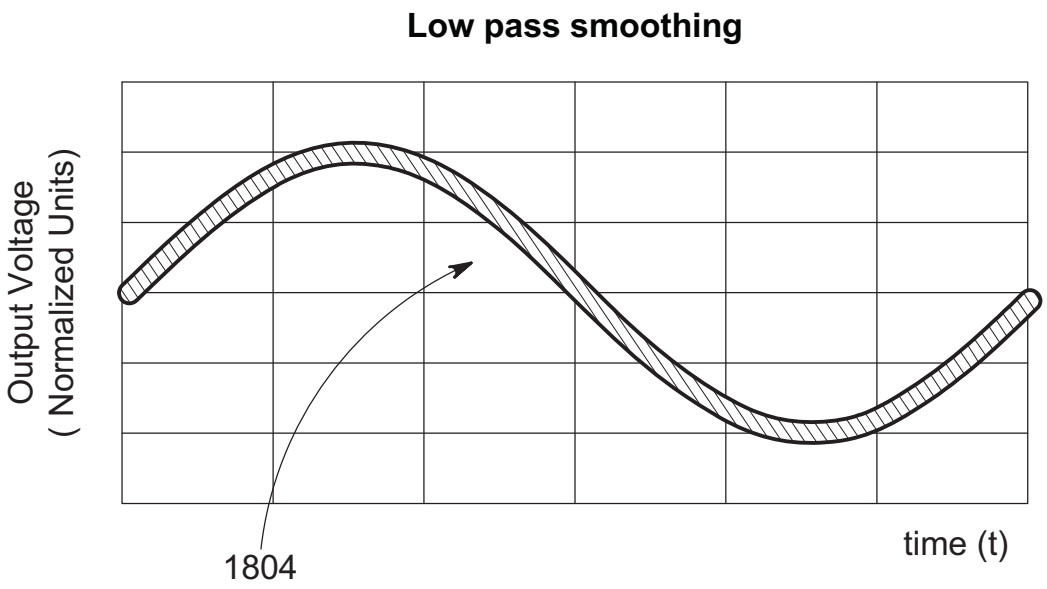

Low pass smoothing
Output Voltage
(Normalized Units)
1804
time (t)

FIG. 18B

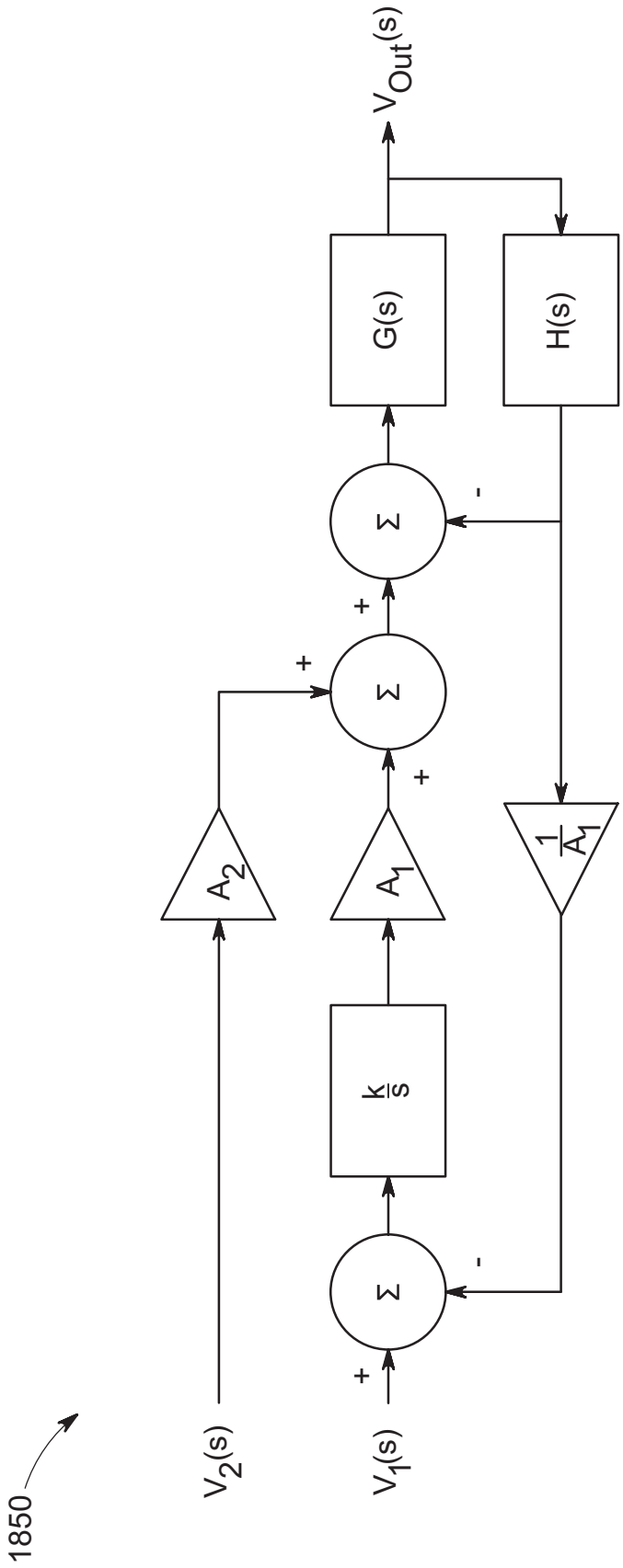


FIG. 18C

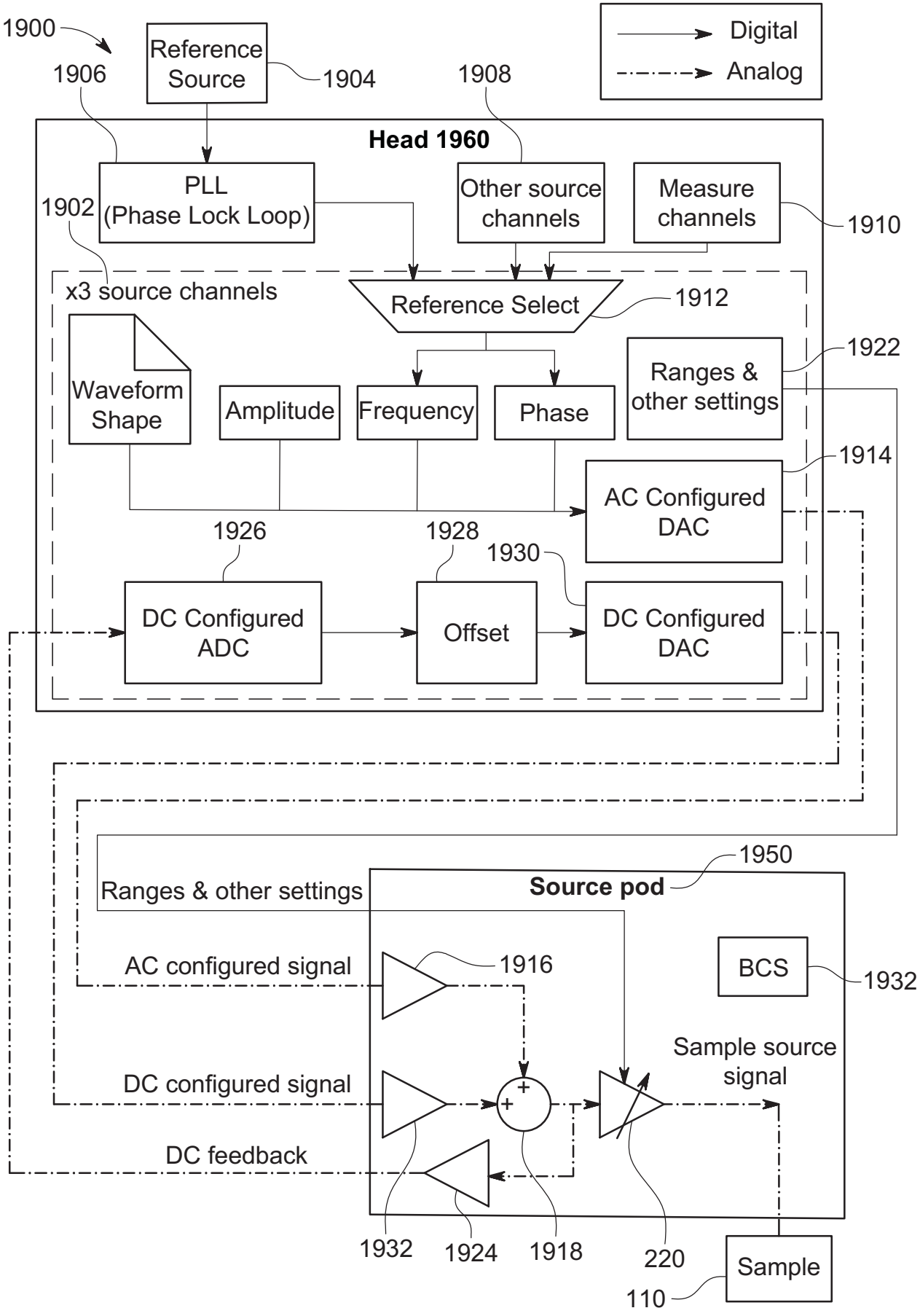

1900
Reference Source
1904
1906
1908
Digital
Analog
Head 1960
PLL (Phase Lock Loop)
1902
Other source channels
Measure channels
1910
x3 source channels
Reference Select
1912
Waveform Shape
Amplitude
Frequency
Phase
Ranges & other settings
1922
1914
AC Configured DAC
1926
1928
1930
DC Configured ADC
Offset
DC Configured DAC
1950
Ranges & other settings
Source pod
AC configured signal
1916
BCS
1932
Sample source signal
DC configured signal
DC feedback
1932
1924
1918
220
Sample
110

FIG. 19

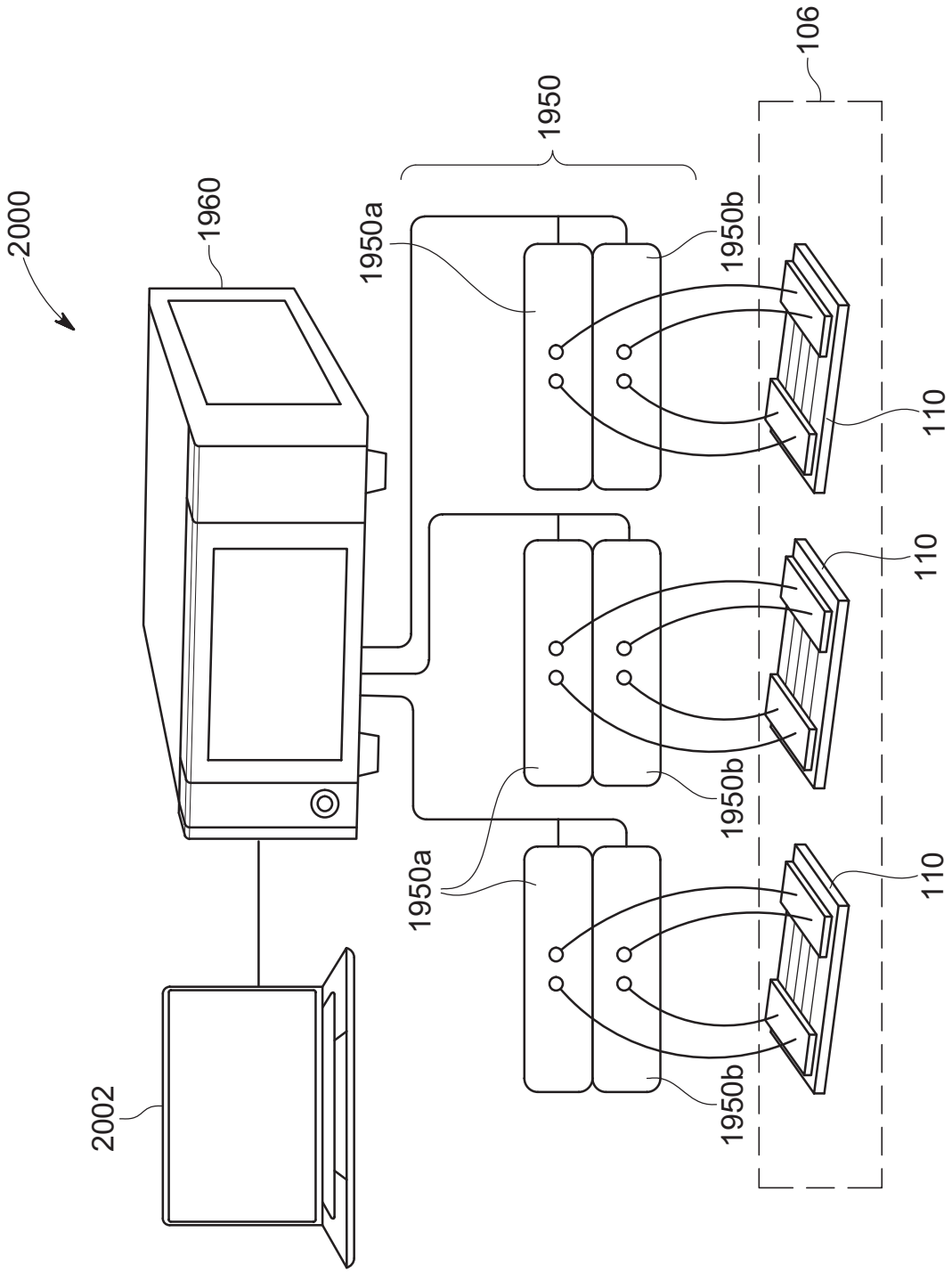

2000
1960
1950
1950a
1950b
106
110
110
110
1950a
1950b
1950b
2002

FIG. 20