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LAYOUT FOR CMOS IMAGE SENSOR

Field of the Invention

[0001]. The present invention relates to a fabrication of a CMOS image sensor (CIS) and, more specifically, to a novel layout design for CIS in which metal lines are provided to connect a photodiode with an active area comprising three transistors.

Background of the Invention

[0002]. Since a CMOS image sensor (CIS) has a low operation voltage, low power consumption and high operation efficiency, it is broadly applied in the current semiconductor industry such as videophones, digital cameras, mobile phones and aerospace aspects. Particularly, the CIS can be operated in random access based on demands and the fabricating process thereof is compatible with the logic process in the semiconductor fabrication. Therefore, it is even more important.

[0003]. Please refer to FIG. 1, which shows a typical CIS design. The CIS is composed by a photodiode D and three MOS transistors M1, M2 and M3, wherein the photodiode D is connected to the element M1 used as a switch, and when the element M1 is activated, a reverse bias

required for operation of the photodiode D is provided to the photodiode D from the power source V_{DD}, as shown by the signal A in voltage-timing diagram in FIG. 2. During the reverse bias period, the photodiode D is illuminated. Under the electric field of the reverse bias period, the electron and hole pairs of unequal extents generated according to irradiation intensity result in reducing a portion of the reverse bias. When the reverse bias period is ended, the irradiation ceases (in which the transistor M1 is turned off). At this time, if a read signal voltage is applied to the gate of the transistor M3 to active it, a light signal can thus be read. The light signal (voltage) is outputted from the photodiode D to the transistor M2 and is amplified. The amplified signal is then outputted to the source of the transistor M3.

[0004]. Referring to FIG. 3, which is a top view of a single pixel layout for a conventional CIS, a pixel region 102 is formed on a P-type semiconductor substrate 100 and the pixel region 102 includes a photodiode area 104 and an active area 105 separated from the photodiode area 104 by an insulation area 110. An N-type well 106 is formed in the photodiode area 104. When a positive voltage is exerted to the N-type well 106 and a negative voltage is applied to the other P-type substrate in the photodiode area 104, a depletion region 108 of P/N junction is formed. The three transistors 112a, 112b, 112c in the active area 105 respectively, corresponding to M1, M2, M3 in FIG. 1, are used to control the operation of the photodiode D.

[0005]. After the photodiode area 104 is irradiated with a visible light in a range between 390 nm and 770 nm, a response is resulted and generates different voltages whose magnitudes are based on the light intensity detecting in the pixel region 102 of the conventional CIS. Therefore, in order for the photodiode area 104 to have a good response to light, the pixel region 102 must have a laminar structure which is pervious to light thereon.

[0006]. However, after light irradiation, the source and drain 106a of the transistors in the active area 105 also respond to the light intensity, as the photodiode area 104 does, to result the dark current defect. Nevertheless, in the SPICE model of the characteristics of the photodiode, it is generally presumed that the transistors in the active area 105 are in a dark environment. But the active area 105 and the photodiode area 104 are actually operated in a bright environment, it causes that the characteristics of the transistors do not match and leads to distortion.

[0007]. The metallization process of the peripheral circuits has to be performed to have three metal layers, and the metallization process in the pixel region 102 is usually simpler than in the peripheral region; for instance, the pixel region 102 has only two metal layers. Therefore, the difference of patterns is great and it requires longer etching time in the peripheral region. Once the etching time is too long, the metal layer around the peripheral region

will be over-etched. The metal lines with narrower widths are liable to be over-etched and then the process window becomes narrow. This is a serious defect in process.

[0008]. In view of the above-mentioned, a method is provided in the present invention to solve the aforesaid problems such as dark current etc.

Summary of the Invention

[0009]. The major objective of the present invention is to provide a fabrication of a CMOS image sensor (CIS) so as to reduce the defects of the CIS.

[0010]. A layout of a CMOS image sensor is disclosed in this invention, wherein said layout comprises a photodiode area which is formed on a P-type semiconductor substrate; an active area which is formed on the semiconductor substrate and is separated from the photodiode area by an insulating area and comprises a plurality of transistors for driving the photodiode; and a shield which is formed on top of the active area and protects the active area from irradiation.

[0011]. For the photodiode area, the P-type semiconductor substrate is used as a positive electrode and a N-type well in the P-type semiconductor substrate

is used as a negative electrode. For the photodiode area, a N-type well is used as a negative electrode and a P-type diffusion area in the N-type well is used as a positive electrode. Moreover, the shield can be made of metal.

Brief Description of the Drawings

[0012]. The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

[0013]. FIG. 1 shows a typical CIS design in the prior art;

[0014]. FIG. 2 is a wave diagram of the CIS in operation;

[0015]. FIG. 3 is a top view of a single pixel layout for a conventional CIS;

[0016]. FIG. 4 is a top view of a CIS;

[0017]. FIGs. 5 and 6 are respectively a top view of a CIS pixel layout of this invention;

[0018]. FIG. 7 is a cross-sectional diagram of the CIS layout in FIG. 6 along a aa' line; and

[0019]. FIG. 8 is a cross-sectional diagram of the CIS layout in FIG. 6 along a bb' line.

Detailed Description of the Preferred Embodiments

[0020]. This invention discloses an improved layout design for CIS. When the metal layers of the peripheral circuits are formed, a shielding metal for the active area is simultaneously fabricated, thereby to improve the defects of dark current and noise, etc. resulted from the irradiation of the active area in the conventional pixels.

[0021]. Please refer to FIG. 4, which is a top view of a CMOS image sensor (CIS). The CIS includes an array of a plurality of pixels102 and a region 200 of peripheral circuits. To take example by the four pixels 102 around the peripheral circuits, the four pixels 102 are magnified as shown in FIG. 5, which is a top view of a CIS pixel layout of this invention. Firstly, a P-type semiconductor substrate 100 is provided. In one example, the P-type semiconductor substrate 100 has a P-type dopant such as boron. Then, a pixel region 102 is fabricated on the P-type semiconductor substrate 100, wherein before a photodiode area 104 and an active area 105 are formed, an insulation area 110 of insulation structures such as FOX and STI etc.

must be first formed on the top surface of the P-type semiconductor substrate 100 in order to separate the photodiode area 104 from the active area 105.

[0022]. Subsequently, the photodiode area 104 is fabricated in the pixel region 102. A photoresist pattern is formed on the P-type semiconductor substrate 100 to define a N-type well area 106 and a first ion implantation is then performed in the photodiode area 104 to form the N-type well area 106 therein. In one example, the N-type well area 106 is implanted with a N-type dopant such as phosphorous and arsenic, etc. After completion of the N-type well area 106 fabrication, the photoresist pattern is removed.

[0023]. Afterwards, gate structures of the transistors 112a, 112b, 112c of the active area 105 are fabricated in the pixel region 102, and gate structures of transistors in the region 200 of peripheral circuits are also fabricated. In one example, a gate oxide layer of the three transistors 112a, 112b, 112c of the active area 105 is first formed, and a polysilicon layer is then formed to cover the gate oxide layer, and a photoresist pattern is subsequently defined on the polysilicon layer.

[0024]. After the polysilicon layer and the gate oxide layer are etched, the photoresist is removed to form the gate structure. Spacers

are then formed on the sidewall of the gate structure. Afterwards, a second ion implantation is performed in the active area 105. The gate structure having the spacers is used as a mask for the ion implant, and the N^+ ions are implanted to form the sources and drains of the transistors 112a, 112b, 112c, i.e. the N^+ doped area 106a of the active area 105. An annealing procedure is subsequently performed.

[0025]. After completion of the main gate structures of the transistors 112a, 112b, 112c in the active area 105 and the transistors in the region of peripheral circuits, a dielectric layer 114 is formed to cover all of the areas and is planarized. Subsequently, a photolithography and etching procedures are performed to form contact windows for the elements in the region of peripheral circuits as well as for the sources of the transistors 112a, 112b, 112c in the active area 105 of the pixel region 102, the gates of the transistors 112a, 112b, 112c in the active area 105, the N^+ doped area 106a of the active area 105 and the photodiode area 104. Then, a metallization process is performed to form a metal layer filling the contact windows up and to form a shielding metal 116 on the top surface of the dielectric layer 114 in the active area 105 so as to avoid irradiation of the active area 105, as shown in FIG. 6. A chemical mechanical polishing (CMP) procedure is performed to remove excess metal on the top surface of the dielectric layer 114.

[0026]. Referring to FIG. 7, which is a cross-sectional diagram of the CIS layout in FIG. 6 along an aa' line, the insulating area 110 and the dielectric layer 114 are formed on the P-type semiconductor substrate 100, wherein the insulating area 110 is adjacent to and around the periphery of the photodiode area 104 and separates the photodiode area 104 from the active area 105. Moreover, the shielding metal 116 is formed above the N^+ doped area 106a of the active area 105. Similarly, FIG. 8 is a cross-sectional diagram of the CIS layout in FIG. 6 along a bb' line, in which the shielding metal 116 is formed above the transistors 112b, 112c of the active area 105.

[0027]. The shielding metal 116 is applied with a specific voltage or is grounded so as to prevent the shielding metal 116 is from floating which leads to an unfavorable effect of charge accumulation.

[0028]. The advantages of this invention are mentioned as follows:

(a) the metal shielding fabrication process is quite simple, and it merely modifies the design of mask patterns to simultaneously define the shielding metals in the active area during the metallization process for the typical peripheral circuits so as to avoid the defects of dark current, etc. after the irradiation of the active area and

to be consistent in the SPICE model in a non-irradiation environment;

(b) the load effect can be improved and the too long etching time is avoided in the metallization process, and thus the defects that the surrounding metal layer is over-etched, the metal lines with narrower widths are liable to be etched off and the process window becomes narrow in the prior art are solved; and

(c) the process cost is low and the operation performances and effects of the elements are enhanced and the conventional defects are greatly reduced.

[0029]. As is understood by a person skilled in the art, the foregoing preferred embodiment of the present invention is illustrated of the present invention rather than limiting of the present invention. It is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims, the scope of which should be accorded the broadest interpretation so as to encompass all such modifications and similar structure.

Patent Claims

What is claimed:

1. A layout of a CMOS image sensor, said layout comprising:

a photodiode area, formed on a P-type semiconductor substrate;

an active area, formed on said semiconductor substrate, separated from said photodiode area by an insulating area and comprising a plurality of transistors for driving said photodiode; and

a shield, formed on top of said active area and protecting said active area from irradiation, wherein said shield is connected to a predetermined voltage or is grounded.

2. The layout of Claim 1, wherein for said photodiode area, said P-type semiconductor substrate is used as a positive electrode and a N-type well in said P-type semiconductor substrate is used as a negative electrode.

3. The layout of Claim 1, wherein for said photodiode area, a N-type well is used as a negative electrode and a P-type diffusion area in said N-type well is used as a positive electrode.

4. The layout of Claim 1, wherein said shield is made of metal.

5. The layout of Claim 1, wherein said shield is connected to a predetermined voltage or is grounded to avoid charge accumulation.

6. A layout of a CMOS image sensor, said layout comprising:

a photodiode area, formed on a P-type semiconductor substrate; and

an active area, formed on said semiconductor substrate, separated from said photodiode area by an insulating area and comprising a plurality of transistors for driving said photodiode;

wherein said layout is characterized in that a shielding metal is simultaneously formed on top of said active area during the metallization process of peripheral circuits and is connected to a predetermined voltage or is grounded.