VIRTUAL CHANNEL MEMORY SYSTEM

ABSTRACT

A memory system (300) having a main memory which is coupled to a plurality of parallel virtual access channels. Each of the virtual access channels (1) provides a set of memory access resources for controlling the main memory. These memory access resources include cache resources (including cache chaining), burst mode operation control and precharge operation control. A plurality of the virtual access channels are cacheable virtual access channels, each of which includes a channel row cache memory (601-607) for storing one or more cache entries and a channel row address register (701-707) for storing corresponding cache address entries. One or more non-cacheable virtual access channels (1-8) are provided by a bus bypass circuit (311). Each virtual access channel is addressable, such that particular memory masters can be assigned to access particular virtual access channels.

Fig. 3