CIRCUIT FOR HANDLING DISTRIBUTED ARBITRATION
IN A COMPUTER SYSTEM HAVING MULTIPLE ARBITERS

ABSTRACT OF THE DISCLOSURE

An arbitration scheme for a computer system having multiple arbiters for arbitrating access to a plurality of buses. In the preferred embodiment, a computer system is divided into a detachable laptop portion and an expansion base unit coupled through a shared PCI bus. Each of the two portions of the computer system includes separate PCI arbitration circuitry for arbitrating requests for the PCI bus from potential PCI and ISA bus masters. Included within the laptop portion of the computer system is a top level arbiter that determines whether the PCI arbiter in the laptop or expansion base unit has access to the PCI bus. Either PCI arbiter normally must receive a grant from the top level arbiter before it runs a cycle. While the laptop computer is docked, the top level arbiter selects between the PCI arbiters on an essentially time multiplexed basis. While the expansion base and laptop computer are undocked, the top level arbiter grants bus access to the laptop PCI arbiter.

(Figure 1)