(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
26 February 2009 (26.02.2009)

PCT

(10) International Publication Number
WO 2009/025706 A1

(51) International Patent Classification:
H01L 21/285 (2006.01) *H01L 23/485* (2006.01)
H01L 21/336 (2006.01)

(21) International Application Number:
PCT/US2008/008801

(22) International Filing Date: 18 July 2008 (18.07.2008)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/841,161 20 August 2007 (20.08.2007) US

(71) Applicant *(for all designated States except US)*: **ADVANCED MICRO DEVICES, INC.** [US/US]; One Amd Place, Mail Stop 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: **BALASUBRAMANIAN, Sriram** [IN/US]; 39663 Leslie Street Apt. 412, Fremont, CA 94538 (US).

(74) Agent: **DRAKE, Paul, S.**; Advanced Micro Devices, Inc., 7171 Southwest Parkway, Mail Stop B100.3.341, Austin, TX 78735 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

(54) **Title:** MOS STRUCTURES THAT EXHIBIT LOWER CONTACT RESISTANCE AND METHODS FOR FABRICATING THE SAME

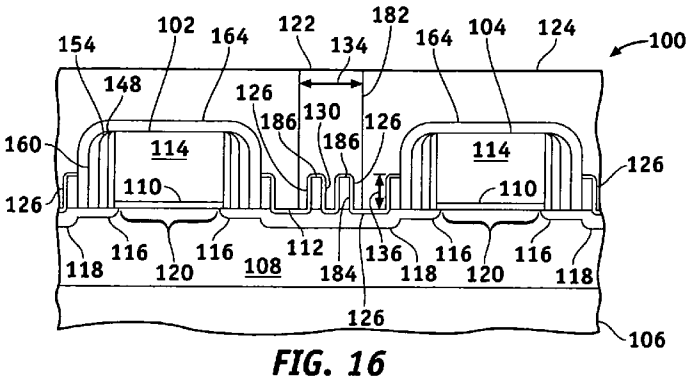


FIG. 16

(57) **Abstract:** MOS structures (100, 200) that exhibit lower contact resistance and methods for fabricating such MOS structures are provided. In one method, a semiconductor substrate (106) is provided and a gate stack (146) is fabricated on the semiconductor substrate. An impurity-doped region (116) within the semiconductor substrate aligned with the gate stack is formed. Adjacent contact fins (186) extending from the impurity-doped region are fabricated and a metal suicide layer (126) is formed on the contact fins. A contact (122) to at least a portion of the metal suicide layer on at least one of the contact fins is fabricated.

WO 2009/025706 A1