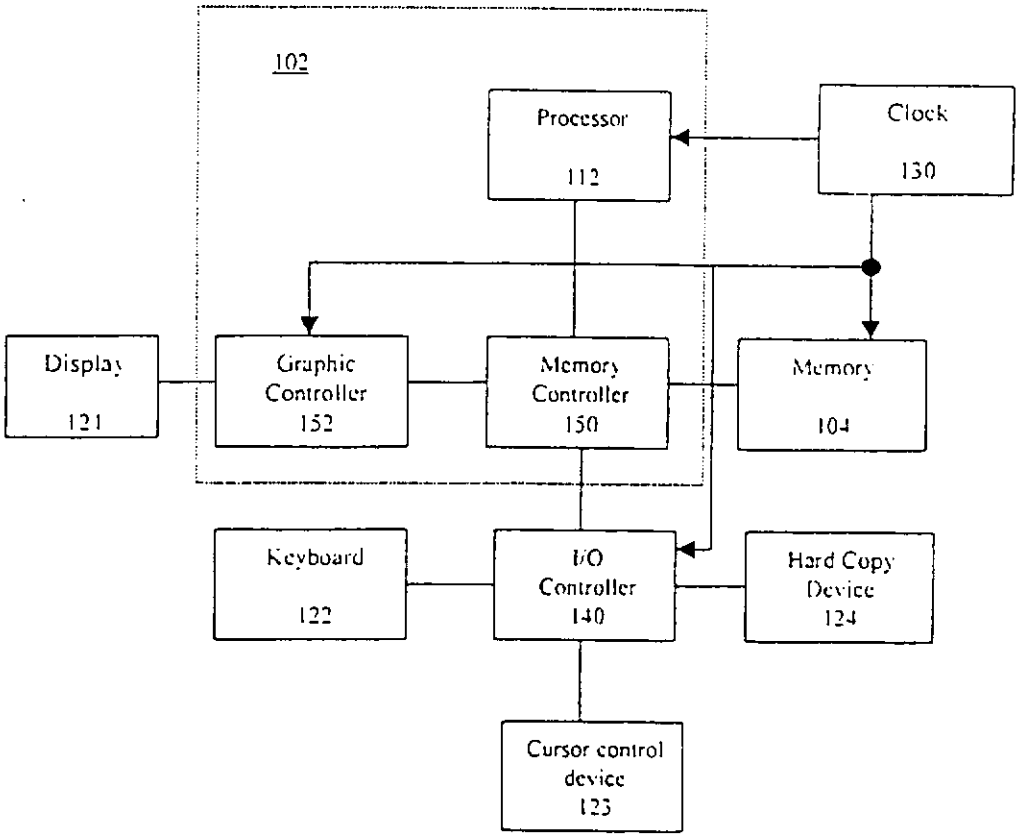

100
102
Processor
112
Clock
130
Display
121
Graphic
Controller
152
Memory
Controller
150
Memory
104
Keyboard
122
I/O
Controller
140
Hard Copy
Device
124
Cursor control
device
123

FIG. 1

200

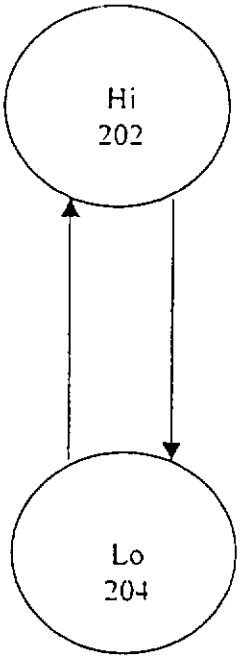


FIG. 2

300

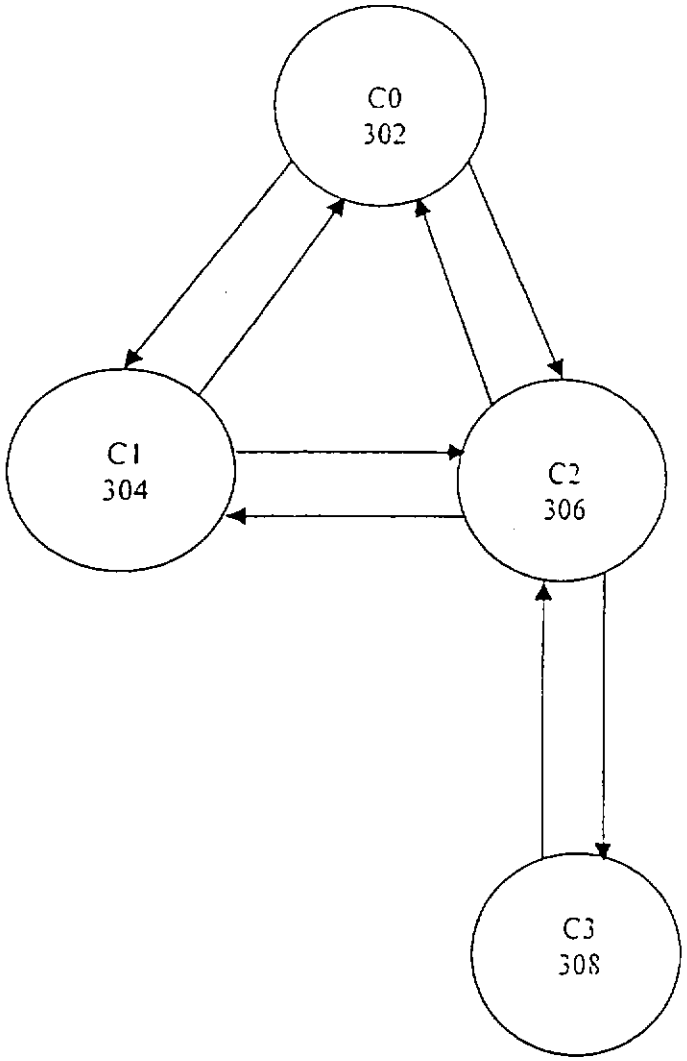


FIG. 3

400

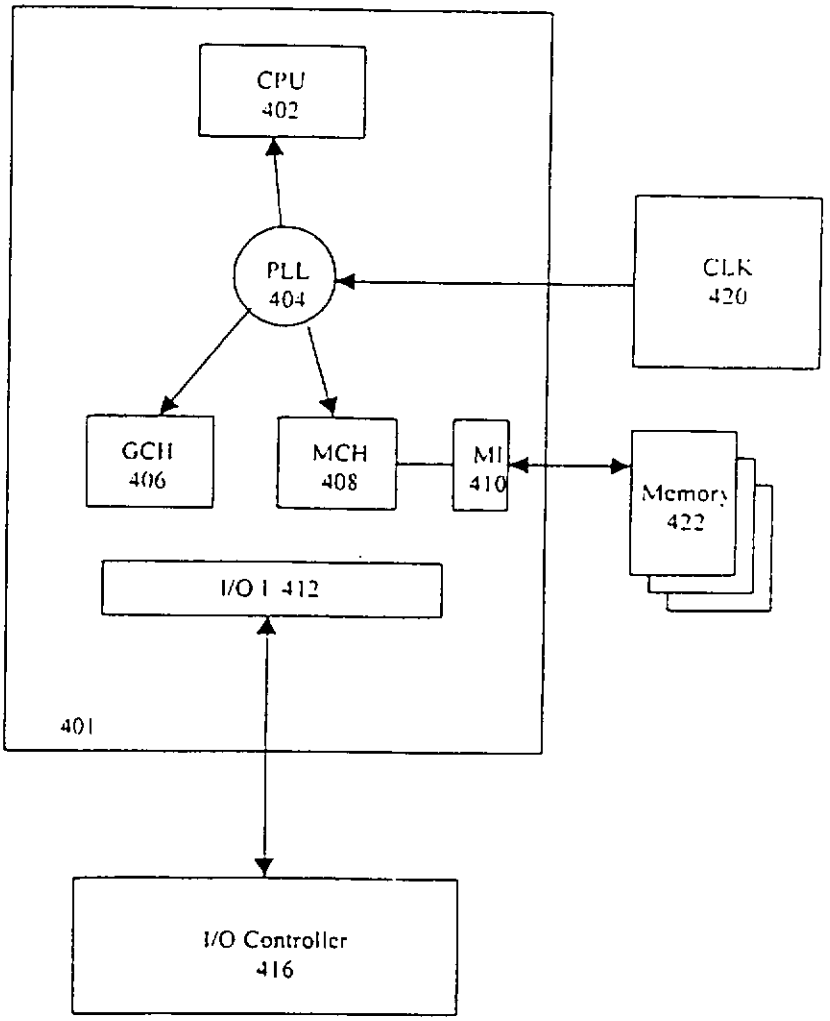

CPU
402
PLL
404
CLK
420
GCH
406
MCH
408
MI
410
Memory
422
I/O I 412
401
I/O Controller
416

FIG. 4

500

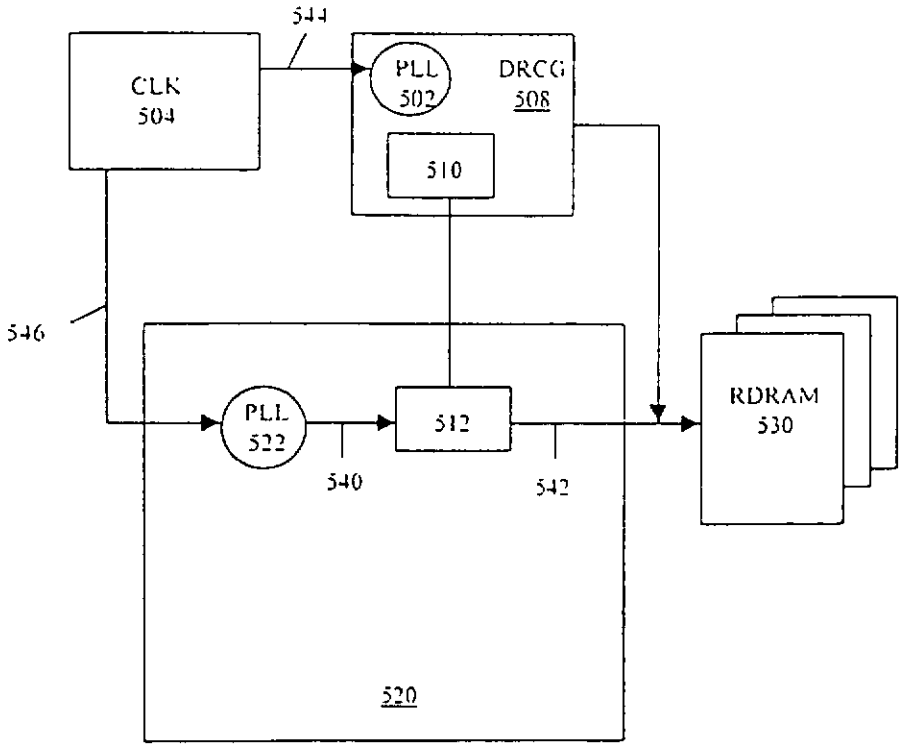

544
CLK
504
PLL
502
DRCG
508
510
546
PLL
522
512
RDRAM
530
540
542
520

FIG. 5

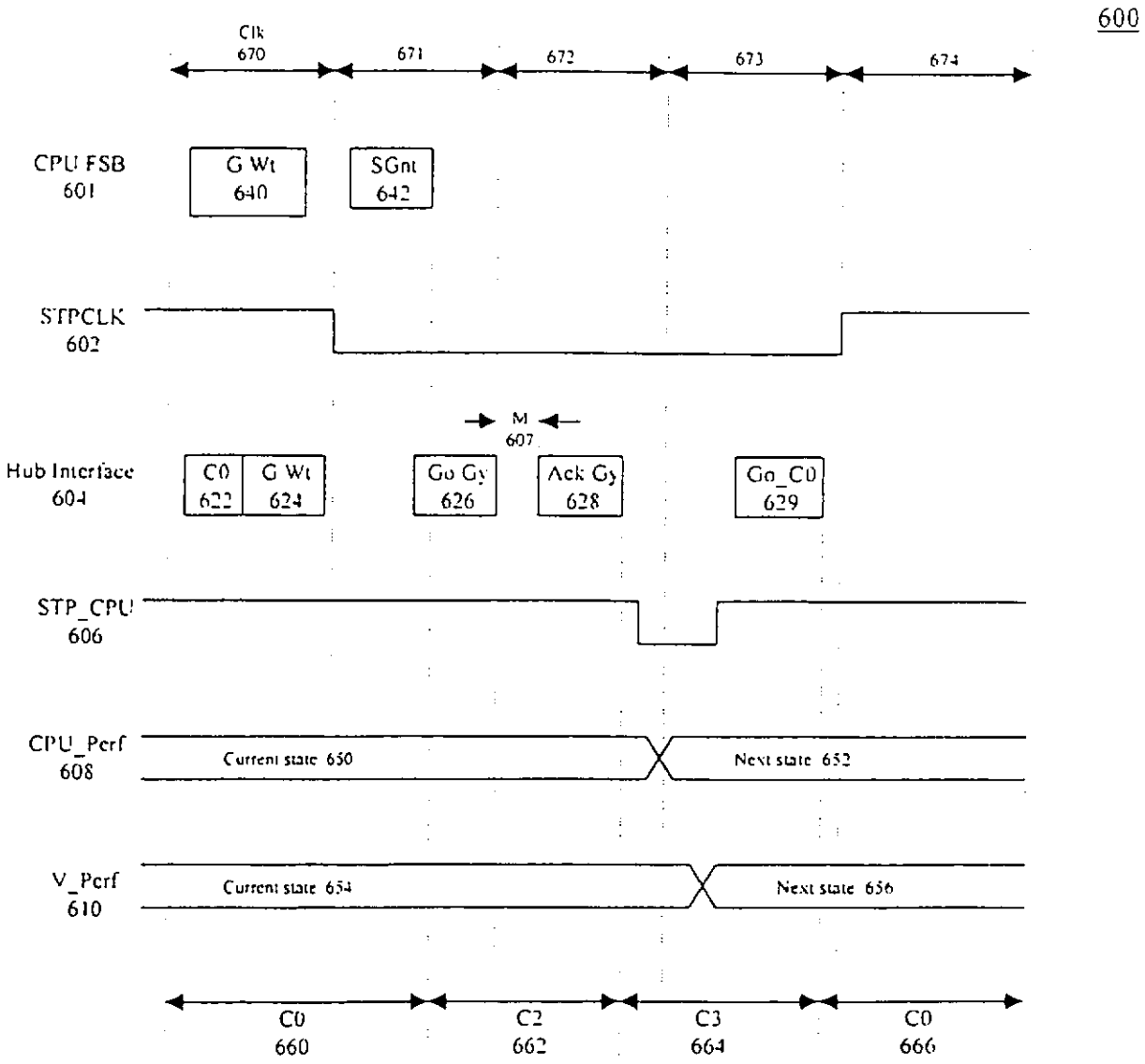

600
Clk
670
671
672
673
674
CPU FSB
601
G Wt
640
SGnt
642
STPCLK
602
M
607
Hub Interface
604
C0
622
G Wt
624
Go Gy
626
Ack Gy
628
Go_C0
629
STP_CPU
606
CPU_Perf
608
Current state 650
Next state 652
V_Perf
610
Current state 654
Next state 656
C0
660
C2
662
C3
664
C0
666

FIG. 6

700

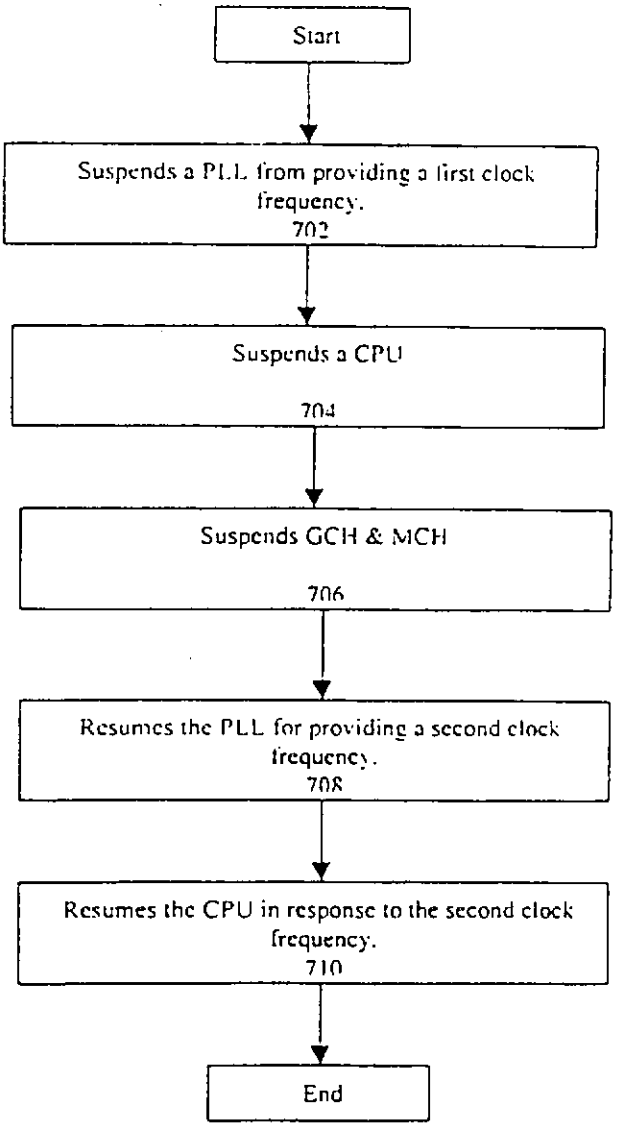

Start
Suspends a PLL from providing a first clock frequency.
702
Suspends a CPU
704
Suspends GCH & MCH
706
Resumes the PLL for providing a second clock frequency.
708
Resumes the CPU in response to the second clock frequency.
710
End

FIG. 7

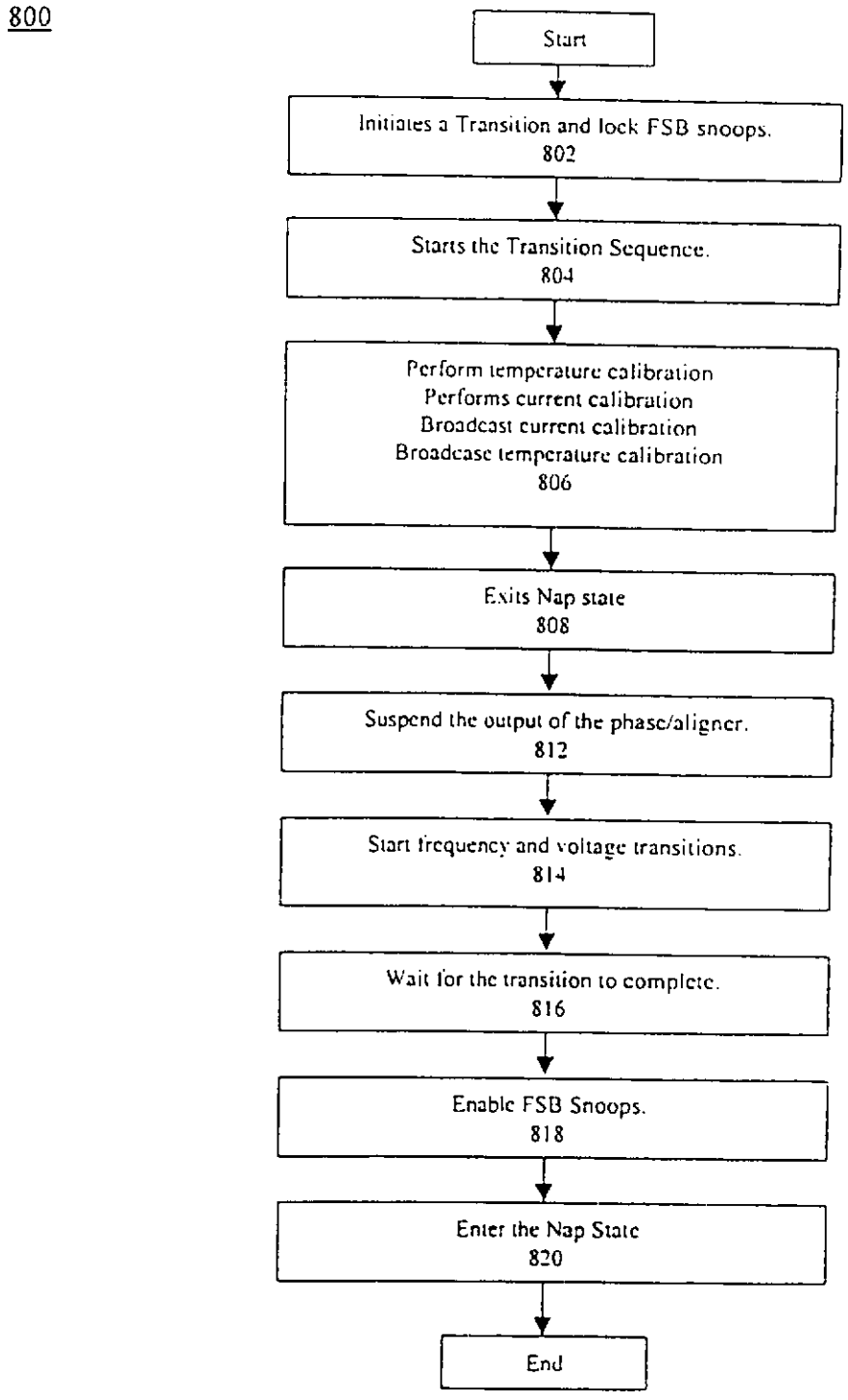

800
Start
Initiates a Transition and lock FSB snoops.
802
Starts the Transition Sequence.
804
Perform temperature calibration
Performs current calibration
Broadcast current calibration
Broadcase temperature calibration
806
Exits Nap state
808
Suspend the output of the phase/aligner.
812
Start frequency and voltage transitions.
814
Wait for the transition to complete.
816
Enable FSB Snoops.
818
Enter the Nap State
820
End

FIG. 8