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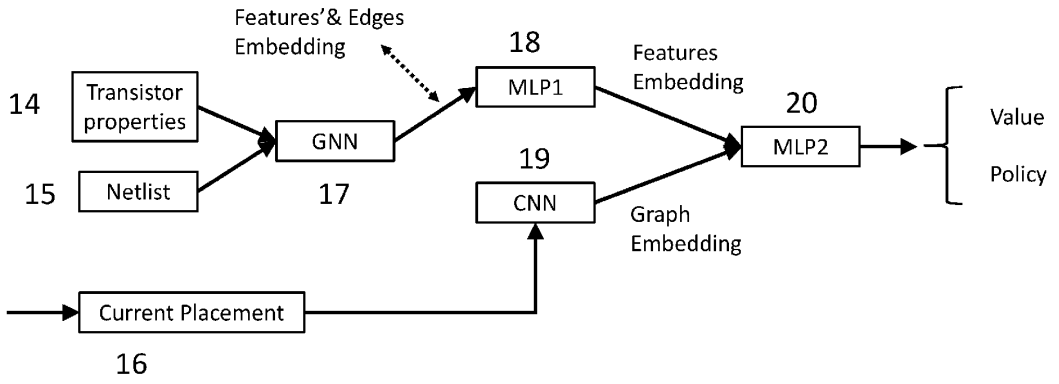

Fig. 3

(57) Abstract: In an integrated circuit, a method of flattened placement and/or routing of multiple transistors using an artificial intelligence (Al) model, comprising the steps of receiving an input consisting of a circuit schematic and features; performing supervised or unsupervised learning of the Al model, to produce a predicted placement and/or routing by the Al model; using a cost function for optimizing transistor placement and/or routing. An optimal placement and/or routing is generated by iteratively running cycles of placement and/or routing, based on the Al model; assigning a value to each placement and/or routing combination, according to the cost function and recording the placements and/or routings and value information across the performed iterations until meeting a predetermined metric or exceeding a predetermined number of iterations or elapsed time; ranking each of the generated placements and/or routing according to the cost function; selecting the k-top (k=l,2,....) placement and/or routing combinations.

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