

Abstract

A semiconductor memory device with improved performance and reliability is provided. The semiconductor memory device includes a substrate having a cell region and a peripheral region, a cell region isolation layer that separates the cell region from the peripheral region, and a plurality of cell gate structures, each including a cell gate electrode that extends in a first direction. The cell region includes a plurality of active areas that extend in a second direction different from the first direction, and are between a respective cell element isolation layer and the cell region isolation layer. Each of the active areas includes a first portion and a second portion separated by the cell gate structure, the second portion of the active area is on both sides of a respective one of the first portion of the active area. The active areas includes a normal active area and a dummy active area.

FIG. 4