

## ABSTRACT

## A METHOD OF FABRICATING THREE DIMENSIONAL CMOSFET DEVICES FOR AN EMBEDDED DRAM APPLICATION

A method of reducing the aspect ratio for dry etch processes used to form contact hole and storage node openings in composite insulator layers, to expose regions of CMOS devices used for embedded memory cell applications, has been developed. The method features formation of CMOS devices for an embedded memory cell in a recessed region of a semiconductor substrate, while peripheral, higher performing CMOS devices are formed on a non-recessed, SOI layer. Removal of a top portion of a first planarized insulator layer, only in the embedded memory cell region, allows reduction of the aspect ratio of a storage node opening formed in the bottom portion of the first planarized insulator layer. Formation of an overlying, second planarized insulator layer results in a composite insulator layer comprised of a thinned, second planarized insulator layer on the underlying first planarized insulator layer, in the peripheral CMOS device region. The thinned, second planarized insulator component of the composite insulator layer allows reduction of the aspect ratio for formation of a contact hole now defined in the composite insulator layer.

(Fig. 1)



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