CLAIMS

What is claimed is:

1. A clock generation circuit, comprising:

an input end, configured to input a pulse signal;

a first output end, configured to output a first clock signal;

a second output end, configured to output a second clock signal; and

an input drive circuit, a latch circuit, an edge shaping circuit, a feedback delay circuit, and an output drive circuit, wherein

the input end is connected to the input drive circuit,

the input drive circuit is connected to the latch circuit and the edge shaping circuit,

the latch circuit is connected to the edge shaping circuit and the feedback delay circuit,

the edge shaping circuit is connected to the feedback delay circuit and the output drive circuit, and

the output drive circuit is connected to the first output end and the second output end.

2. The clock generation circuit according to claim 1, wherein the input drive circuit comprises a first inverter and a second inverter that are sequentially connected in series, each of the first inverter and the second inverter comprises a first end and a second end, the first end of the first inverter is electrically connected to the input end, the second end of the second inverter is electrically connected to the latch circuit, and the second end of the first inverter is electrically connected to the first end of the second inverter and the edge shaping circuit.

3. The clock generation circuit according to claim 2, wherein the latch circuit comprises a first NAND gate and a second NAND gate that are in a cross-connection with each other, each of the first NAND gate and the second NAND gate comprises a first end, a second end, and a third end, the first end of the first NAND gate is electrically connected to the third end of the second NAND gate, the second end of the first NAND gate is electrically connected to the feedback delay circuit, the third end of the first NAND gate is electrically connected to the second end of the second NAND gate and the edge shaping circuit, and the first end of the second NAND gate is electrically connected to the second end of the second inverter.

4. The clock generation circuit according to claim 3, wherein the edge shaping circuit comprises a first PMOS transistor, a second PMOS transistor, a third PMOS transistor, a first

NMOS transistor, a second NMOS transistor, and a third NMOS transistor, each of the first PMOS transistor, the second PMOS transistor, the third PMOS transistor, the first NMOS transistor, the second NMOS transistor, and the third NMOS transistor comprises a first end, a second end, and a control end, the first end of the first PMOS transistor and the first end of the second PMOS transistor are electrically connected to a power supply, the second end of the first PMOS transistor and the second end of the second PMOS transistor are electrically connected to the first end of the third PMOS transistor, the second end of the third PMOS transistor is respectively electrically connected to the first end of the first NMOS transistor and the first end of the second NMOS transistor, the second end of the second NMOS transistor is electrically connected to the first end of the third NMOS transistor, the second end of the first NMOS transistor and the second end of the third NMOS transistor are electrically connected to a ground, the control end of the first PMOS transistor and the control end of the second NMOS transistor are electrically connected to the second end of the first inverter, the control end of the third PMOS transistor and the control end of the first NMOS transistor are electrically connected to the third end of the first NAND gate, and the control end of the second PMOS transistor and the control end of the third NMOS transistor are electrically connected to the second end of the third PMOS transistor, the feedback delay circuit, and the output drive circuit.

5. The clock generation circuit according to claim 4, wherein the feedback delay circuit comprises a first end, a second end, and a plurality of inverters connected between the first end of the feedback delay circuit and the second end of the feedback delay circuit in series, the first end of the feedback delay circuit is electrically connected to the second end of the third PMOS transistor, and the second end of the feedback delay circuit is electrically connected to the second end of the first NAND gate.

6. The clock generation circuit according to claim 5, wherein the output drive circuit comprises a third inverter, a fourth inverter, and a fifth inverter, each of the third inverter, the fourth inverter, and the fifth inverter comprises a first end and a second end, the first end of the third inverter is electrically connected to the second end of the third PMOS transistor, the second end of the third inverter is electrically connected to the first output end, the first end of the fourth inverter is electrically connected to the second end of the third PMOS transistor, the second end of the fourth inverter is electrically connected to the first end of the fifth inverter, and the second end of the fifth inverter is electrically connected to the second output end.

7. A latch, comprising:

a data input end, configured to input a data signal;

a data output end, configured to output the data signal;

a clock signal input end, configured to input a first clock signal;

a plurality of levels of latch circuits, sequentially connected between the data input end and the data output end in series according to a first sequence; and

a plurality of levels of clock generation circuits, sequentially connected in series according to a second sequence and electrically connected to the plurality of levels of latch circuits, wherein

a direction of the first sequence is opposite to a direction of the second sequence, and each clock generation circuit in each level of the plurality of levels of clock generation circuits is the clock generation circuit according to claim 1.

8. The latch according to claim 7, wherein one level of the levels of latch circuits corresponds to one level of the levels of clock generation circuits.

9. The latch according to claim 8, wherein each level of the levels of latch circuits further comprises a plurality of latch units.

10. The latch according to claim 9, wherein each level of the levels of clock generation circuits further comprises a plurality of clock generation circuits.

11. The latch according to claim 9, wherein the plurality of latch units are connected in series.

12. The latch according to claim 9, wherein the plurality of latch units are connected in parallel.

13. The latch according to claim 9, wherein the plurality of latch units are in a combination of serial and parallel connections.

14. The latch according to claim 10, wherein each of the latch units corresponds to each of the clock generation circuits.

15. A computing device, comprising one or more latches according to any one of claims 7 to 14.