What is Claimed is:

1. A method of forming an integrated circuit device, comprising:

forming a field effect transistor having a gate electrode, a sacrificial spacer on a sidewall of the gate electrode and silicided source/drain regions, on a semiconductor substrate;

depositing a mask layer to expose at least a portion of the sacrificial spacer on the semiconductor substrate;

removing the sacrificial spacer by selectively etching the exposed sacrificial spacer using the mask layer as an etching mask; and

forming a stress-inducing electrically insulating layer that is configured to induce a net tensile or compressive stress in a channel region of the field effect transistor, on the sidewall of the gate electrode.

2. The method of Claim 1, wherein the silicided source/drain regions comprise source/drain regions having a first metal silicide layer thereon that is self-aligned to the sacrificial spacer.

3. The method of Claim 2, wherein depositing a mask layer comprises:

forming a mask layer on the field effect transistor; and

partially etching back the mask layer to expose the sacrificial spacer.

4. The method of Claim 1, wherein the mask layer is a photoresist layer.

5. The method of Claim 1, wherein the sacrificial spacer comprises a nitride insulating material.

6. The method of Claim 3, wherein the field effect transistor comprises a second metal silicide layer on the gate electrode; and wherein partially etching comprises partially etching back the mask layer to expose the sacrificial spacer and the second metal silicide layer.

7. The method of Claim 6, wherein selectively etching comprises exposing the second metal silicide layer to a wet and/or dry etchant.

8. The method of Claim 3, further comprising removing the partially etched-back mask layer; and wherein forming a stress-inducing electrically insulating layer comprises depositing a stress-inducing electrically insulating layer on the second metal silicide layer.

9. The method of Claim 3, further comprising removing the partially etched-back mask layer; and wherein forming a stress-inducing electrically insulating layer comprises depositing a stress-inducing electrically insulating layer on an upper surface and the sidewall of the gate electrode.

10. The method of Claim 1, wherein the mask layer covers a top surface of the source/drain region.

11. The method of Claim 1, wherein the sacrificial spacer is removed by dry etching.

12. The method of Claim 11, wherein the dry etching is performed using an etching gas having a higher etch rate of the first spacer than that of the mask layer.

13. The method of Claim 1, wherein the stress layer is a tensile stress layer.

14. The method of Claim 13, wherein the transistor is an N-type transistor.

15. The method of Claim 1, wherein the stress layer is a compressive stress layer.

16. The method of claim 15, wherein the transistor is a P-type transistor.

17. A method of forming an integrated circuit device, comprising:

forming a gate electrode on a surface of a semiconductor substrate;

forming a first electrically insulating spacer on a sidewall of the gate electrode;

depositing a second electrically insulating layer on the gate electrode and on the surface of the semiconductor substrate;

etching back the second electrically insulating layer for a sufficient duration to define a sacrificial spacer on the first electrically insulating spacer;

forming source and drain regions adjacent the gate electrode by implanting source and drain region dopants into the surface using the sacrificial spacer as an implant mask;

forming metal silicide layers on the source and drain regions;

depositing a mask layer on the gate electrode, the sacrificial spacer and the metal silicide layers;

partially etching back the mask layer to expose the sacrificial spacer;

removing the sacrificial spacer by selectively etching the exposed sacrificial spacer using the mask layer to protect the metal silicide layers from etching damage; and

forming a stress-inducing electrically insulating layer that is configured to induce a net tensile or compressive stress in a portion of the semiconductor substrate, on the sidewall of the gate electrode.

18. A method of forming an integrated circuit device, comprising:

forming a field effect transistor having a gate electrode, a sacrificial spacer on a sidewall of the gate electrode and LDD source/drain regions, on a semiconductor substrate; and

replacing the sacrificial spacer with a stress-inducing electrically insulating layer that is configured to induce a net tensile or compressive stress in a channel region of the field effect transistor.

19. The method of Claim 18, wherein the LDD source/drain regions have silicided layers thereon; and wherein replacing the sacrificial spacer comprises selectively etching the sacrificial spacer using a mask layer to protect the silicided layers from etching damage.

20. A semiconductor integrated circuit device comprising:

a gate insulating film formed on a semiconductor substrate;

a gate electrode formed on the gate insulating film;

a source/drain region aligned with the gate electrode; and

silicide layers formed on the source/drain region and a top surface of the gate electrode, respectively,

wherein the surface damage of the silicide layer formed on the source/drain region is less than that of the silicide layer formed on the top surface of the gate electrode.

21. The device of Claim 20, wherein the silicide layer on the source/drain region is separated a predetermined distance away from the gate electrode, and a portion of a surface of the semiconductor substrate on which the silicide layer is not formed is more damaged than a surface of the silicide layer on the source/drain region.

22. The device of Claim 21, further comprising a first spacer extending from a side surface of the gate electrode to a portion of a top surface of the semiconductor substrate on which the silicide layer is not formed.

23. The device of Claim 22, wherein the first spacer is an oxide film.

24. The device of Claim 20, further comprising a stress layer covering the gate electrode and the semiconductor substrate.

What is claimed is:

1. A method of forming an integrated circuit device, comprising:

forming a field effect transistor having a gate electrode, a sacrificial spacer on a sidewall of the gate electrode and silicided source/drain regions, on a semiconductor substrate;

depositing a mask layer to expose at least a portion of the sacrificial spacer on the semiconductor substrate;

removing the sacrificial spacer by selectively dry etching the exposed sacrificial spacer using the mask layer as an etching mask, said dry etching performed using an etching gas having higher etch rate for the sacrificial spacer relative to the mask layer; and

forming a stress-inducing electrically insulating layer that is configured to induce a net tensile or compressive stress in a channel region of the field effect transistor, on the sidewall of the gate electrode.

2. The method of claim 1, wherein the silicided source/drain regions comprise source/drain regions having a first metal silicide layer thereon that is self-aligned to the sacrificial spacer.

3. The method of claim 2, wherein depositing a mask layer comprises:

forming a mask layer on the field effect transistor; and

partially etching back the mask layer to expose the sacrificial spacer.

4. The method of claim 3, wherein the field effect transistor comprises a second metal silicide layer on the gate electrode; and wherein partially etching comprises partially etching back the mask layer to expose the sacrificial spacer and the second metal silicide layer.

5. The method of claim 4, further comprising removing the partially etched-back mask layer; and wherein forming a stress-inducing electrically insulating layer comprises depositing a stress-inducing electrically insulating layer on the second metal silicide layer.

6. The method of claim 1, wherein the mask layer is a photoresist layer.

7. The method of claim 1, wherein the sacrificial spacer comprises a nitride insulating material.

8. The method of claim 1, wherein the mask layer covers a top surface of the source/drain region.

9. The method of claim 1, wherein the stress-inducing electrically insulating layer is a tensile stress layer.

10. The method of claim 9, wherein the field effect transistor is an N-type transistor.

11. The method of claim 1, wherein the stress-inducing electrically insulating layer is a compressive stress layer.

12. The method of claim 11, wherein the field effect transistor is a P-type transistor.

13. A method of forming an integrated circuit device, comprising:

forming a field effect transistor having a gate electrode, a sacrificial spacer on a

sidewall of the gate electrode and silicided source/drain regions, on a semiconductor substrate;

depositing a mask layer to expose at least a portion of the sacrificial spacer on the semiconductor substrate;

removing the sacrificial spacer by selectively etching the exposed sacrificial spacer using the mask layer as an etchin mask; and

forming a stress-inducing electrically insulating layer that is configured to induce a net tensile or compressive stress in a channel region of the field effect transistor, on the sidewall of the gate electrode;

wherein the silicided source/drain regions comprise source/drain regions having a first metal silicide layer thereon that is self-aligned to the sacrificial spacer;

wherein depositing a mask layer comprises:

forming a mask layer on the field effect transistor; and

partially etching back the mask layer to expose the sacrificial spacer;

wherein the field effect transistor comprises a second metal silicide layer on the gate electrode;

wherein partially etching comprises partially etching back the mask layer to expose the sacrificial spacer and the second metal silicide layer; and

wherein selectively etching comprises exposing the second metal silicide layer to a wet and/or dry etchant.

14. A method of forming an integrated circuit device, comprising:

forming a field effect transistor having a gate electrode, a sacrificial spacer on a sidewall of the gate electrode and silicided source/drain regions, on a semiconductor substrate;

depositing a mask layer to expose at least a portion of the sacrificial spacer on the semiconductor substrate;

removing the sacrificial spacer by selectively etching the exposed sacrificial spacer using the mask layer as an etching mask; and

forming a stress-inducing electrically insulating layer that is configured to induce a net tensile or compressive stress in a channel region of the field effect transistor, on the sidewall of the gate electrode;

wherein the silicided source/drain regions comprise source/drain regions having a first metal silicide layer thereon that is self-aligned to the sacrificial spacer;

wherein depositing a mask layer comprises:

forming a mask layer on the field effect transistor;

partially etching back the mask layer to expose the sacrificial spacer; and

removing the partially etched-back mask layer; and

wherein forming a stress-inducing electrically insulating layer comprises depositing a stress-inducing electrically insulating layer on an upper surface and the sidewall of the gate electrode.

15. A method of forming an integrated circuit device, comprising:

forming a field effect transistor having a gate electrode, a sacrificial spacer on a sidewall of the gate electrode and LDD source/drain regions, on a semiconductor substrate; and

replacing the sacrificial spacer with a stress-inducing electrically insulating layer that is configured to induce a net tensile or compressive stress in a channel region of the field effect transistor;

wherein the LDD source/drain regions have silicided layers thereon; and

wherein replacing the sacrificial spacer comprises selectively etching the sacrificial spacer using a mask layer to protect the silicided layers from etching damage.