

## DIFFERENTIAL SENSE AMPLIFIER WITHOUT SWITCH TRANSISTORS

DESCRIPTIVE ABSTRACT

A differential sense amplifier for sensing data stored in a plurality of memory cells (C) of a memory cell array, including:

- a first CMOS inverter having an output connected to a first bit line (BL) and an input connected to a second bit line (/BL) complementary to the first bit line,
- a second CMOS inverter having an output connected to the second bit line (/BL) and an input connected to the first bit line (BL),

each CMOS inverter comprising a pull-up transistor (M21, M22) and a pull-down transistor (M31, M32), wherein the sources of the pull-up transistors (M21, M22) or pull-down transistors (M31, M32) are electrically coupled and connected to a pull-up voltage source or a pull-down voltage source, without an intermediate transistor between the sources of the transistors and the voltage source.

FIGURE 3