based systems. In order to perform CMOS compatible processes with suitable isolation schemes, there is a need to develop a new device processing sequence.

Accordingly, there is a need to provide a method for fabricating semiconductor devices which overcomes, or at least ameliorates, one or more of the disadvantages described above.

To overcome the abovementioned issues, there is a need to develop an Au-free CMOS compatible self-aligning method for fabricating transistors (e.g. MOSFETs) using AlGaN/GaN HEMT based systems grown on bulk Si or silicon on insulator (SOI) substrates. Such a method may also be applicable to GaN-based HEMT structure on sapphire substrates or silicon carbide (SiC) substrate.

Particularly, there is a need to develop an intermediate platform or layer to enhance the compatibility of CMOS process technology on HEMT devices while using selected metal layering that could improve contact/ohmic resistance.

Summary

There is provided a method for fabricating a semiconductor device comprising the steps of:

growing a first and a second nucleation layer on a substrate;

depositing a binary layer over the first and second nucleation layers; and

annealing the binary layer to form a first contact area and a second contact area on the substrate, wherein the annealed binary layer comprises a group 14 element selected from Si, Ge and their combination thereof, and the annealed binary layer in the first and second contact areas are capable of providing a lower contact resistance for a current to flow in the device.

so as to improve contact/ohmic resistance, particularly at the S/D.

A CMOS compatible metal selected from the group of Ta, TaN, Ti, TiN, Ni, Co, Al, W, WN, any non-gold based metal and their combination thereof, may then be deposited on the metal layer having a group 14 element selected from Si, Ge and their combination thereof, to form the binary layer in the at least two troughs, and the gate electrode may be formed on the island between the first and second contact areas after the binary layer in the at least two troughs is annealed with the second epitaxial layer to form the first and second contact areas. The CMOS compatible metal may also be deposited on the metal layer to form the binary layer over the exposed second and/or third epitaxial layer while the gate electrode is formed on the island between the first and second contact areas after the binary layer is annealed with the second and/or third epitaxial layer to form the first and second contact areas.

In the present method, the annealing of the binary layer with the first, second or third epitaxial layer to form the first and second contact areas may occur at 400°C to 800°C. The annealing may involve any of the first, second or third epitaxial layer.

There is provided a semiconductor device having a structure comprising:

a first and a second nucleation layer disposed on a substrate;

a binary layer comprising a group 14 element selected from Si, Ge and their combination thereof disposed over the first and second nucleation layers; and

a first contact area and a second contact area disposed over the substrate, wherein the first and second contacts areas formed from annealing the binary layer with

the first, second or third epitaxial layer are capable of providing a lower contact resistance for a current to flow in the device.

In another aspect, there is provided a semiconductor device having a structure comprising:

a first nucleation layer and a second nucleation layer disposed on a substrate;

a first epitaxial layer and a second epitaxial layer disposed over the first and second nucleation layers to form a channel layer comprising portions of the first and second epitaxial layers;

a third epitaxial layer disposed on the second epitaxial layer;

a binary layer comprising a group 14 element selected from Si, Ge and their combination thereof disposed over the first and second nucleation layers;

a thin spacer located between the binary layer and the third epitaxial layer; and

a first contact area and a second contact area disposed over the substrate, wherein the first and second contacts areas formed from annealing the binary layer with the first, second or third epitaxial layer are capable of providing a lower contact resistance for a current to flow in the device.

The first and second nucleation layers may comprise a first aluminum nitride nucleation layer followed by a second thicker aluminum nitride nucleation layer. A gallium nitride layer may be disposed over the first and second nucleation layers followed by an ultrathin spacer AlN layer, an AlGaN barrier layer, and a thin binary GaN cap layer.

Advantageously, this structure provides a way for integrating CMOS compatible process on GaN/AlGaN HEMT structure. This structure may be produced via a self-

aligning method in the sense that multiple photo-resist steps may be circumvented or minimized in order to build the various structures such as the S/D features, the gate electrode etc. This structure is capable of allowing the contact resistance to be reduced to at least match or overcome the performance of devices produced using Au-based contact technologies.

Advantageously, the structure comprises of a thicker aluminium nitride (AlN) layer grown over the first and second nucleation layers on the substrate which allows the quality of a deposited GaN epitaxial layer to be fine-tuned via the thickness of both the first and the second AlN layers. The thickness may be altered by growing or depositing at least one layer of aluminum nitride (AlN). Hence, at least one AlN layer may be deposited. Each of this at least one AlN layer may be deposited at different temperatures or pressures. The surface temperature during the growth of the first AlN nucleation layer may be in the range of about 950 °C to about 1000 °C. The pressure during the growth of the first AlN nucleation layer may be in the range of about 50 torr to about 100 torr. The

fabricate a semiconductor device having the present semiconductor structure. Such devices may be selected from a group consisting of field effect transistors, high electron mobility transistors, inverters, power switches, power transistor devices, radio switches and radio-frequency based devices.

There is provided a transistor produced by the method as defined above.

In another aspect, there is provided a transistor having the structure as defined above.

Definitions

The following words and terms used herein shall have the meaning indicated:

The term "group 14 element" may be used interchangeably with the term "group IV" element which both refer to elements in the carbon group. Group 14 or group IV elements may be selected from the group consisting of carbon (C), silicon (Si), germanium (Ge), tin (Sn) and lead (Pb).

The word "substantially" does not exclude "completely" e.g. a composition which is "substantially free" from Y may be completely free from Y. Where necessary, the word "substantially" may be omitted from the definition of the invention.

Unless specified otherwise, the terms "comprising" and "comprise", and grammatical variants thereof, are intended to represent "open" or "inclusive" language such that they include recited elements but also permit inclusion of additional, unrecited elements.

As used herein, the term "about", in the context of concentrations of components of the formulations, typically means +/- 5% of the stated value, more typically +/- 4% of the stated value, more typically +/- 3% of the

Claims

1. A semiconductor device having a structure comprising:

a first nucleation layer and a second nucleation layer disposed on a substrate;

a first epitaxial layer and a second epitaxial layer disposed over the first and second nucleation layers to form a channel layer comprising portions of the first and second epitaxial layers;

a third epitaxial layer disposed on the second epitaxial layer;

a binary layer comprising a group 14 element selected from Si, Ge and their combination thereof disposed over the first and second nucleation layers;

a thin spacer located between the binary layer and the third epitaxial layer; and

a first contact area and a second contact area disposed over the substrate, wherein the first and second contacts areas formed from annealing the binary layer with the first, second or third epitaxial layer are capable of providing a lower contact resistance for a current to flow in the device.

2. The semiconductor device of claim 1,

wherein the binary layer is disposed over the first, second and third epitaxial layers, and

wherein the first and second contact areas formed from annealing the binary layer with the first, second or third epitaxial layer, are disposed on the first or third epitaxial layer or partially embedded in the second and/or third epitaxial layer,

preferably further comprising a gate electrode disposed between the first and second contact areas before

or after the binary layer is annealed with the first, second or third epitaxial layer, and

preferably wherein the height of the gate electrode is 100 nm to 300 nm, and

preferably wherein the first nucleation layer has a thickness in the range of 25 nm to 30 nm, and

preferably wherein the second nucleation layer has a thickness in the range of 200 nm to 400 nm, and

preferably wherein the first epitaxial layer is a gallium nitride layer with a thickness of 1.5 um to 3.0 um, and

preferably wherein the second epitaxial layer is an aluminum gallium nitride layer with a thickness of 15 nm to 25 nm.

3. The semiconductor device of claim 2, wherein the second epitaxial layer has an aluminum content of 20 to 25 wt%,

preferably wherein the second epitaxial layer has an aluminum content of 22 to 23 wt%.

4. The semiconductor device of claim 2, wherein the third epitaxial layer is a gallium nitride layer having a thickness of 1.5 nm to 3.5 nm,

preferably wherein the gallium nitride layer has a thickness of 1.5 nm to 3.0 nm.

5. The semiconductor device of claim 2, wherein the channel layer is a two dimension electron gas (2DEG) layer,

optionally wherein the structure further comprises shallow isolated trenches, mesa isolated trenches or deposited oxide layers.

6. The semiconductor device of claim 2, wherein the gate electrode has a structure comprising the second epitaxial layer, the third epitaxial layer, a dieletric layer comprising aluminum oxide, hafnium oxide, or their combination thereof, and a CMOS compatible metal selected from the group of Ta, TaN, Ti, TiN, Ni, Co, Al, W, WN, any non-gold based metal and their combination thereof,

preferably wherein the first and the second contact areas are formed from annealing the first epitaxial layer, the binary layer comprising a group 14 element selected from Si, Ge and their combination thereof, and a CMOS compatible metal selected from the group of Ta, TaN, Ti, TiN, Ni, Co, Al, W, WN, any non-gold based metal and their combination thereof.

7. The semiconductor device of claim 6, wherein the gate electrode further comprises two thin spacer structures on both sides of the gate electrode, wherein the two thin spacer structures are disposed on the dielectric layer,

preferably wherein the gate electrode further comprises two thick spacer structures on both sides of the gate electrode, wherein the two thick spacer structures are disposed on the first epitaxial layer, and

preferably wherein the two thin and two thick spacers are made up of aluminum oxide, silicon nitride, silicon dioxide or their combination thereof, and

preferably wherein the two thick spacers have a width of 50 nm to 10um.

8. The semiconductor device of claim 2, wherein the gate electrode comprises a single CMOS compatible metal selected from the group of Ta, TaN, Ti, TiN, Ni, Co, Al, W, WN, any non-gold based metal and their combination thereof,

when the first and second contact areas are disposed over the third epitaxial layer or partially embedded in the second and/or third epitaxial layer,

preferably wherein the structure further comprises a field insulator layer disposed on an island formed from the first, second and third epitaxial layers in which the first and second contact areas are disposed over the third epitaxial layer or partially embedded in the second and/or third epitaxial layers, and a gate insulating layer disposed on the field insulator layer, and

preferably wherein the field insulator layer is a silicon nitride, silicon oxide, silicon-oxynitride or Al_2O_3 layer, and the gate insulating layer is gate dielectric layer selected from Al_2O_3, HfO_2, ZrO_2, TiO_2, Ta_2O_5, Ta-doped Al_2O_3, HfAlO, La_2O_3, Si_3N_4, SiON, Y_2O_3, $HfSiO_4$, $SrTiO_2$, $LaAlO_3$, SiO_2 and their combination thereof, and

preferably wherein the first and second contact areas disposed over the third epitaxial layer or partially embedded in the second and/or third epitaxial layer are made up of an annealed layer comprising the second and/or the third epitaxial layer, and the binary layer comprising a group 14 element selected from Si, Ge and their combination thereof, and a CMOS compatible metal selected from the group of Ta, TaN, Ti, TiN, Ni, Co, Al, W, WN, any non-gold based metal and their combination thereof.

9. The semiconductor device of claim 2, wherein the height of the gate electrode is 100 nm to 300 nm, and

optionally wherein the substrate is a sapphire substrate, a silicon substrate, a silicon on insulator substrate or a silicon carbide substrate.

10. A transistor having the structure of claim 1.