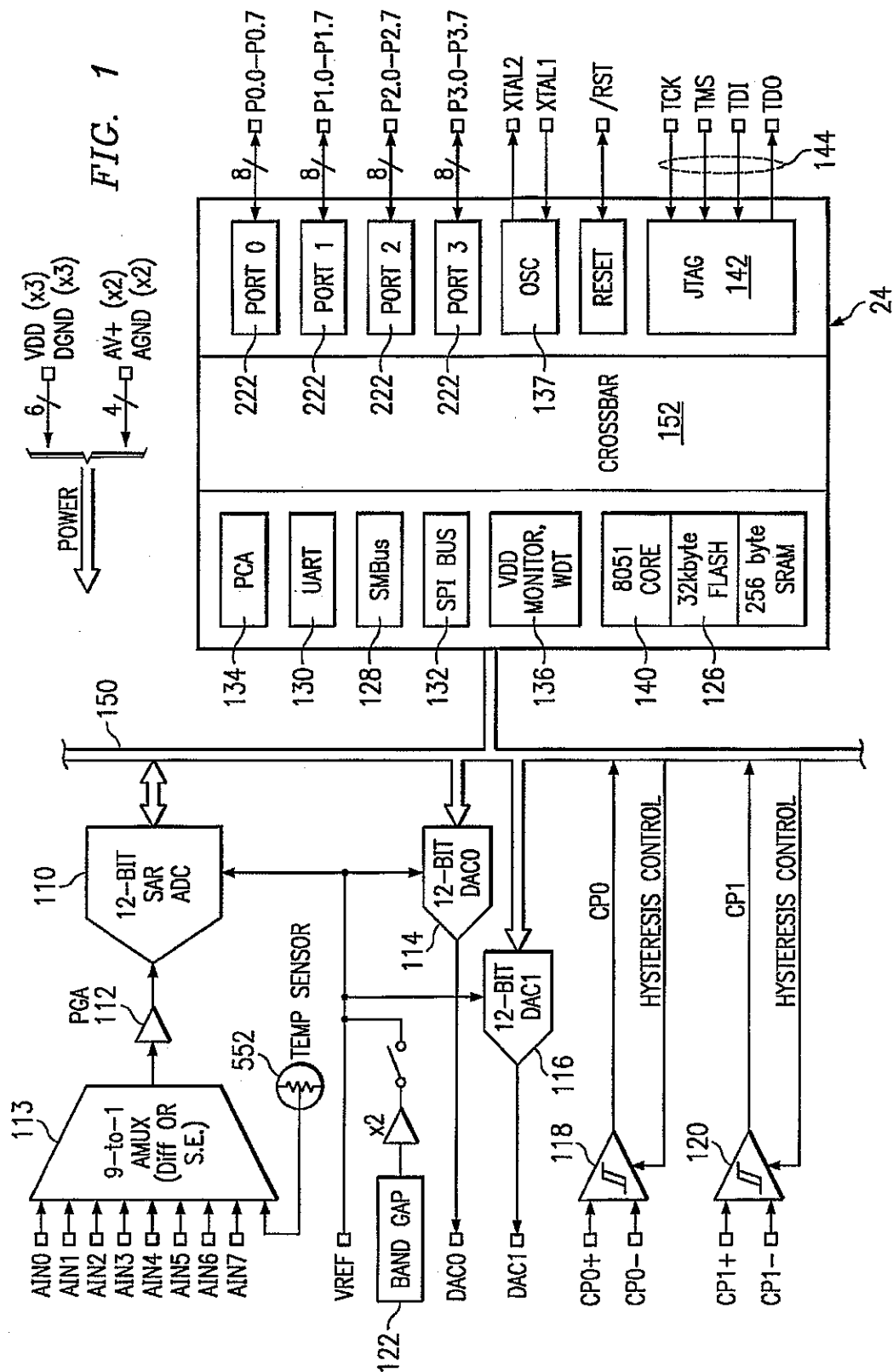
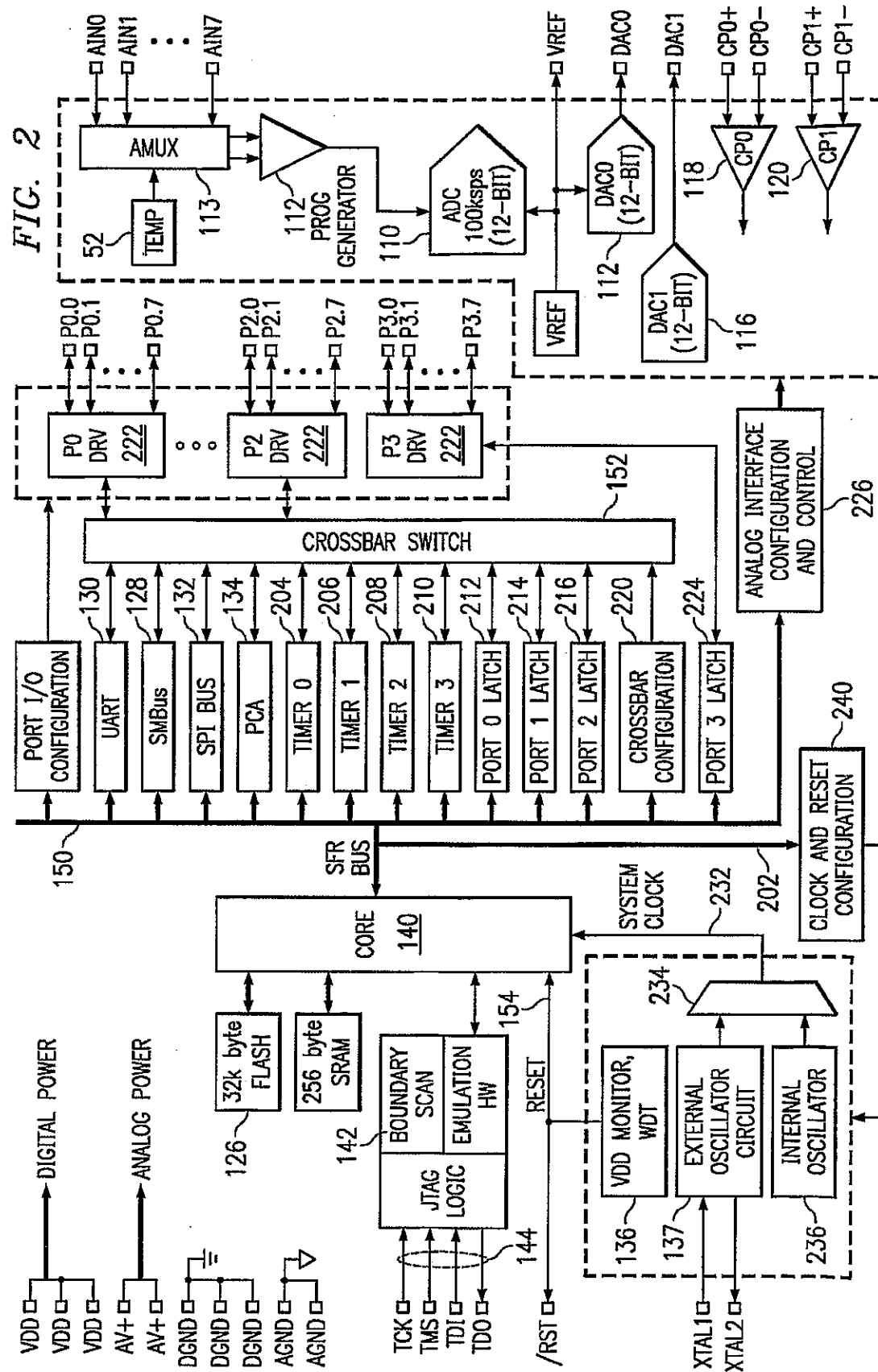






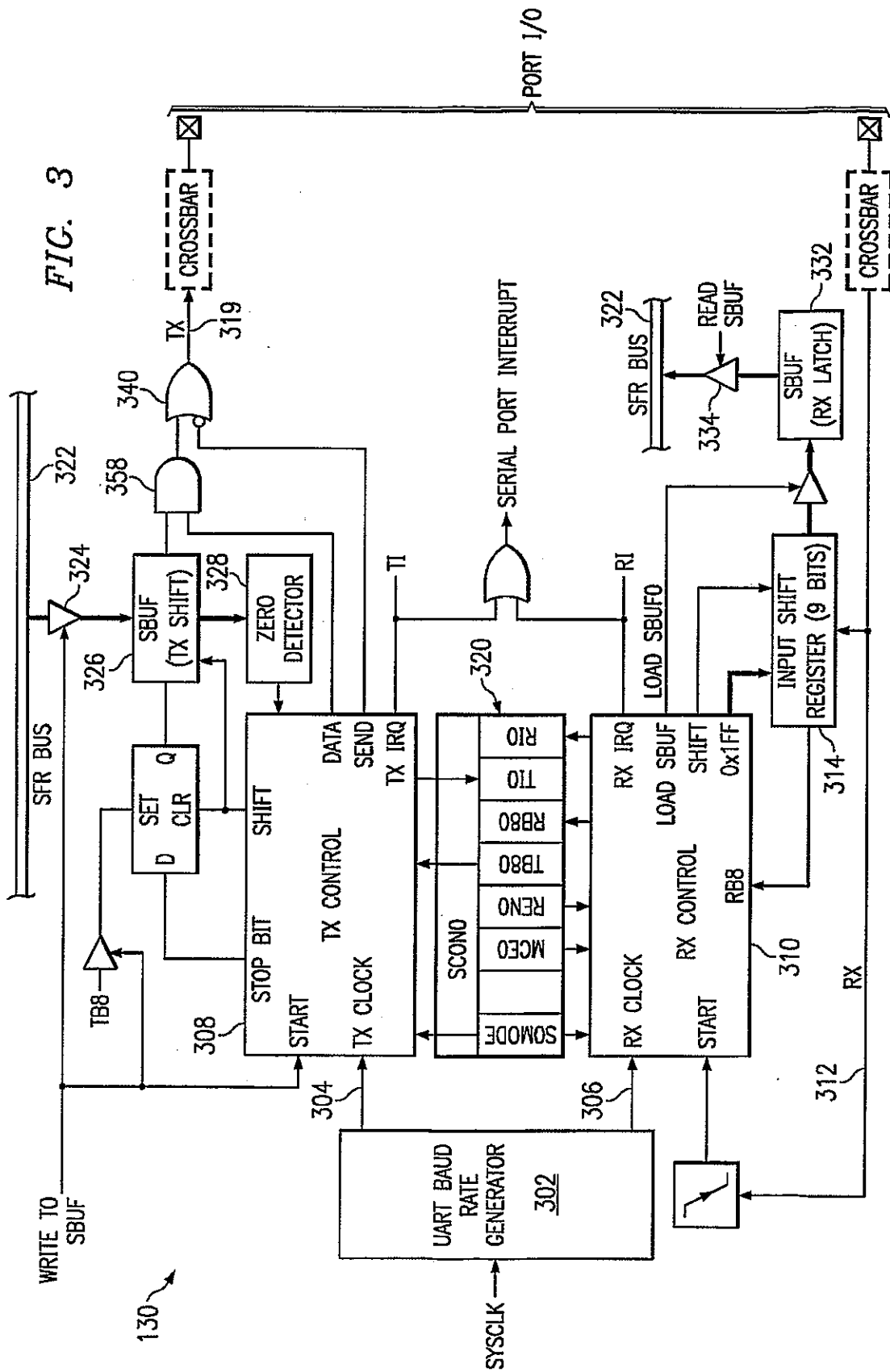


FIG. 3A

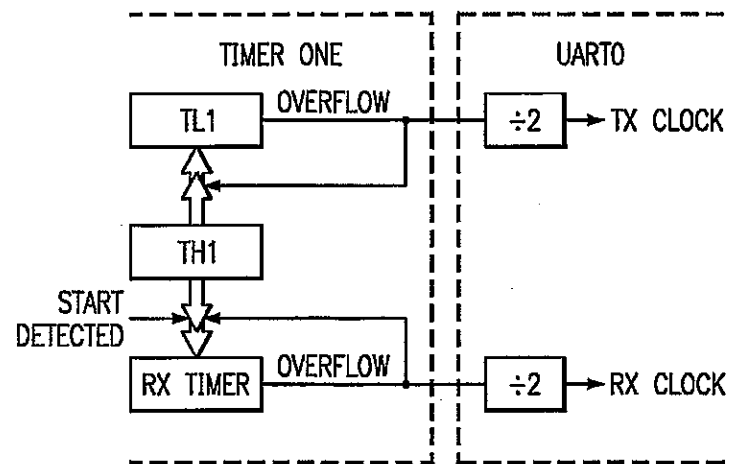


FIG. 4

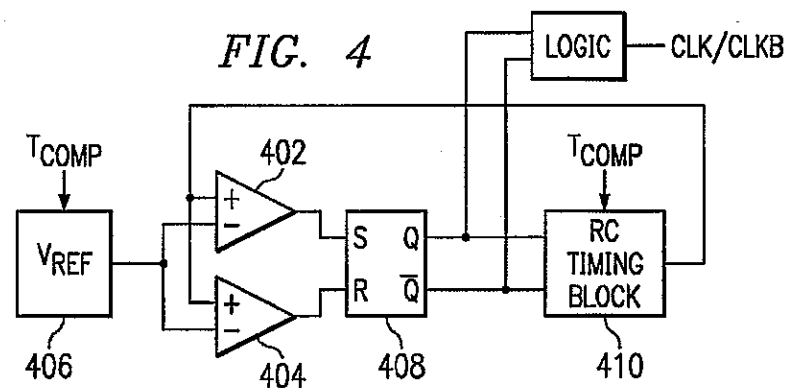


FIG. 5

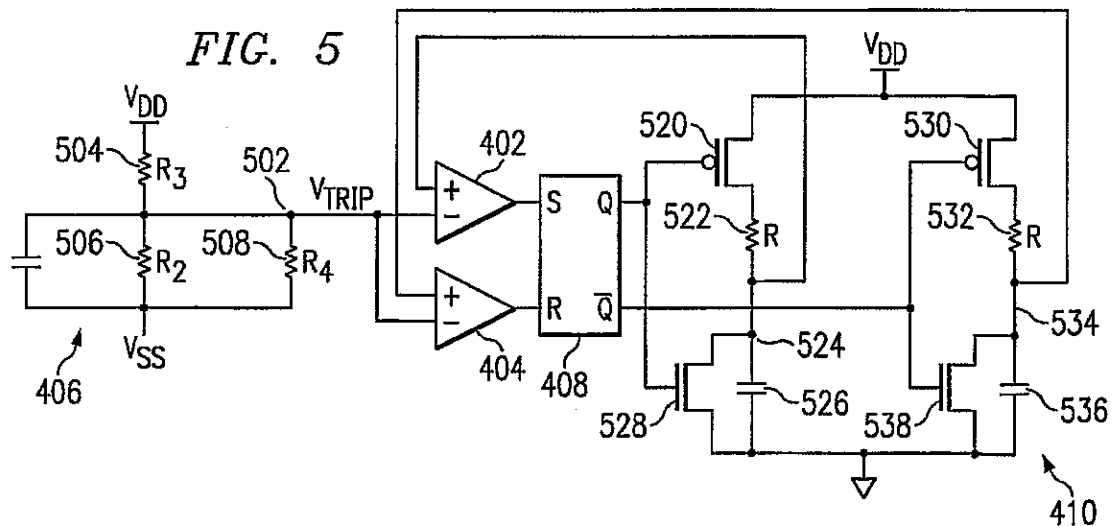


FIG. 6

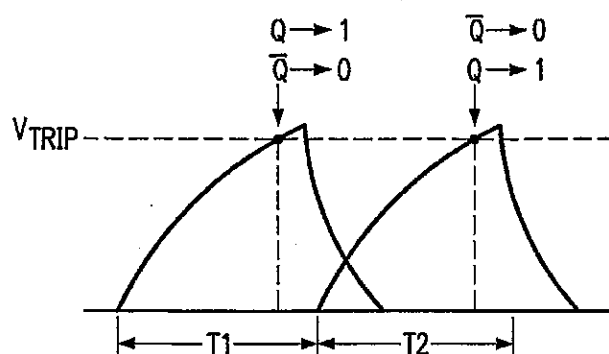


FIG. 7

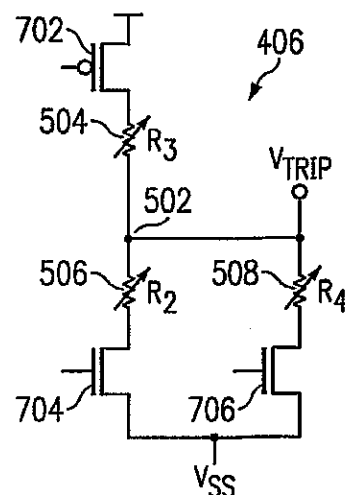


FIG. 8

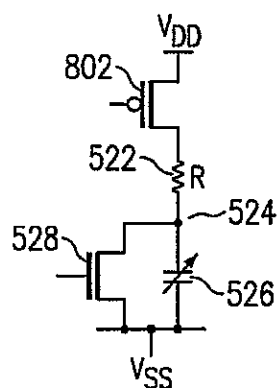


FIG. 9

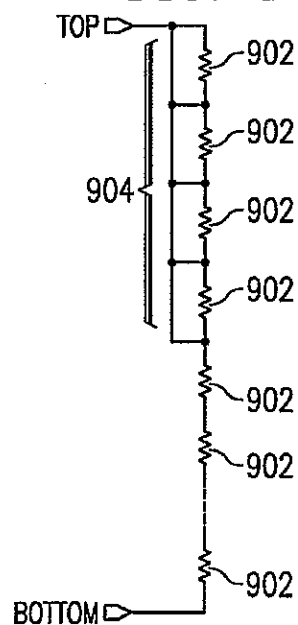


FIG. 10

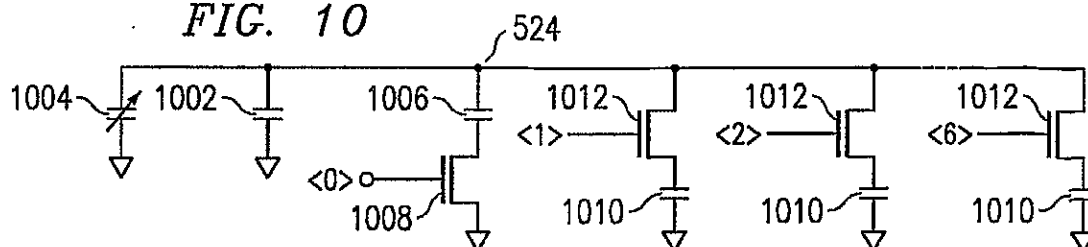


FIG. 11

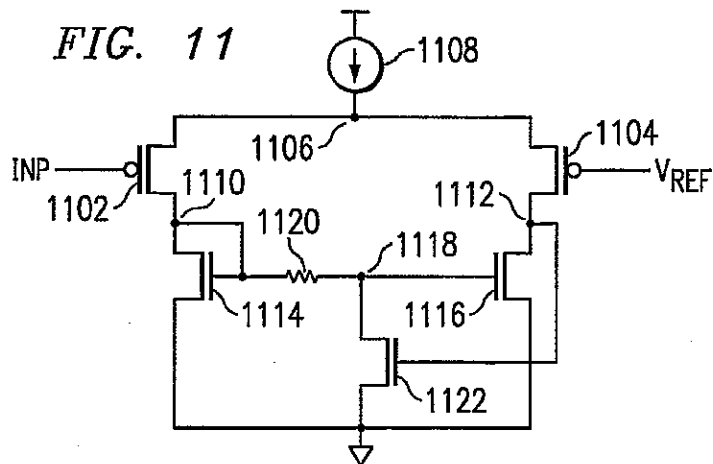


FIG. 12

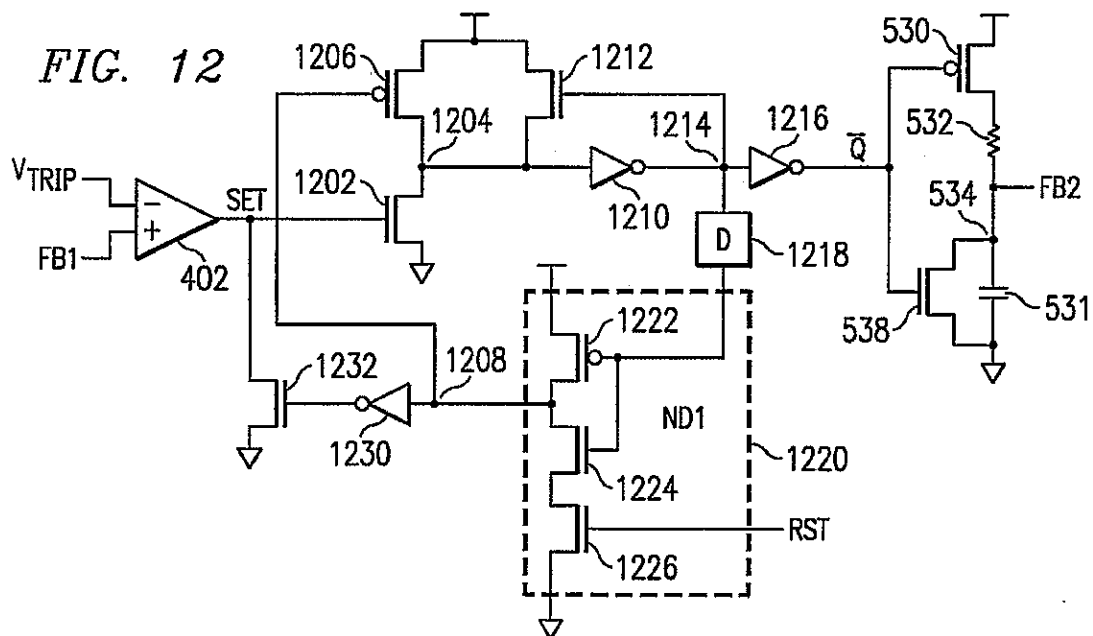


FIG. 13

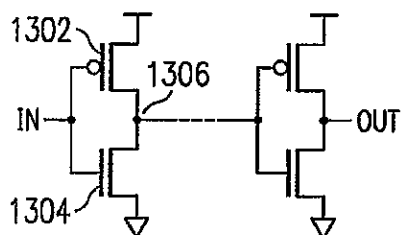
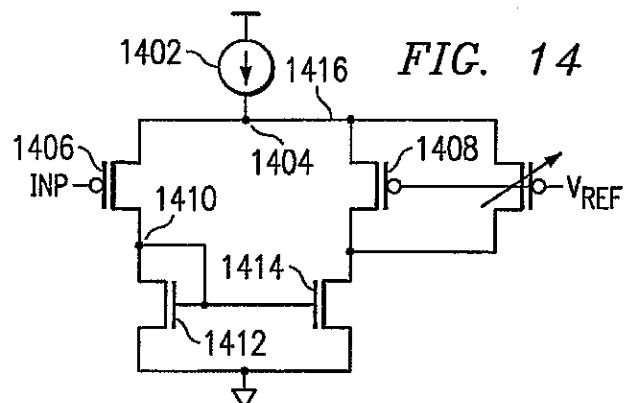


FIG. 14



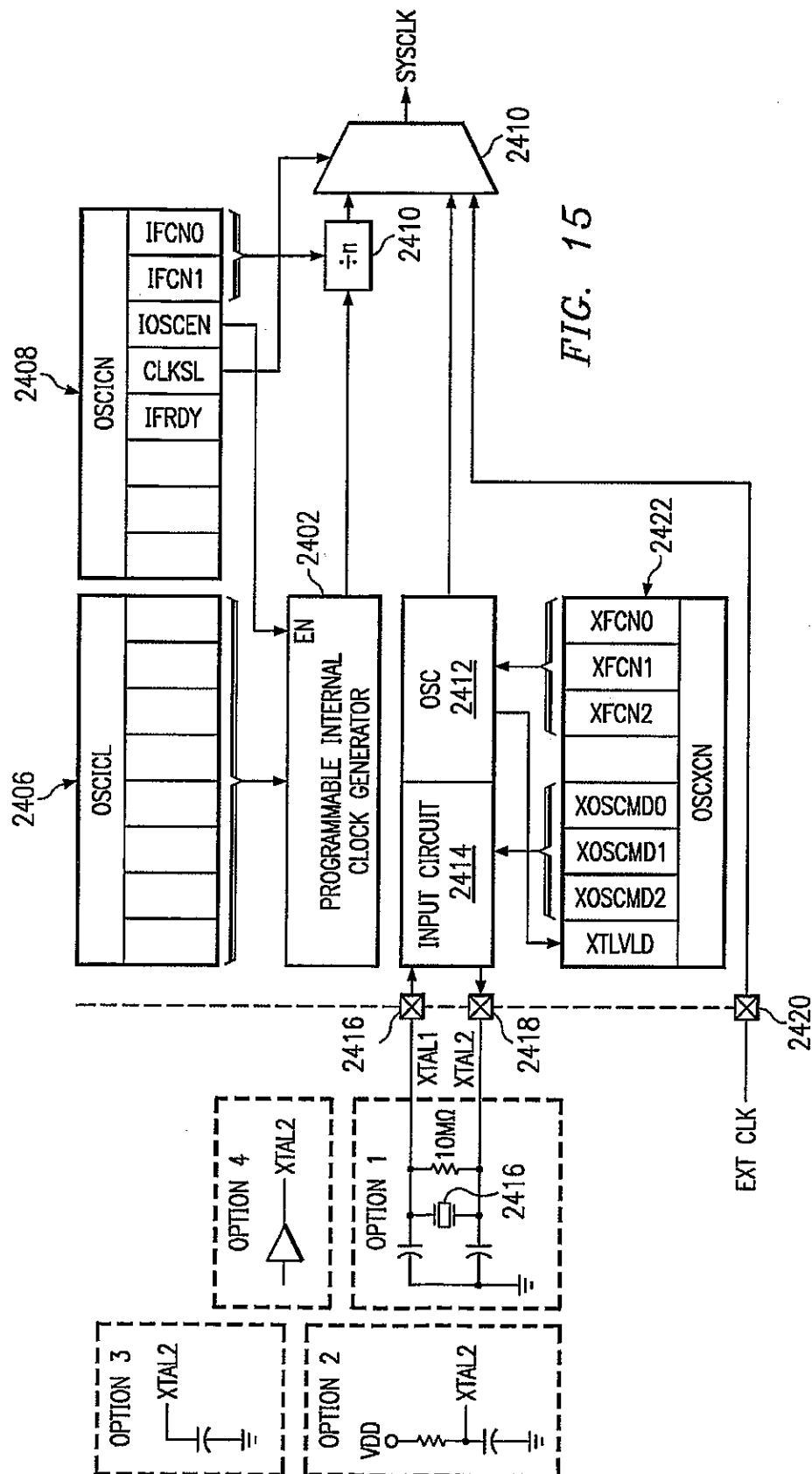


FIG. 16

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RESET VALUE VARIABLE SFR ADDRESS: 0xB3
-								
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	

Bit7: UNUSED. Read=0. Write=don't care.
 Bits 6-0: OSCICL: Internal Oscillator Calibration Register.
 This register determines the internal oscillator period

FIG. 17

R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	RESET VALUE 00010100 SFR ADDRESS: 0xB2
-	-	-	IFRDY	CLKSL	IOSCEN	IFCN1	IFCN0	
BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	

Bits7-5: UNUSED. Read=000b, Write=don't care.
 Bit4: IFRDY: Internal Oscillator Frequency Ready Flag.
 0: Internal Oscillator is not running at programmed frequency.
 1: Internal Oscillator is running at programmed frequency.
 Bit3: CLKSL: System Clock Source Select Bit.
 0: SYSCLK derived from the Internal Oscillator, and scaled as per the IFCN bits.
 1: SYSCLK derived from the External Oscillator circuit.
 Bit2: IOSCEN: Internal Oscillator Enable Bit.
 0: Internal Oscillator Disabled.
 1: Internal Oscillator Enabled.
 Bits1-0: IFCN1-0: Internal Oscillator Frequency Control Bits.
 00: SYSCLK derived from Internal Oscillator divided by 8.
 01: SYSCLK derived from Internal Oscillator divided by 4.
 10: SYSCLK derived from Internal Oscillator divided by 2.
 11: SYSCLK derived from Internal Oscillator divided by 1.