A SILICON NITRIDE CAPPED SHALLOW TRENCH ISOLATION METHOD FOR FABRICATING SUB-MICRON DEVICES WITH BORDERLESS CONTACTS

ABSTRACT

An improved and new process for fabricating MOSFET's in shallow trench isolation (STI), with sub-quarter micron ground rules, includes a passivating trench cap layer of silicon nitride. The silicon nitride passivating trench cap is utilized in the formation of borderless or "unframed" electrical contacts, without reducing the poly to poly spacing. Borderless contacts are formed, wherein contact openings are etched in an interlevel dielectric (ILD) layer over both an active region (P-N junction) and an inactive trench isolation region. During the contact hole opening, a selective etch process is utilized which etches the ILD layer, while the protecting passivating silicon nitride trench cap layer remains intact protecting the P-N junction at the edge of trench region. Subsequent processing of conductive tungsten metal plugs are prevented from shorting by the passivating trench cap. This method of forming borderless contacts with a passivating trench cap in a partially recessed trench isolation scheme improves device reliability since it prevents electrically short circuiting of the P-N junction and lowers the overall diode leakage. Furthermore, the use of the silicon nitride trench cap protects the underlying STI trench oxide during subsequent cleaning process steps. In addition, the nitride cap protects the STI oxide from excessive recess formation and prevents the exposure of STI seams, in addition to minimizing transistor junction leakage.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)