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(54) Title: REGULATING A DATA TRANSFER TIME

(57) Abstract

A computer system (50) includes a bus (52), a first bus device (60), a core circuit (58) and a second circuit (54). The first bus device (60) is coupled to the bus (52) and adapted to furnish a first indication of data to a portion of a bus (52) beginning at a first clock cycle. The bus is capable of skewing the first indication to produce a second indication of the data at another portion of the bus (52) beginning at another clock cycle. The second circuit (54) is coupled to the bus (52) and is adapted to receive an indication of a selected latency time. The second circuit (54) is also adapted to transfer the data to the core circuit (58) in response to the second indication and regulate the transfer so that the circuit receives the data beginning at the selected latency time after the first clock cycle.

