

WAFER SCALE ACTIVE THERMAL INTERPOSER WITH THERMAL ISOLATION STRUCTURES

ABSTRACT OF THE DISCLOSURE

A system for testing circuits of an integrated circuit semiconductor wafer includes a tester system testing the circuits of the wafer and a test stack coupled to the tester system. The test stack includes a wafer probe for contacting a first surface of the wafer and for probing individual circuits of the circuits of the wafer, a wafer scale active thermal interposer layer operable to contact a second surface of the wafer and containing a plurality of thermal zones corresponding to a die layout of the wafer and further operable to selectively heat areas of the wafer. The thermal zones are thermally isolated using a plurality of thermal resistance structures disposed between the thermal zones.

FIG. 1