

CLAIMS

What is claimed is:

1. A method for fabricating an integrated circuit, the method comprising:
providing a sacrificial gate structure over a semiconductor substrate, wherein the sacrificial gate structure includes two spacers and sacrificial gate material between the two spacers;
recessing a portion of the sacrificial gate material between the two spacers;
etching upper regions of the two spacers while using the sacrificial gate material as a mask;
removing a remaining portion of the sacrificial gate material and exposing lower regions of the two spacers;
depositing a first metal between the lower regions of the two spacers; and
depositing a second metal between the upper regions of the two spacers.
2. The method of claim 1 wherein providing a sacrificial gate structure over a semiconductor substrate comprises providing the sacrificial gate structure including a hard mask over the sacrificial gate material and between the spacers, and wherein the method further comprises removing the hard mask and a portion of the spacers by planarization before recessing a portion of the sacrificial gate material between the two spacers.
3. The method of claim 1 wherein providing a sacrificial gate structure over a semiconductor substrate comprises providing the sacrificial gate structure including a hard mask over the sacrificial gate material and between the spacers, and wherein the method further comprises:
depositing a dielectric material over the sacrificial gate structure and the semiconductor substrate; and
removing the hard mask, a portion of the spacers, and a portion of the dielectric material by planarization before recessing a portion of the sacrificial gate material between the two spacers.

4. The method of claim 1 further comprising forming a cap over the second metal between the upper regions of the two spacers.

5. The method of claim 1 further comprising forming a high-k dielectric layer over the lower regions of the two spacers and over the semiconductor substrate between the two spacers, wherein depositing a first metal between the lower regions of the two spacers comprises depositing a first metal over the high-k dielectric layer.

6. The method of claim 1 wherein the two spacers are two first spacers, and wherein the method further comprises forming second spacers adjacent the upper regions of the two first spacers after depositing the first metal.

7. The method of claim 6 wherein forming second spacers adjacent the upper regions of the two first spacers comprises forming each of the second spacers with a tapered sidewall surface to define a trench therebetween with an upwardly expanding width.

8. The method of claim 1 wherein the two spacers are two first spacers, and wherein the method further comprises:

removing the two first spacers after depositing a first metal between the lower regions of the two spacers; and

forming two second spacers having lower regions adjacent the first metal, wherein the two second spacers have upper regions bounding an upper portion of a trench having an upwardly expanding width, wherein depositing a second metal between the upper regions of the two spacers comprises depositing a second metal between the upper regions of the two second spacers.

9. The method of claim 8 further comprising recessing the two second spacers to a depth below an upper surface of the second metal after depositing the second metal between the upper regions of the two spacers.

10. The method of claim 1 wherein depositing a first metal between the lower regions of the two spacers comprises depositing a workfunction metal between the lower regions of the two spacers, and wherein depositing a second metal between the upper regions of the two spacers comprises depositing a fill metal between the upper regions of the two spacers.

11. A method for fabricating an integrated circuit, the method comprising:
forming two spacers over a semiconductor substrate, wherein the two spacers bound a trench having a lower portion, an upper portion, a boundary between the lower portion and the upper portion, and a top; and wherein the lower portion has a first width, the upper portion has a second width at the boundary greater than the first width, and the upper portion has an increasing width from the boundary to the top;
depositing a first metal in the lower portion of the trench; and
depositing a second metal in the upper portion of the trench.

12. The method of claim 11 further comprising forming a cap over the second metal in the upper portion of the trench.

13. The method of claim 11 further comprising forming a high-k dielectric layer in the trench, wherein depositing a first metal in the lower portion of the trench comprises depositing a first metal over the high-k dielectric layer.

14. The method of claim 11 further comprising:
forming a sacrificial gate over the semiconductor substrate before forming the two spacers;
recessing a first portion of the sacrificial gate to expose sidewalls of the two spacers, wherein forming two spacers over a semiconductor substrate comprises etching the two spacers using the sacrificial gate as a mask; and
removing a remaining portion of the sacrificial gate to form the trench between the two spacers after etching the two spacers.

15. The method of claim 11 wherein the two spacers are two first spacers, wherein each first spacer has an upper region corresponding to the upper portion of the trench, and wherein the method further comprises forming a second spacer adjacent the upper region of each first spacer to provide the upper portion of the trench with a reduced width after depositing the first metal in the lower portion of the trench.

16. The method of claim 15 wherein forming a second spacer adjacent the upper region of each first spacer comprises providing the upper portion of the trench with a reduced width at the boundary substantially the same as the first width, and wherein the reduced width increases from the boundary to the top of the trench.

17. The method of claim 11 wherein the two spacers are two first spacers, and wherein the method further comprises:

removing the two first spacers after depositing a first metal in the lower portion of the trench; and

forming two second spacers having lower regions adjacent the first metal, wherein the two second spacers have upper regions bounding the upper portion of the trench, and wherein the upper portion of the trench maintains an increasing width from the boundary to the top.

18. The method of claim 17 further comprising recessing the two second spacers to a depth below an upper surface of the second metal after depositing the second metal in the upper portion of the trench.

19. The method of claim 18 further comprising forming a cap over the second metal and the two second spacers.

20. An integrated circuit comprising
a semiconductor substrate; and

a metal gate electrode structure overlying the semiconductor substrate and including a workfunction metal having a first width and a fill metal overlying the workfunction metal and having a second width greater than the first width.

What is claimed is:

1. A method for fabricating an integrated circuit, the method comprising: providing a sacrificial gate structure over a semiconductor substrate, wherein the sacrificial gate structure includes two spacers having upper regions bounding an upper gate space and lower regions bounding a lower gate space, and wherein the sacrificial gate structure includes sacrificial gate material between the two spacers; recessing a portion of the sacrificial gate material between the two spacers; etching the upper regions of the two spacers while using the sacrificial gate material as a mask and defining a widened upper gate space; removing a remaining portion of the sacrificial gate material and exposing the lower regions of the two spacers; filling the lower gate space with a first metal; and depositing a second metal in the widened upper gate space.
2. The method of claim 1 wherein providing the sacrificial gate structure over the semiconductor substrate comprises providing the sacrificial gate structure including a hard mask over the sacrificial gate material and between the spacers, and wherein the method further comprises removing the hard mask and a portion of the spacers by planarization before recessing the portion of the sacrificial gate material between the two spacers.
3. The method of claim 1 wherein providing the sacrificial gate structure over the semiconductor substrate comprises providing the sacrificial gate structure including a hard mask over the sacrificial gate material and between the spacers, and wherein the method further comprises: depositing a dielectric material over the sacrificial gate structure and the semiconductor substrate; and removing the hard mask, a portion of the spacers, and a portion of the dielectric material by planarization before recessing a portion of the sacrificial gate material between the two spacers.
4. The method of claim 1 further comprising forming a cap over the second metal between the upper regions of the two spacers.
5. The method of claim 1 further comprising forming a high-k dielectric layer over the lower regions of the two spacers and over the semiconductor substrate between the two spacers after removing the remaining portion of the sacrificial gate material and exposing the lower regions of the two spacers, wherein filling the lower gate space with the first metal comprises depositing the first metal over the high-k dielectric layer.
6. The method of claim 1 wherein the two spacers are two first spacers, and wherein the method further comprises forming second spacers adjacent the upper regions of the two first spacers after filling the lower gate space with the first metal.
7. The method of claim 6 wherein forming second spacers adjacent the upper regions of the two first spacers comprises forming the second spacers after etching the upper regions of the two spacers.

8. The method of claim 1 wherein the two spacers are two first spacers, and wherein the method further comprises: removing the two first spacers after filling the lower gate space with the first metal; and forming two second spacers having lower regions adjacent the first metal, wherein the two second spacers have upper regions bounding an upper portion of a trench having an upwardly expanding width, wherein depositing the second metal in the widened upper gate space comprises depositing the second metal between the upper regions of the two second spacers.

9. The method of claim 8 further comprising recessing the two second spacers to a depth below an upper surface of the second metal after depositing the second metal between the upper regions of the two spacers.

10. The method of claim 1 wherein filling the lower gate space with the first metal comprises depositing a workfunction metal between the lower regions of the two spacers, and wherein depositing the second metal in the widened upper gate space comprises filling the widened upper gate space with a fill metal.

11. The method of claim 1 wherein the two spacers are two first spacers, and wherein the method further comprises: removing the two first spacers after filling the lower gate space with the first metal; and forming two second spacers having lower regions adjacent the first metal, wherein the two second spacers have upper regions bounding the upper widened gate space.

12. The method of claim 11 further comprising recessing the two second spacers to a depth below an upper surface of the second metal after depositing the second metal in the widened upper gate space.

13. The method of claim 12 further comprising forming a cap over the second metal and the two second spacers.

14. The method of claim 1 wherein filling the lower gate space with the first metal comprises depositing the first metal along the upper regions of the two spacers, wherein the first metal defines a void in the upper gate space, and wherein the method further comprises removing the first metal from the upper gate space.

15. A method for fabricating an integrated circuit, the method comprising: forming two first spacers over a semiconductor substrate, wherein the two spacers bound a trench having a lower portion, an upper portion, a boundary between the lower portion and the upper portion, and a top; wherein the lower portion has a first width, the upper portion has a second width at the boundary greater than the first width, and the upper portion has an increasing width from the boundary to the top, and wherein each first spacer has an upper region corresponding to the upper portion of the trench; depositing a first metal in the lower portion of the trench; forming a second spacer adjacent the upper region of each first spacer to provide the upper portion of the trench with a reduced width after depositing the first metal in the lower portion of the trench; and depositing a second metal in the upper portion of the trench.

16. The method of claim 15 further comprising forming a cap over the second metal in the upper portion of the trench.

17. The method of claim 15 further comprising forming a high-k dielectric layer in the trench, wherein depositing a first metal in the lower portion of the trench comprises depositing a first metal over the high-k dielectric layer.

18. The method of claim 15 further comprising: forming a sacrificial gate over the semiconductor substrate before forming the two spacers; recessing a first portion of the sacrificial gate to expose sidewalls of the two spacers, wherein forming two spacers over a semiconductor substrate comprises etching the two spacers using the sacrificial gate as a mask; and removing a remaining portion of the sacrificial gate to form the trench between the two first spacers after etching the two first spacers.

19. The method of claim 15 wherein forming the second spacer adjacent the upper region of each first spacer comprises providing the upper portion of the trench with a reduced width at the boundary substantially the same as the first width, and wherein the reduced width increases from the boundary to the top of the trench.

20. An integrated circuit comprising: a semiconductor substrate; first spacers overlying the semiconductor substrate and having base portions with inner surfaces distanced from one another by a first distance and upper portions having inner surfaces distanced from one another by a second distance greater than the first distance; second spacers overlying the base portions of the first spacers and adjacent the upper portions of the first spacers; and a metal gate electrode structure overlying the semiconductor substrate and including a workfunction metal between the base portions of the first spacers and a fill metal overlying the workfunction metal and between the second spacers.

21. An integrated circuit fabricated in accordance with any one of the claims 1-19.