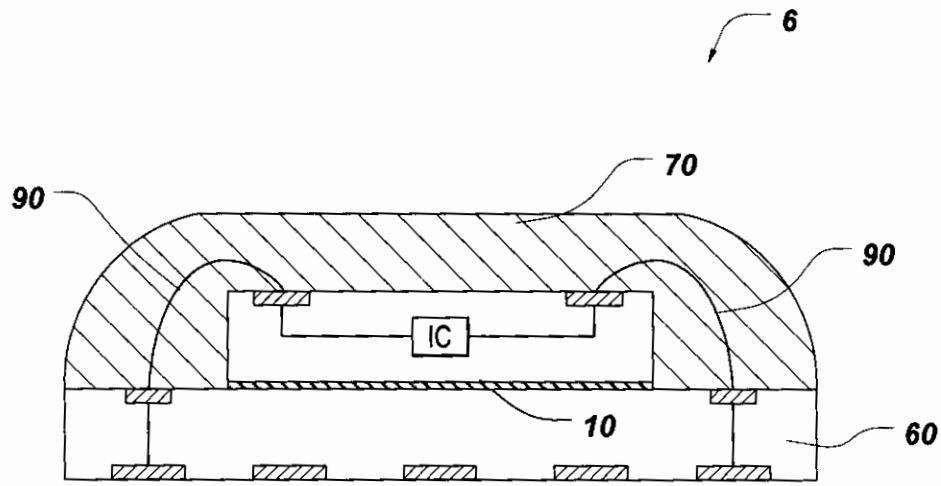


Fig. 1A
(Prior Art)

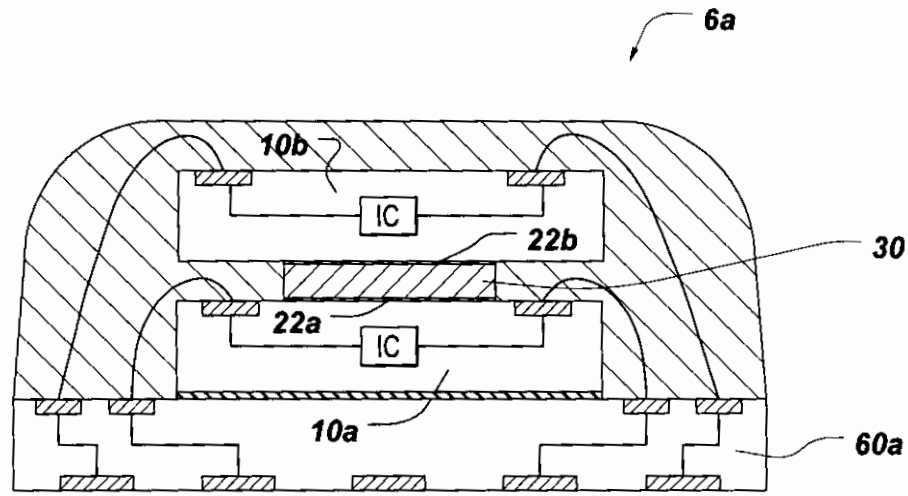


Fig. 1B
(Prior Art)

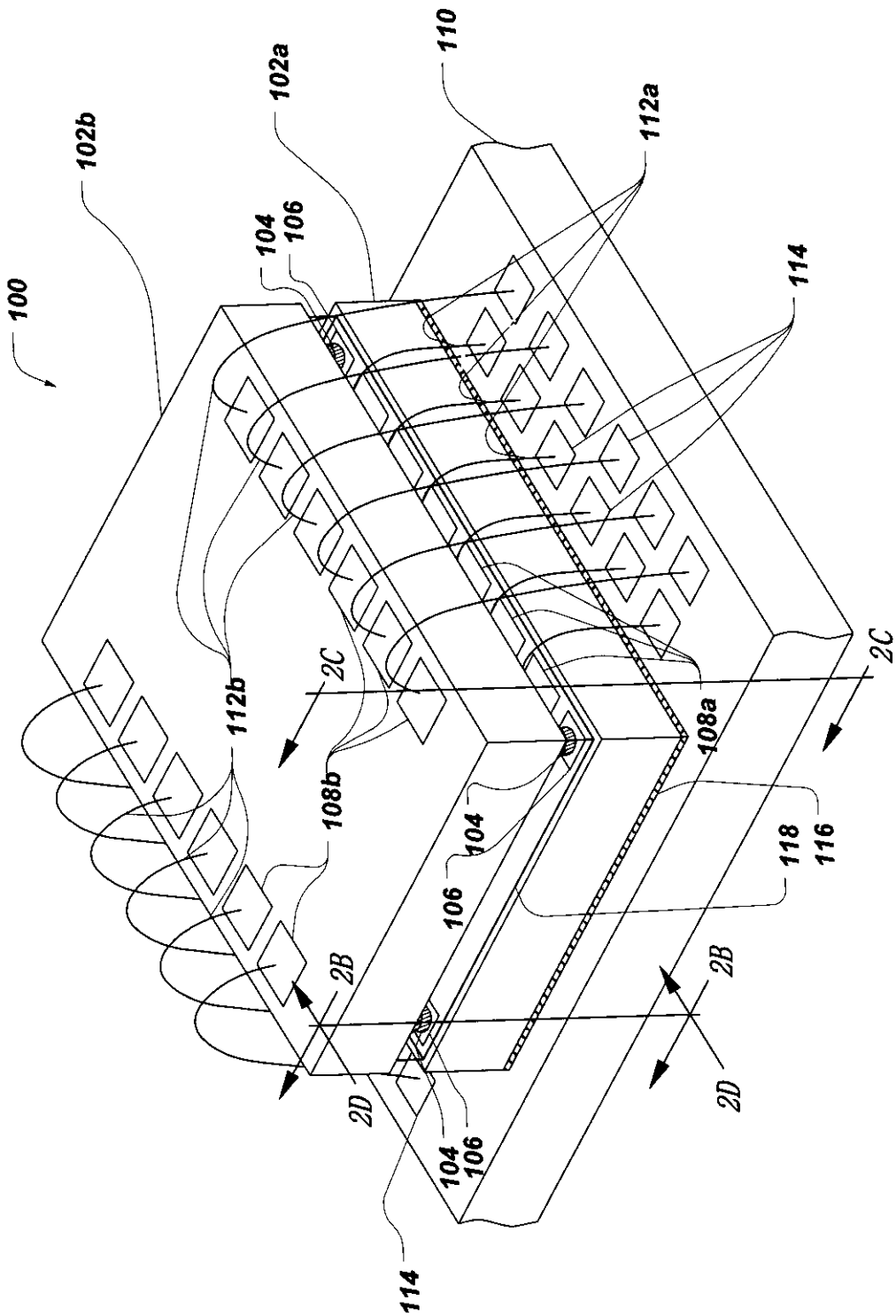

100
102b
102a
110
112a
104
106
114
112b
2C
108b
108a
104
106
118
116
2B
2D
114

Fig. 2A

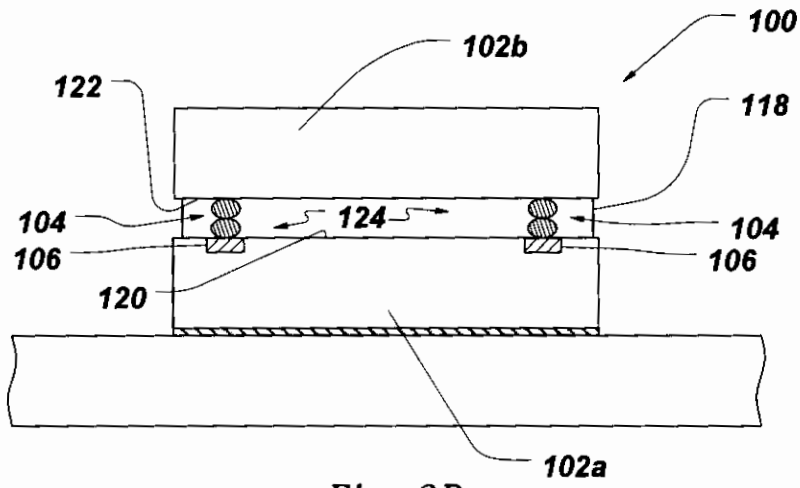


Fig. 2B

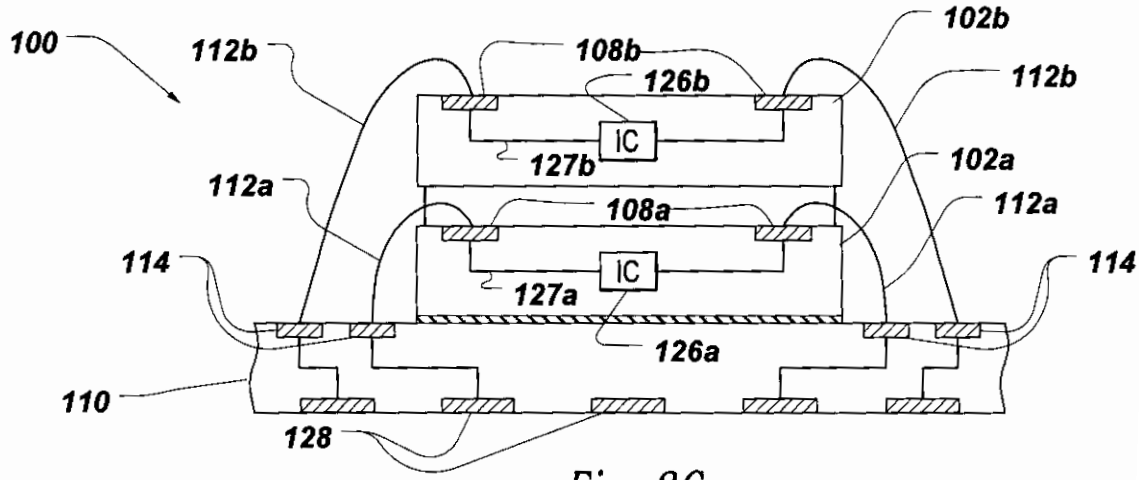


Fig. 2C

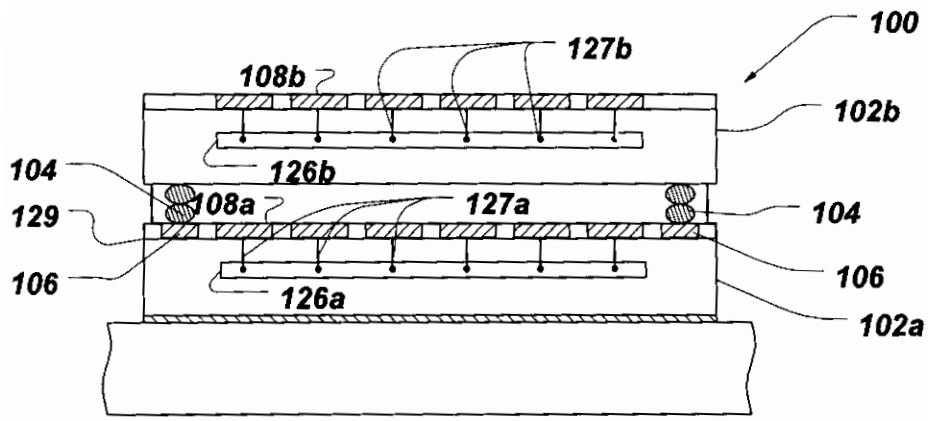


Fig. 2D

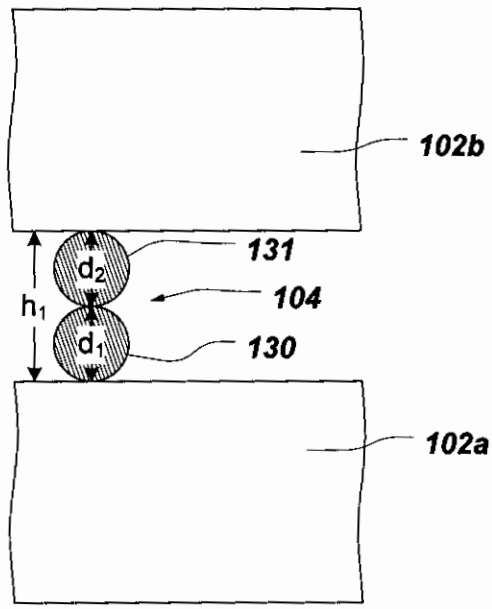


Fig. 3A

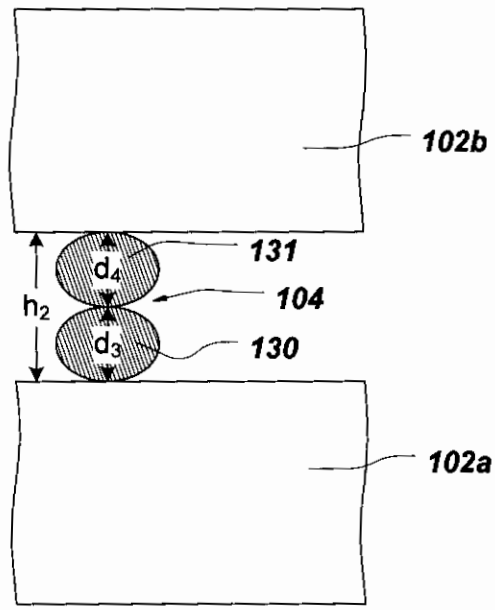


Fig. 3B

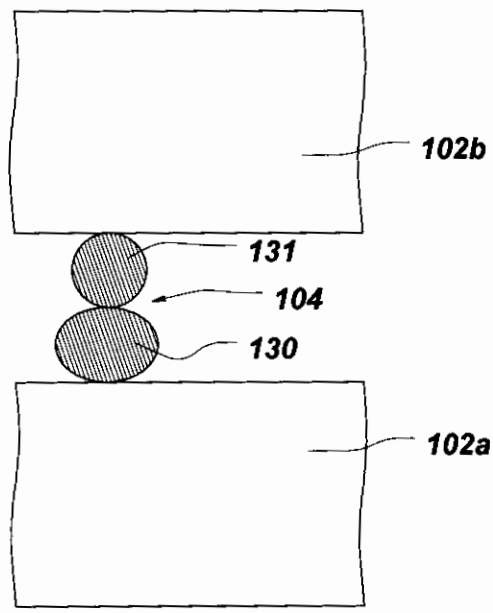


Fig. 3C

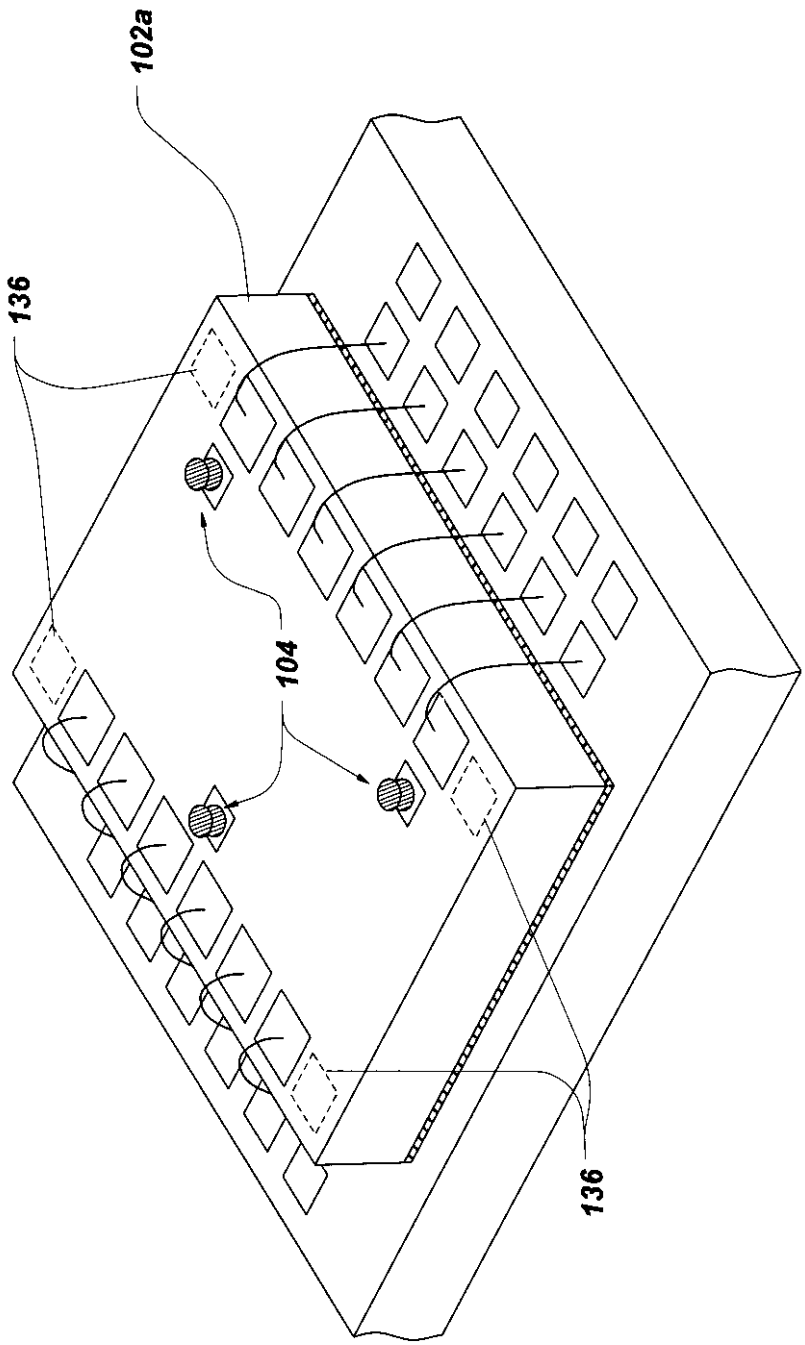


Fig. 4

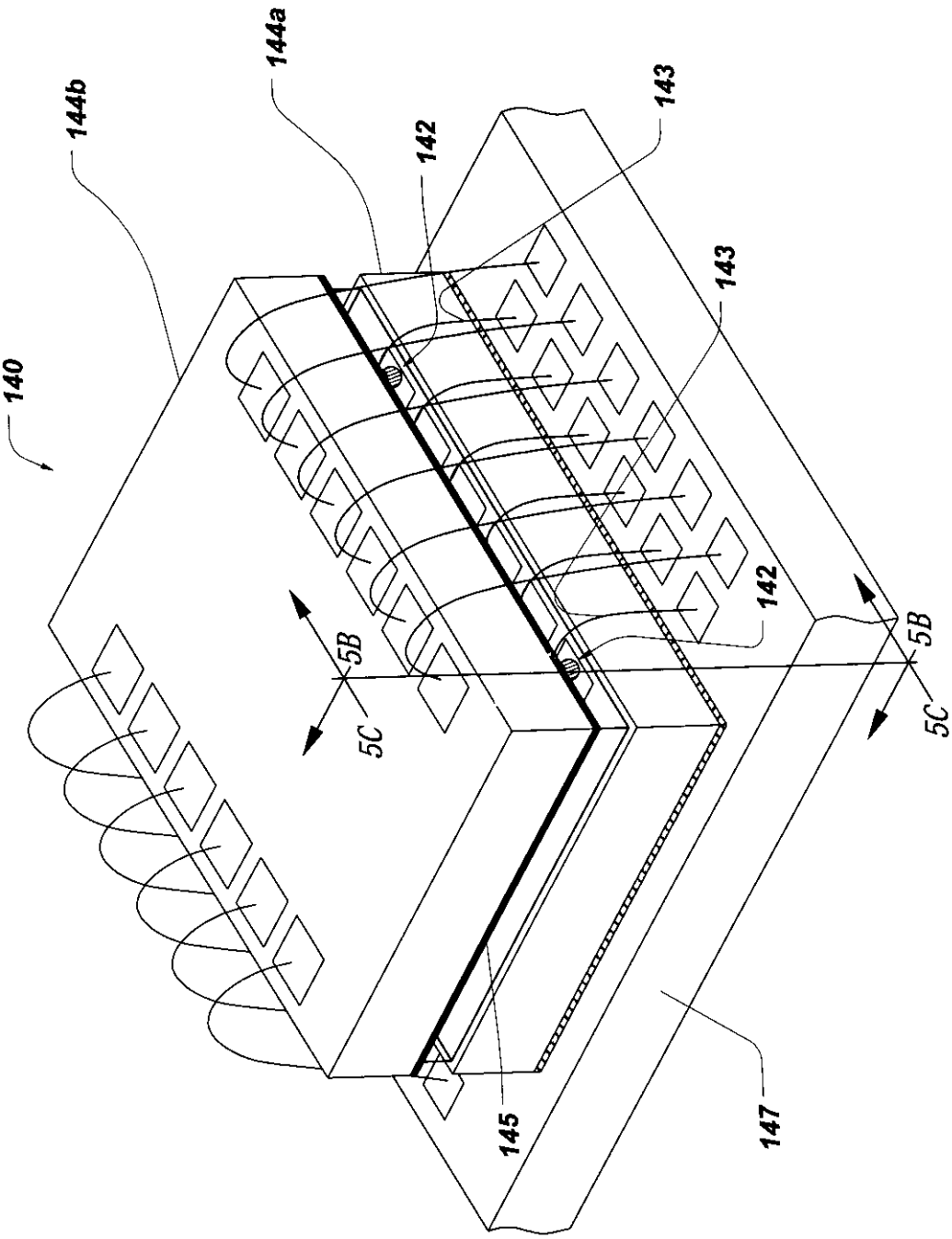


Fig. 5A

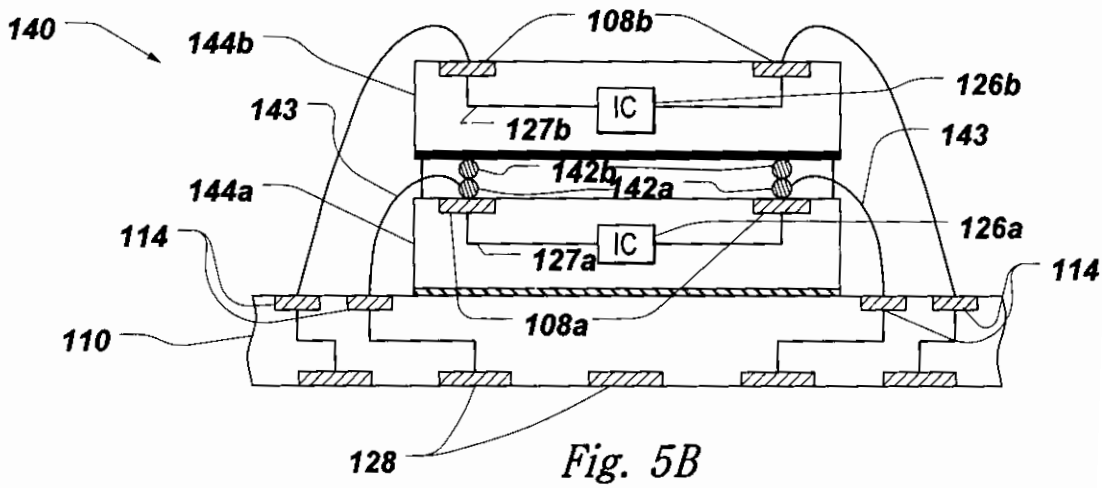

140
144b
108b
126b
143
IC
127b
143
142b
142a
144a
114
IC
126a
127a
114
108a
110
128

Fig. 5B

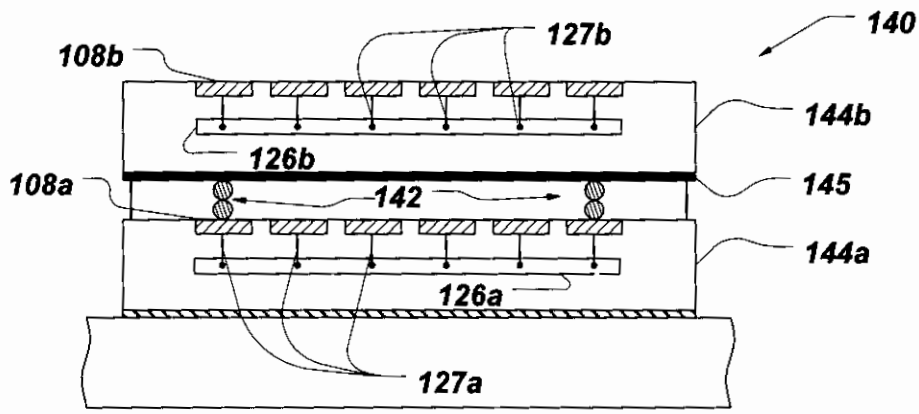

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126b
145
108a
142
144a
126a
127a

Fig. 5C

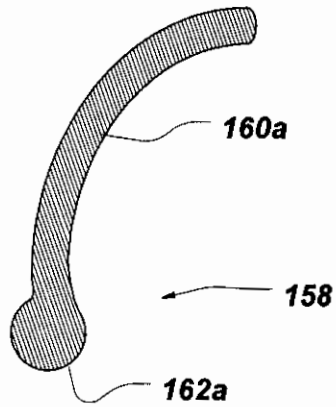


Fig. 6A

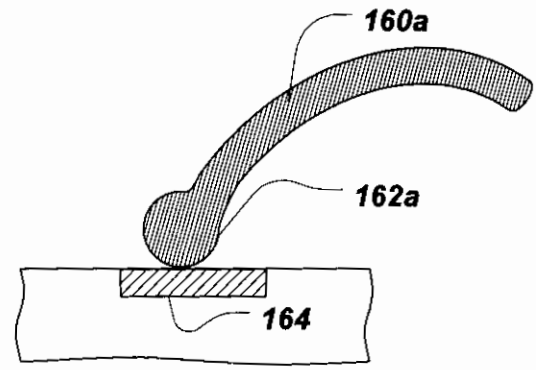


Fig. 6B

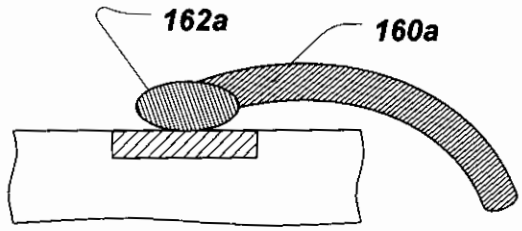


Fig. 6C

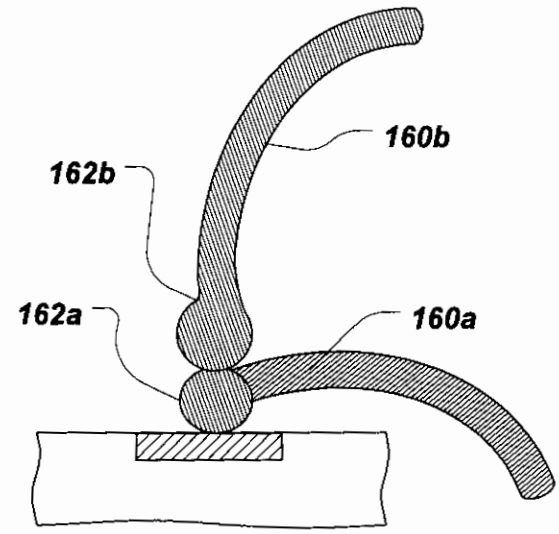


Fig. 6D

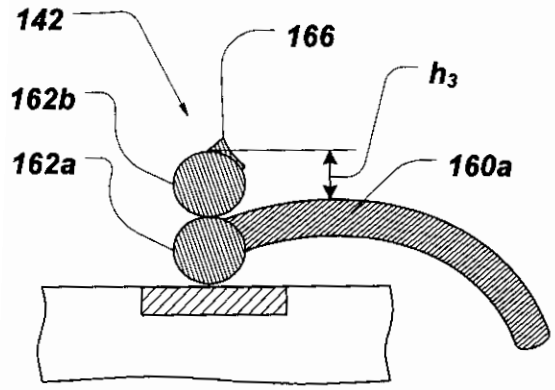


Fig. 6E

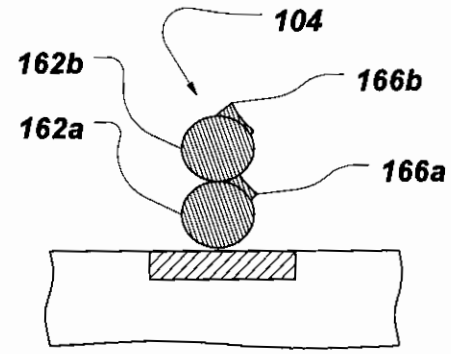


Fig. 6F

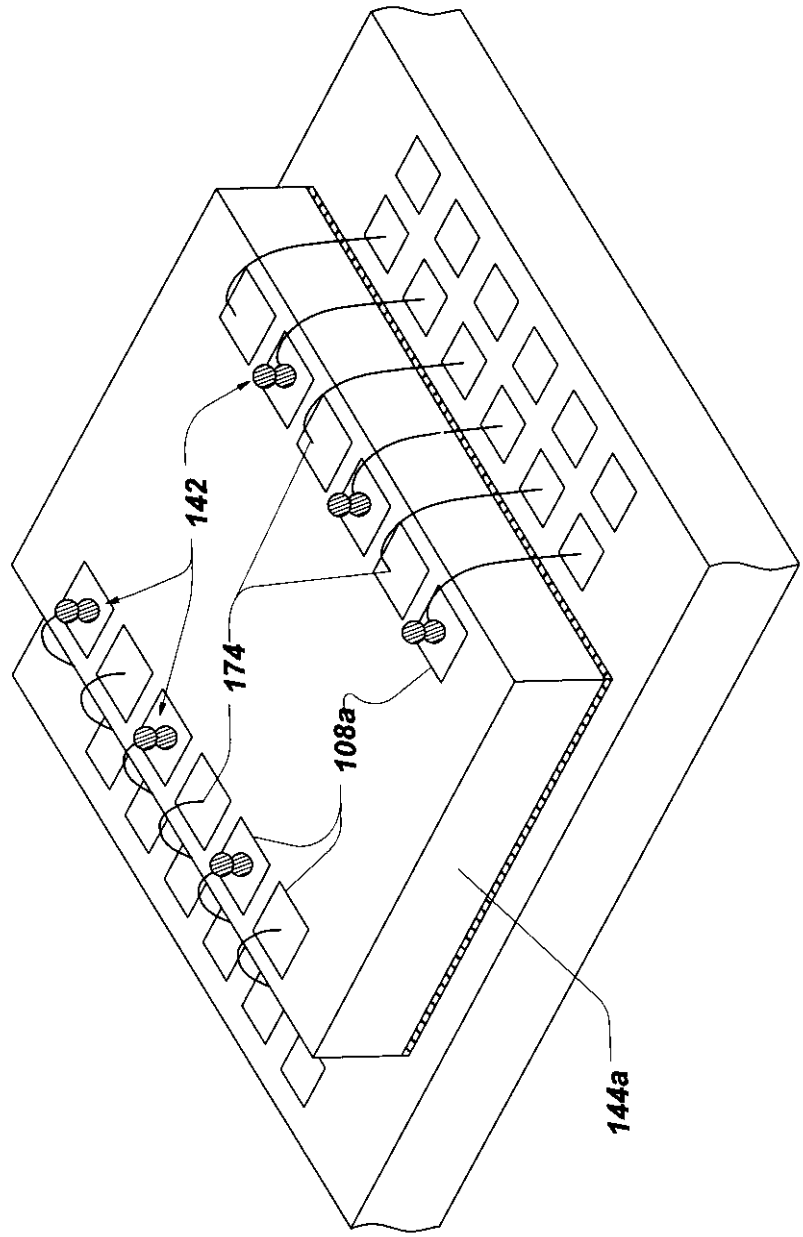


Fig. 7

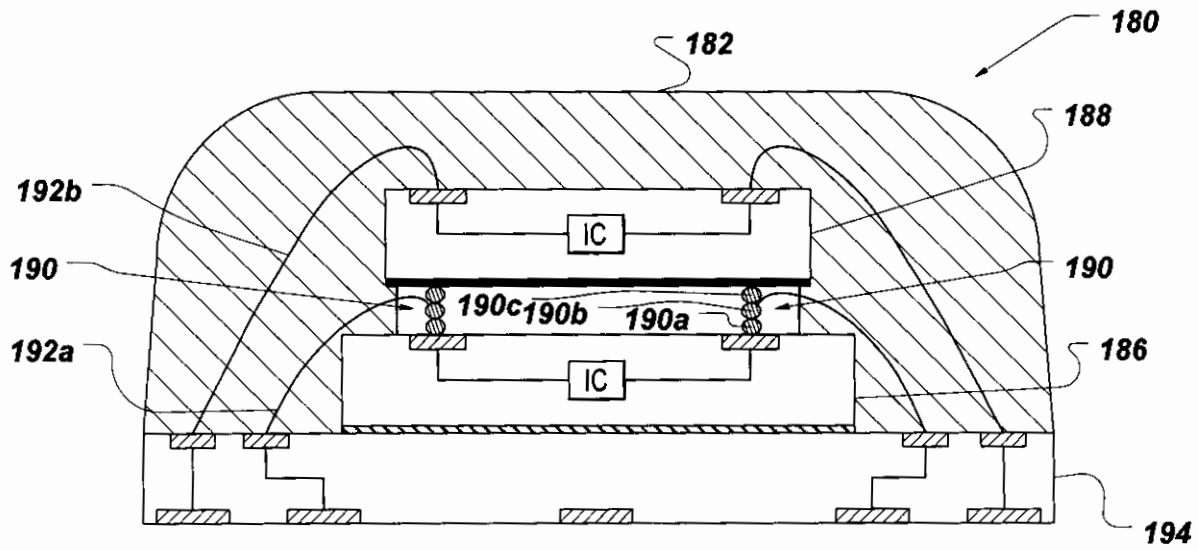

180
182
188
192b
190
190c
190b
190a
190
192a
186
IC
IC
194

Fig. 8

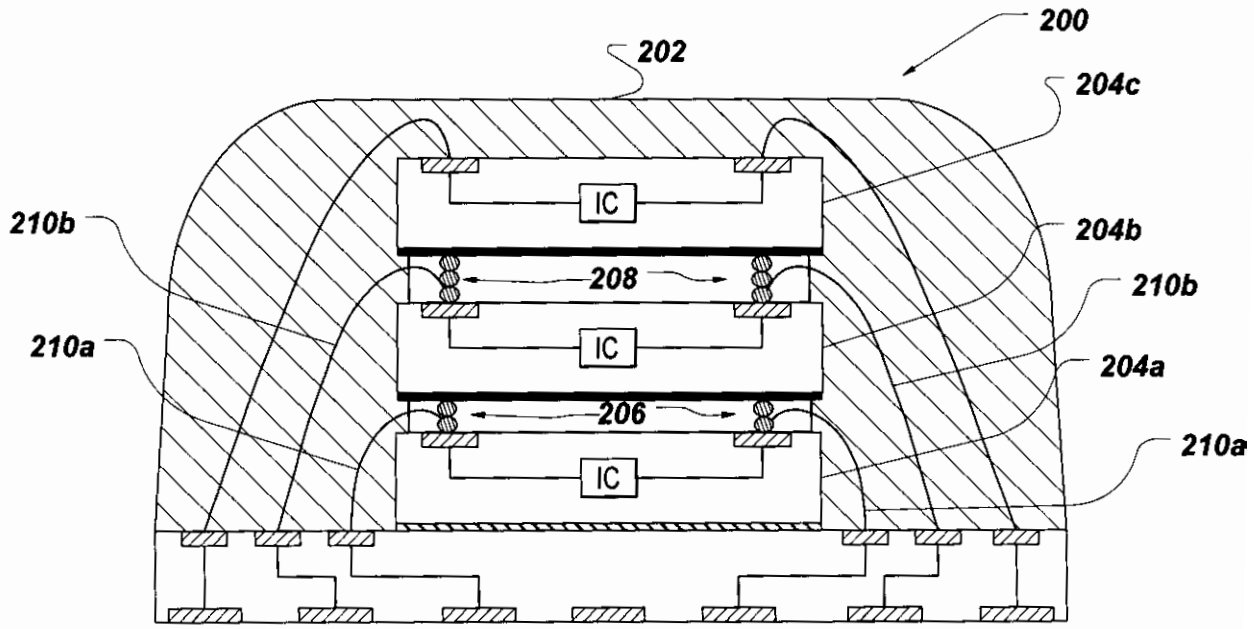

200
202
204c
210b
204b
208
210b
210a
204a
206
210a
IC
IC
IC

Fig. 9

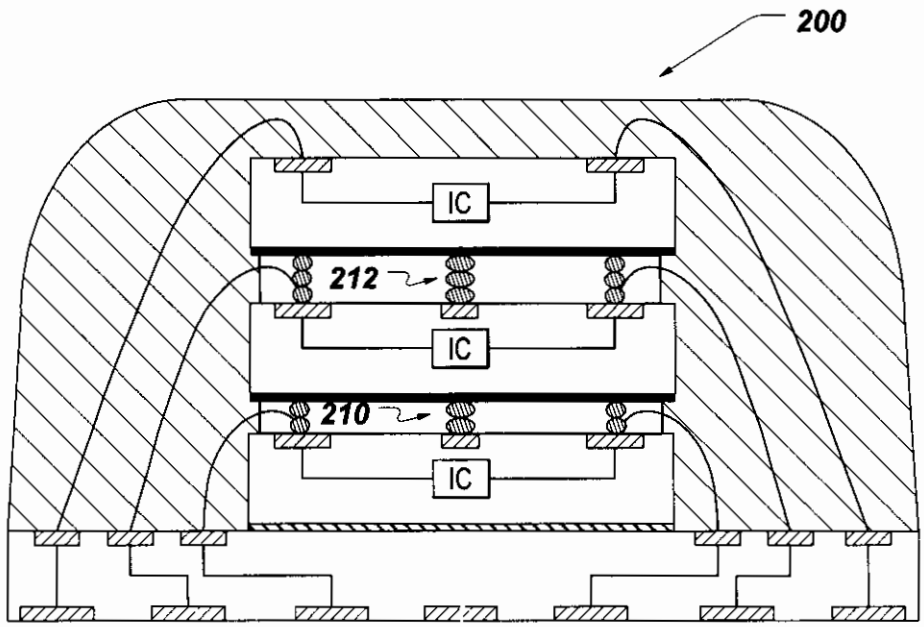

200
IC
212
IC
210
IC

Fig. 10

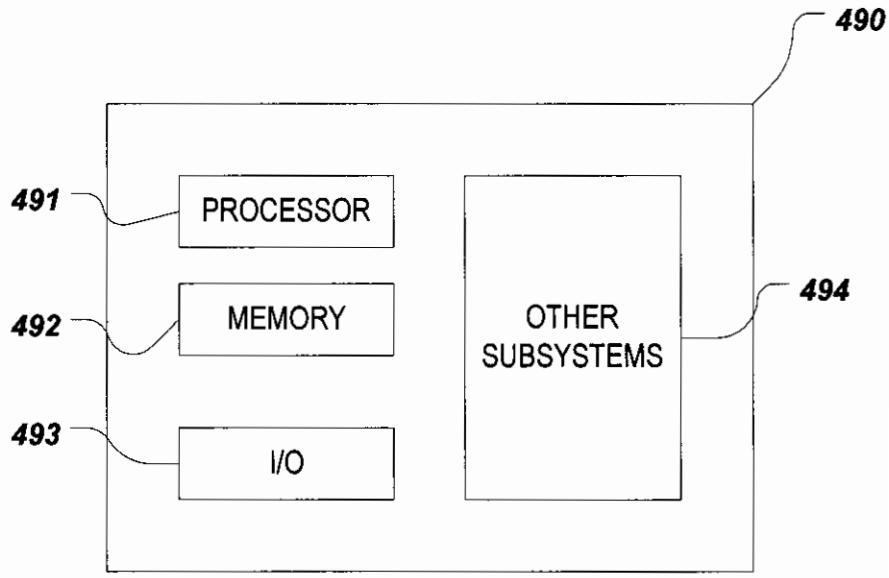

490
491
PROCESSOR
492
MEMORY
493
I/O
OTHER SUBSYSTEMS
494

Fig. 11