4 DEC 2005

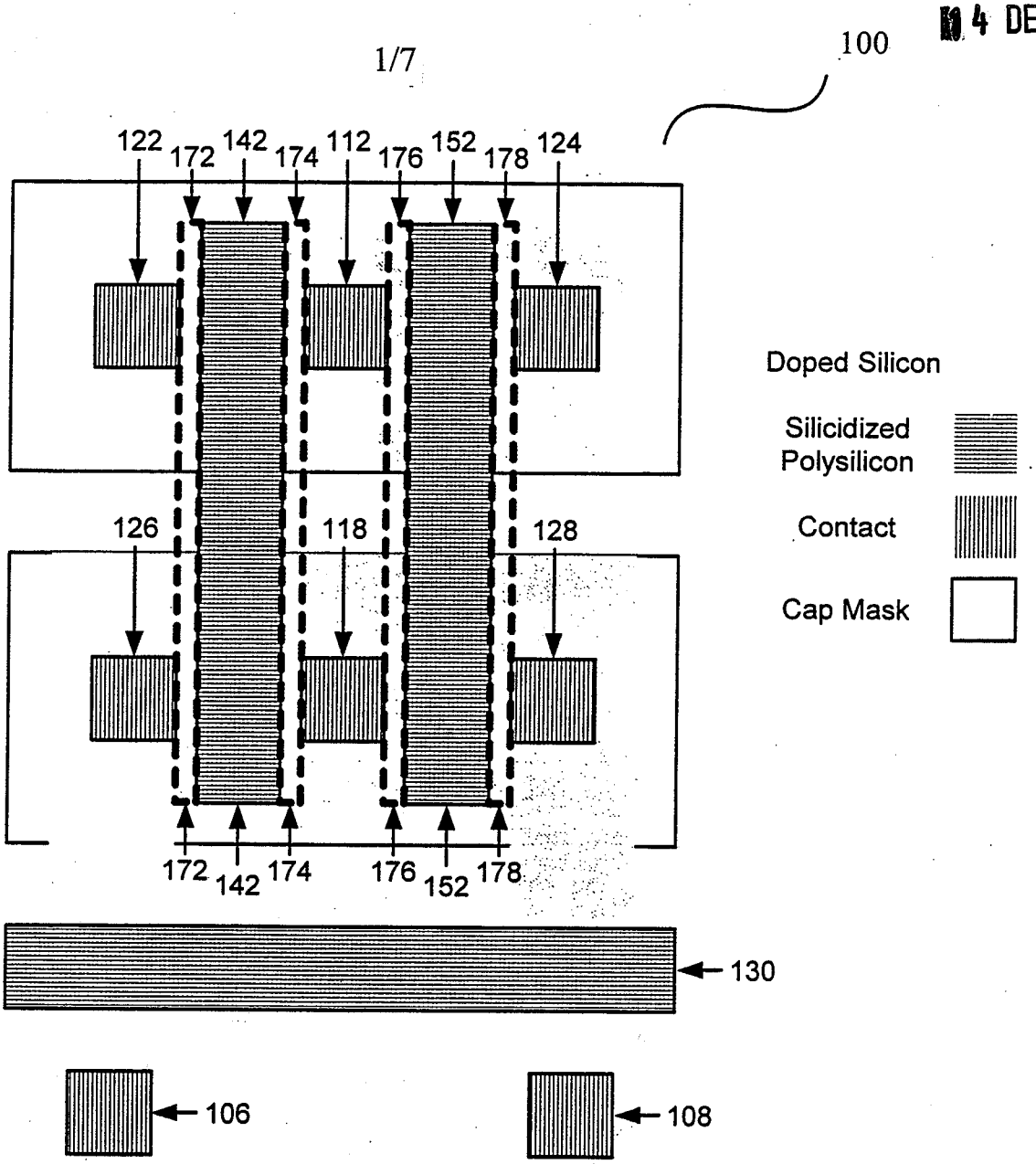


FIGURE 1

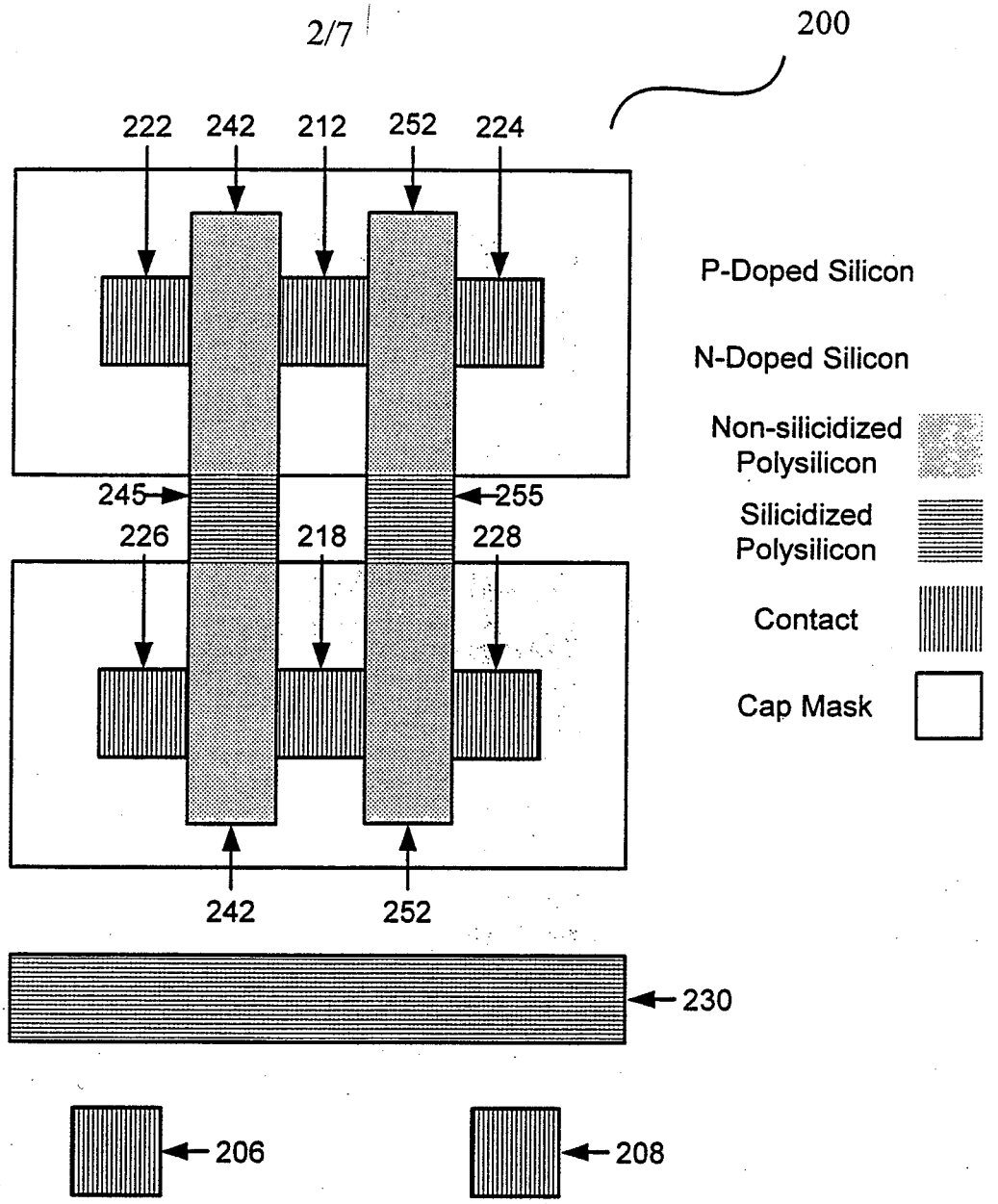

200
222
242
212
252
224
245
255
226
218
228
242
252
230
206
208
P-Doped Silicon
N-Doped Silicon
Non-silicidized Polysilicon
Silicidized Polysilicon
Contact
Cap Mask

FIGURE 2

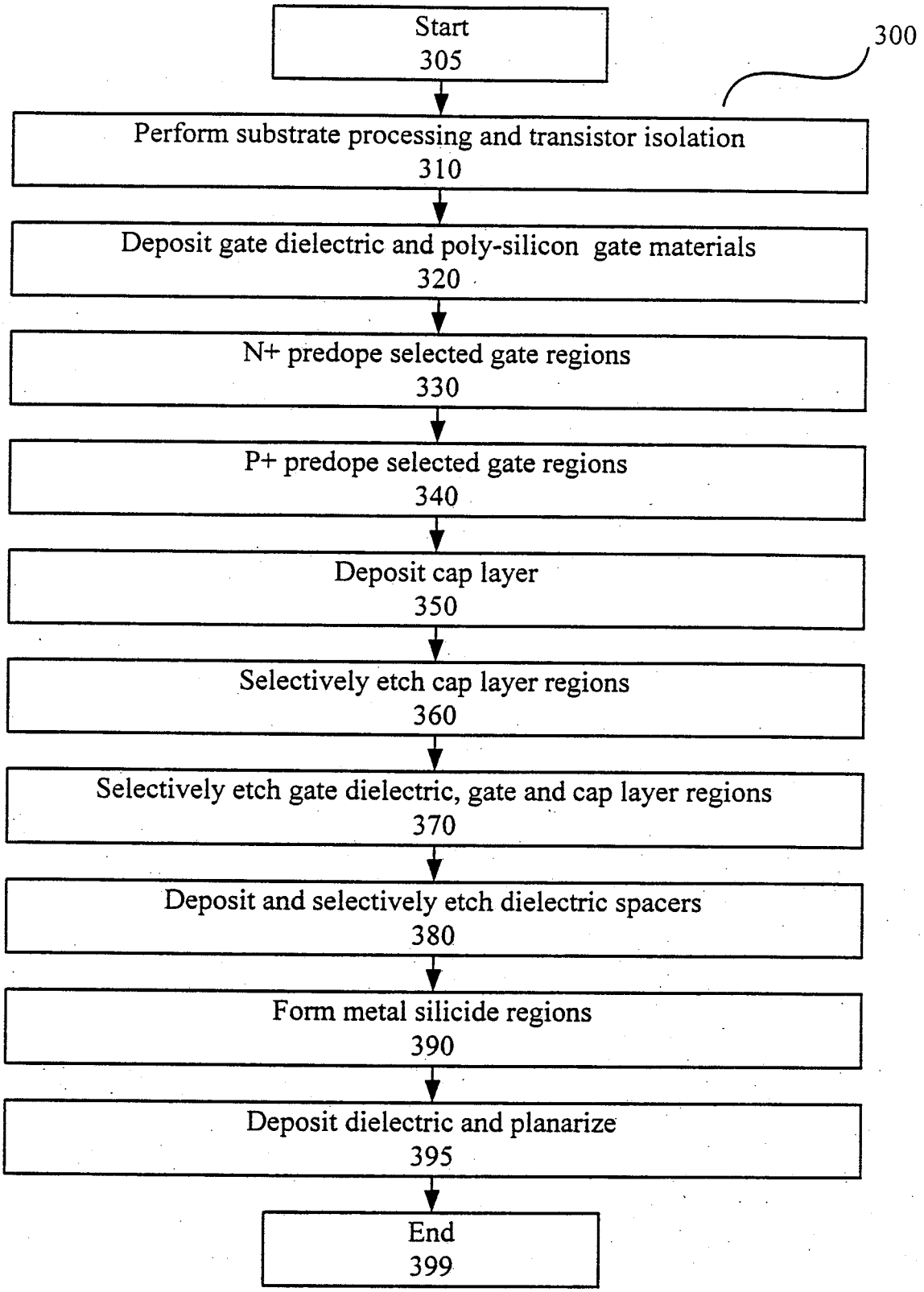

Start
305
300
Perform substrate processing and transistor isolation
310
Deposit gate dielectric and poly-silicon gate materials
320
N+ predope selected gate regions
330
P+ predope selected gate regions
340
Deposit cap layer
350
Selectively etch cap layer regions
360
Selectively etch gate dielectric, gate and cap layer regions
370
Deposit and selectively etch dielectric spacers
380
Form metal silicide regions
390
Deposit dielectric and planarize
395
End
399

FIGURE 3

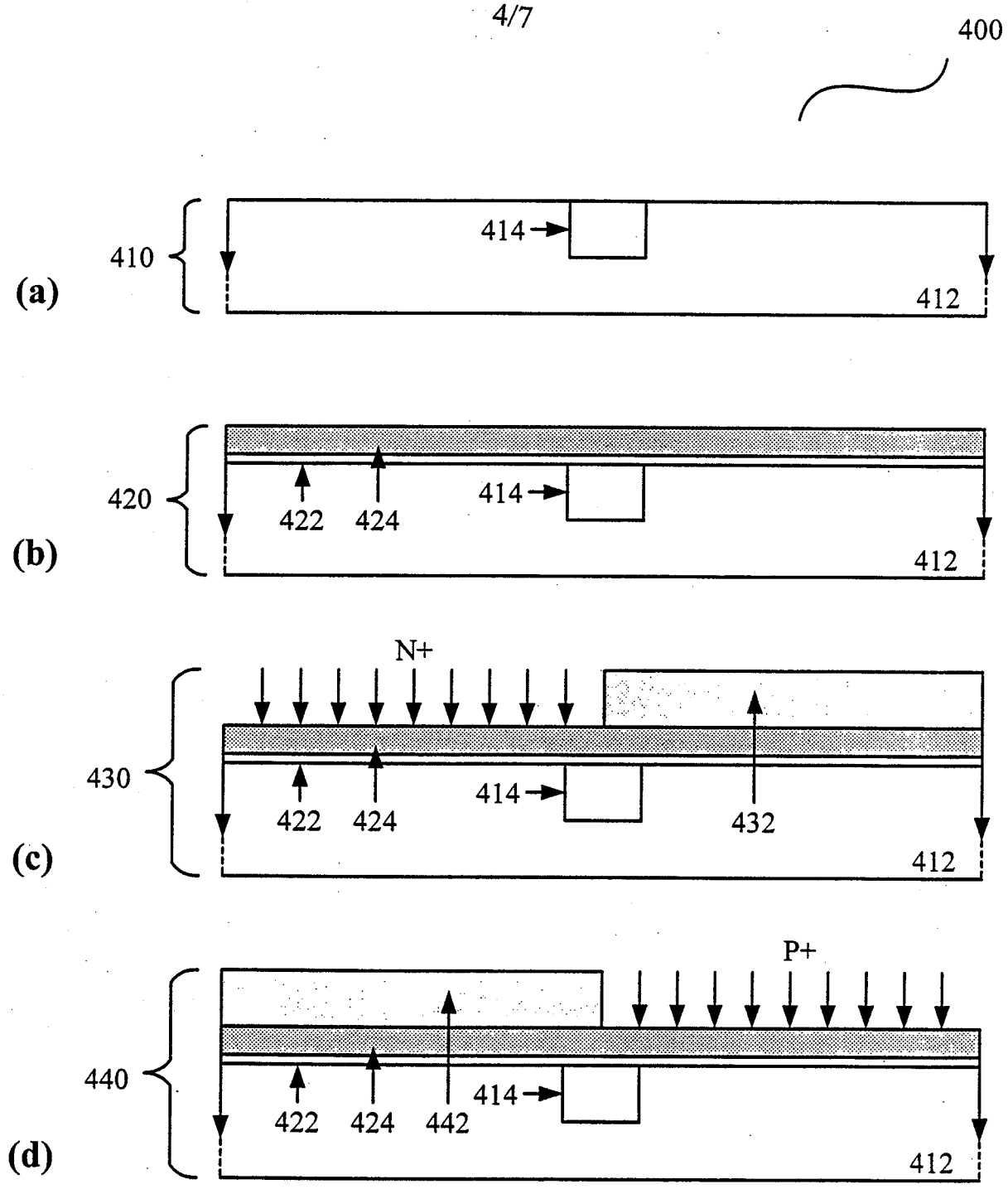

400
(a)
410
414
412
(b)
420
422
424
414
412
(c)
N+
430
422
424
414
432
412
(d)
P+
440
422
424
442
414
412

FIGURE 4

400

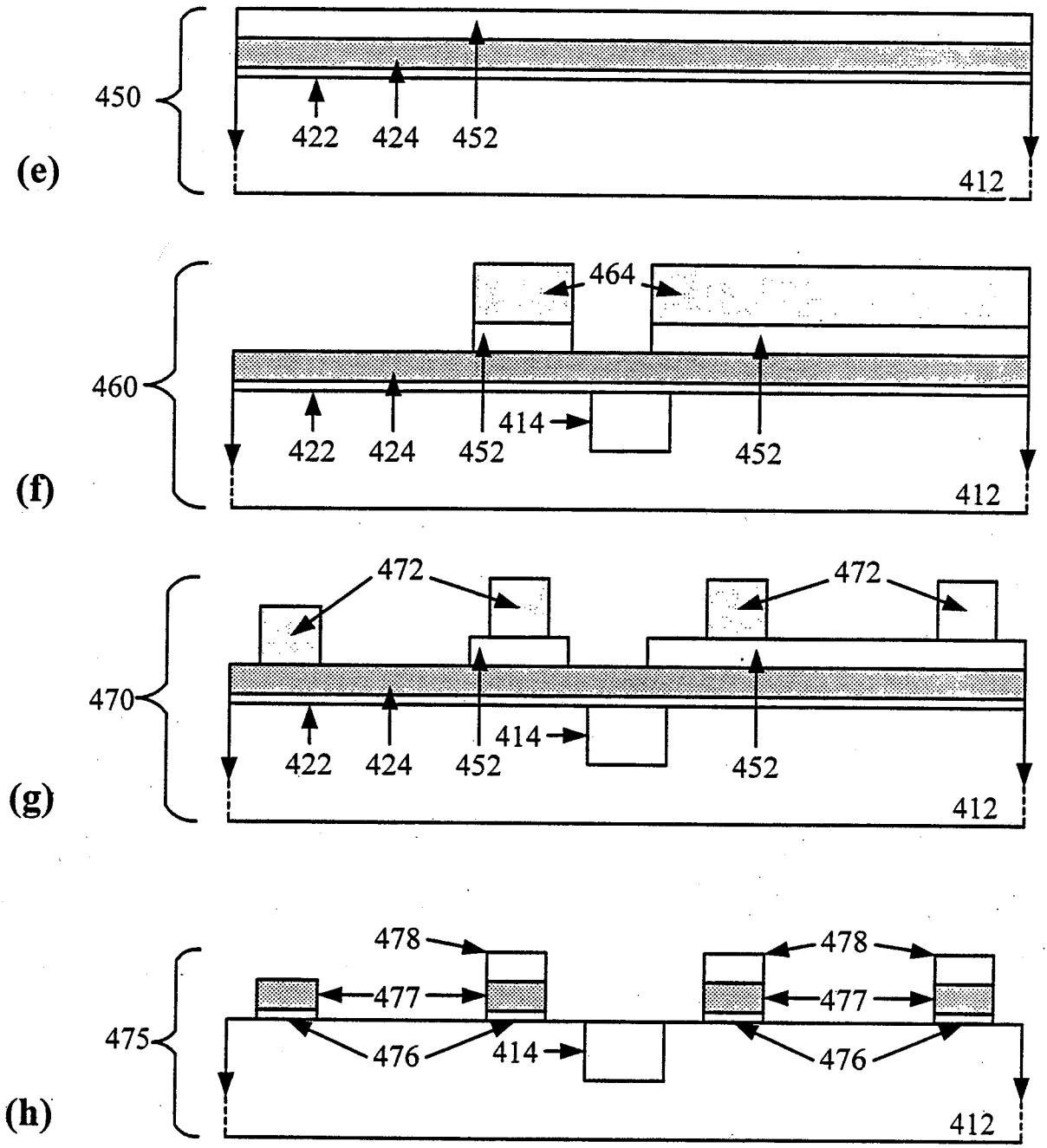

(e)
450
422
424
452
412
(f)
460
464
422
424
452
414
452
412
(g)
470
472
472
422
424
452
414
452
412
(h)
475
478
478
477
477
476
414
476
412

FIGURE 4

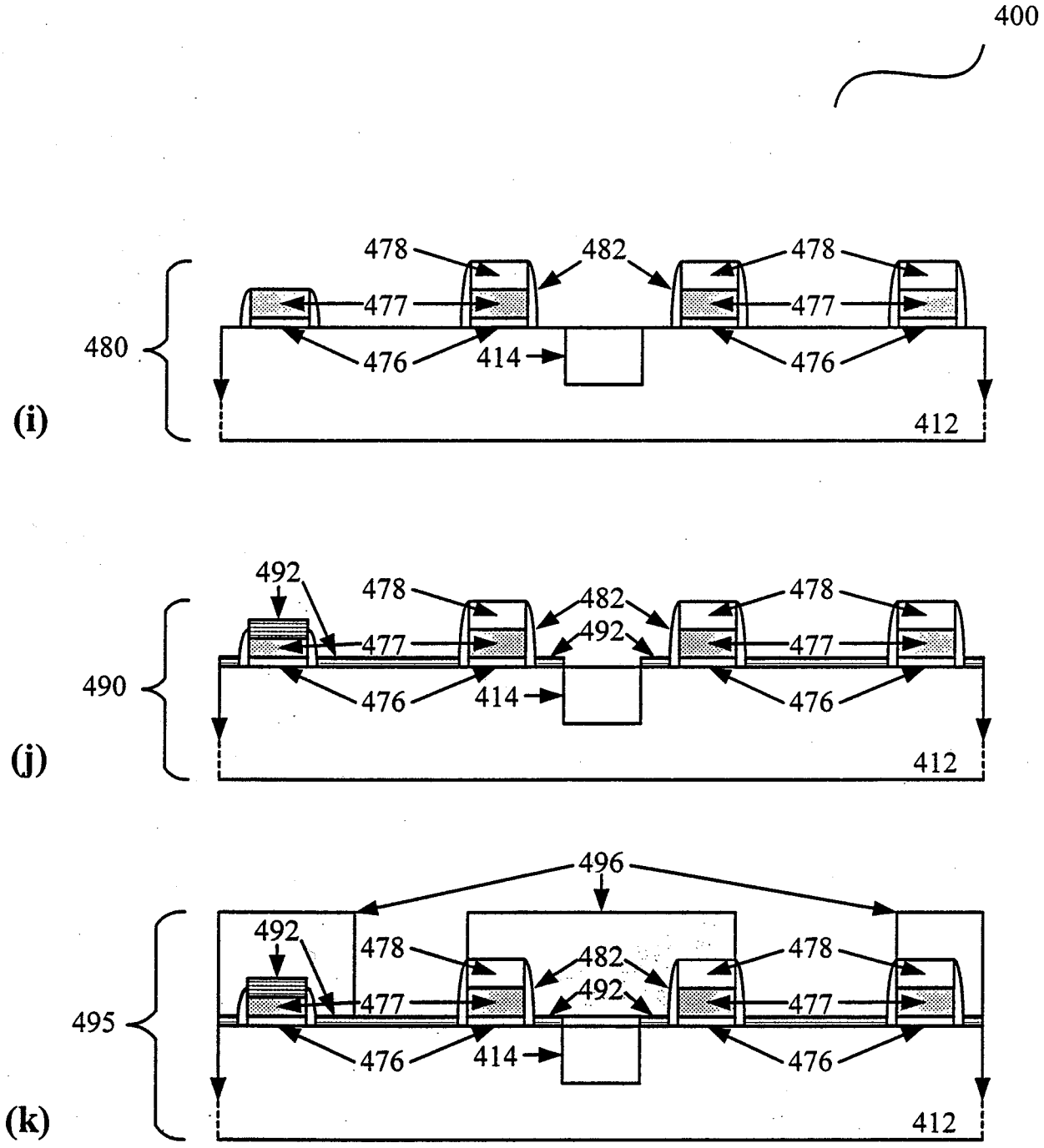

400
478
482
478
477
477
480
476
414
476
412
(i)
492
478
482
478
492
477
477
490
476
414
476
412
(j)
496
492
478
482
478
492
477
477
495
476
414
476
412
(k)

FIGURE 4

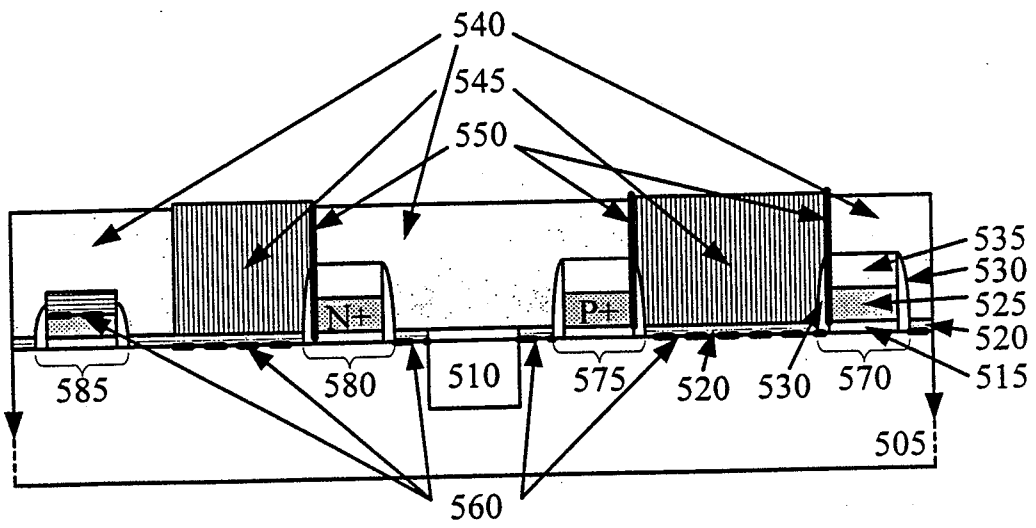

500
540
545
550
535
530
525
520
515
N+
P+
585
580
510
575
520
530
570
505
560

FIGURE 5