CLAIMS

1. An apparatus, comprising:

an integrated circuit, comprising:

a logic analyzer having a first input receiving a plurality of signals and an output for providing an indication of a detection, by the logic analyzer, of at least one trigger event; and

a built in self test (BIST) block having a first input for receiving one or more of the signals appearing at the first input of the logic analyzer, a second input coupled to the output of the logic analyzer for selectively enabling the BIST block, the BIST block generating and maintaining a signature based upon the first and second inputs thereof.

2. The apparatus of claim 1, wherein the BIST block includes an output for providing the maintained signature, the output being coupled to the logic analyzer for sampling or storage therein.

3. The apparatus of claim 1, wherein the logic analyzer includes a multiplexer block having an input coupled to the first input of the logic analyzer, and the first input of the BIST block is coupled to an output of the multiplexer circuit.

4. The apparatus of claim 1, wherein the logic analyzer comprises a multiplexer block having an input coupled to the first input of the logic analyzer and a memory controller block having a first input coupled to an output of the multiplexer block and a second input coupled to the output of the BIST block.

5. The apparatus of claim 1, wherein the BIST block comprises a multiple input shift register, and the signature maintained in the BIST block is maintained in the multiple input shift register.

6. The apparatus of claim 1, wherein the BIST block includes a clock input such that when the BIST block is enabled by the logic analyzer, the BIST block generates a new signature upon each occurrence of a triggering edge of a signal appearing at the clock input of the BIST block.

7. The apparatus of claim 1, further comprising an action block having an input coupled to the logic analyzer to receive the indication of the detection of the at least one trigger event, and an output coupled to the second input of the BIST block, the action block generating at the output thereof a signal that is based upon the input of the action block according to a predetermined function, the predetermined function being configurable.

8. The apparatus of claim 1, further comprising a plurality of BIST blocks, each BIST block having a first input for receiving one or more signals associated with the logic analyzer, a second input coupled to the logic analyzer for enabling the BIST block, and an output coupled to the logic analyzer, wherein each BIST block separately and independently generates and maintains a signature based in part upon the first and second inputs thereof.

9. An integrated circuit, comprising:

a logic analyzer having a first input for receiving a plurality of signals and a first output for providing selected samples of the signals appearing at the first input; and

a signature generator having a first input coupled to the logic analyzer for receiving one or more of the signals appearing at the first input thereof and an output coupled to the logic analyzer for providing the signature thereto.

10. The integrated circuit of claim 9, wherein the logic analyzer includes generates an event signal indicating a detection of an event monitored by the logic analyzer, the signature generator includes an enable input for enabling the signature generator to generate a new signature, and the event signal is coupled to the enable input of the signature generator.

11. The integrated circuit of claim 10, further comprising an action block having an input coupled to the logic analyzer to receive the event signal, and an output signal coupled to the enable input of the signature generator, the action block generating the output signal based at least in part upon the input signal thereof according to a predetermined function.

12. The integrated circuit of claim 12, wherein the predetermined function is programmable.

13. The integrated circuit of claim 9, wherein the logic analyzer includes a multiplexer circuit having an input coupled to the first input of the logic analyzer and a memory control circuit having a first input coupled to an output of the multiplexer block and a second input coupled to the signature generator for receiving the signature therefrom.

14. The integrated circuit of claim 9, wherein the signature generator receives a clock signal and, when enabled, generates a new signature responsive to each triggering edge of the clock signal.

15. The integrated circuit of claim 10, wherein the signature generator is selectively enabled by the logic analyzer.

16. A system, comprising:

one or more system modules; and

an integrated circuit, comprising:

an embedded logic analyzer block having an input for receiving a plurality of signals from the one or more system modules; and

a test block having an input coupled to the embedded logic analyzer block for receiving at least one of the plurality of signals from the one or more system modules, the test block maintaining a signature value therein, the test block selectively generating and maintaining a new signature when enabled based upon the maintained signature and upon the input of the test block.

17. The system of claim 16, wherein the test block includes an output coupled to the embedded logic analyzer block for providing the new signature thereto.

18. The system of claim 16, wherein the test block is enabled and disabled based at least in part by the embedded logic analyzer.

19. The system of claim 16, further comprising a custom block generating at least one output signal according to at least one predetermined function, wherein the test block is enabled and disabled based at least in part by the at least one predetermined function, the at least one predetermined function being programmable.

CLAIMS

1. An apparatus, comprising:

an integrated circuit, comprising:

a logic analyzer having a first input receiving a plurality of signals from one or more portions of the apparatus under test and an output for providing an indication of a detection, by the logic analyzer, of at least one trigger event; and

a built in self test (BIST) block having a first input for receiving one or more of the signals appearing at the first input of the logic analyzer, and a second input coupled to the output of the logic analyzer for selectively enabling the BIST block, the BIST block generating and maintaining a signature based upon the first and second inputs thereof.

2. The apparatus of claim 1, wherein the BIST block includes an output for providing the maintained signature, the output of the BIST block being coupled to the logic analyzer for sampling or storage therein.

3. The apparatus of claim 1, wherein the logic analyzer includes a multiplexer block having an input coupled to the first input of the logic analyzer, and the first input of the BIST block is coupled to an output of the multiplexer block.

4. The apparatus of claim 1, wherein the logic analyzer comprises a multiplexer block having an input coupled to the first input of the logic analyzer and a memory controller block having a first input coupled to an output of the multiplexer block and a second input coupled to the output of the BIST block.

5. The apparatus of claim 1, wherein the BIST block comprises a multiple input shift register, and the signature maintained in the BIST block is maintained in the multiple input shift register.

6. The apparatus of claim 1, wherein the BIST block includes a clock input such that when the BIST block is enabled by the logic analyzer, the BIST block generates a new signature upon each occurrence of a triggering edge of a signal appearing at the clock input of the BIST block.

7. The apparatus of claim 1, further comprising an action block having an input coupled to the logic analyzer to receive the indication of the detection of the at least one trigger event, and an output coupled to the second input of the BIST block, the action block generating at the output thereof a signal that is based upon the input of the action block according to a predetermined function, the predetermined function being configurable.

8. The apparatus of claim 1, further comprising a plurality of BIST blocks, each BIST block having a first input for receiving one or more signals associated with the logic analyzer, a second input coupled to the logic analyzer for enabling the BIST block, and an output coupled to the logic analyzer, wherein each BIST block separately and independently generates and maintains a signature based in part upon the first and second inputs thereof.

9. An integrated circuit, comprising:

a logic analyzer having a first input for receiving a plurality of signals from a system under test and a first output for providing selected samples of the signals appearing at the first input; and

a signature generator having a first input coupled to the logic analyzer for receiving one or more of the signals appearing at the first input thereof and an output coupled to the logic analyzer providing a signature via the output of the signature generator to the logic analyzer, the logic analyzer sampling one or more of the plurality of signals appearing at the first input thereof from the system under test during a test or debug operation as the signature generator generates a new signature.

10. The integrated circuit of claim 9, wherein the logic analyzer generates an event signal indicating a detection of an event monitored by the logic analyzer, the signature generator includes an enable input for enabling the signature generator to generate the new signature, and the event signal is coupled to the enable input of the signature generator.

11. The integrated circuit of claim 10, further comprising an action block having an input coupled to the logic analyzer to receive the event signal, and an output signal coupled to the enable input of the signature generator, the action block generating the output signal based at least in part upon the input signal thereof according to a predetermined function.

12. The integrated circuit of claim 11, wherein the predetermined function is programmable.

13. The integrated circuit of claim 9, wherein the logic analyzer includes a multiplexer circuit having an input coupled to the first input of the logic analyzer and a memory control circuit having a first input coupled to an output of the multiplexer circuit and a second input coupled to the signature generator for receiving the signature therefrom.

14. The integrated circuit of claim 9, wherein the signature generator receives a clock signal and, when enabled, generates a new signature responsive to each triggering edge of the clock signal.

15. The integrated circuit of claim 10, wherein the signature generator is selectively enabled by the logic analyzer.

16. A system, comprising:

one or more system modules; and

an integrated circuit, comprising:

an embedded logic analyzer block having an input for receiving a plurality of signals from the one or more system modules; and

a test block having an input coupled to the embedded logic analyzer block for receiving at least one of the plurality of signals from the one or more system modules, the test block maintaining a signature value therein, the test block selectively generating and maintaining a new signature when enabled based upon the maintained signature and upon the input of the test block, the embedded logic analyzer block sampling and storing one or more of the signals appearing at the input thereof from the one or more system modules while the test block generates at least one new signature.

17. The system of claim 16, wherein the test block includes an output coupled to the embedded logic analyzer block for providing the new signature thereto.

18. The system of claim 16, wherein the test block is enabled and disabled based at least in part by the embedded logic analyzer.

19. The system of claim 16, further comprising a custom block generating at least one output signal according to at least one predetermined function, wherein the test block is enabled and disabled based at least in part by the at least one predetermined function, the at least one predetermined function being programmable.

20. The system of claim 16, wherein the embedded logic analyzer includes an output for providing an indication of a detection of at least one trigger event, and the test block includes an enable input coupled to the output of the embedded logic analyzer, the test block being selectively enabled to generate and maintain the new signature based upon the indication received at the enable input thereof.

21. The apparatus of claim 1, wherein the logic analyzer samples one or more of the plurality of signals appearing at the first input thereof from the one or more portions of the apparatus under test during a test or debug operation as the BIST block generates the signature.