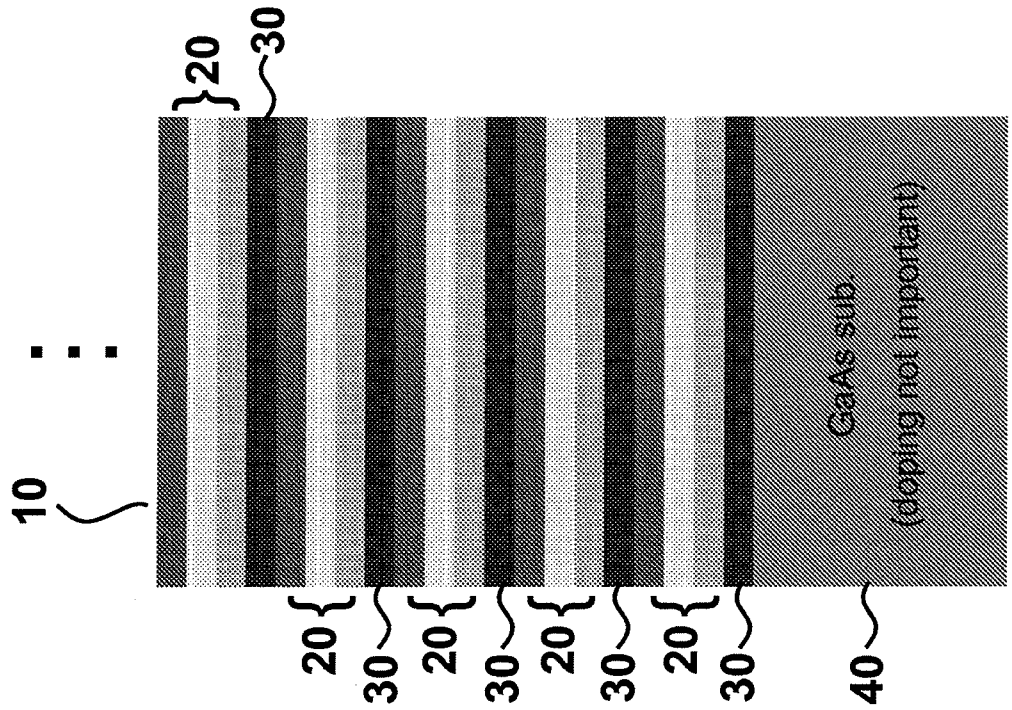

10
20
30
GaAs sub.
(doping not important)
40

Fig. 1A

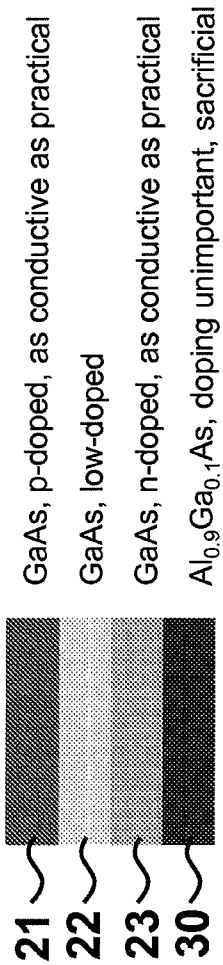

GaAs, p-doped, as conductive as practical
GaAs, low-doped
GaAs, n-doped, as conductive as practical
$Al_{0.9}Ga_{0.1}As$, doping unimportant, sacrificial
21
22
23
30

Fig. 1B

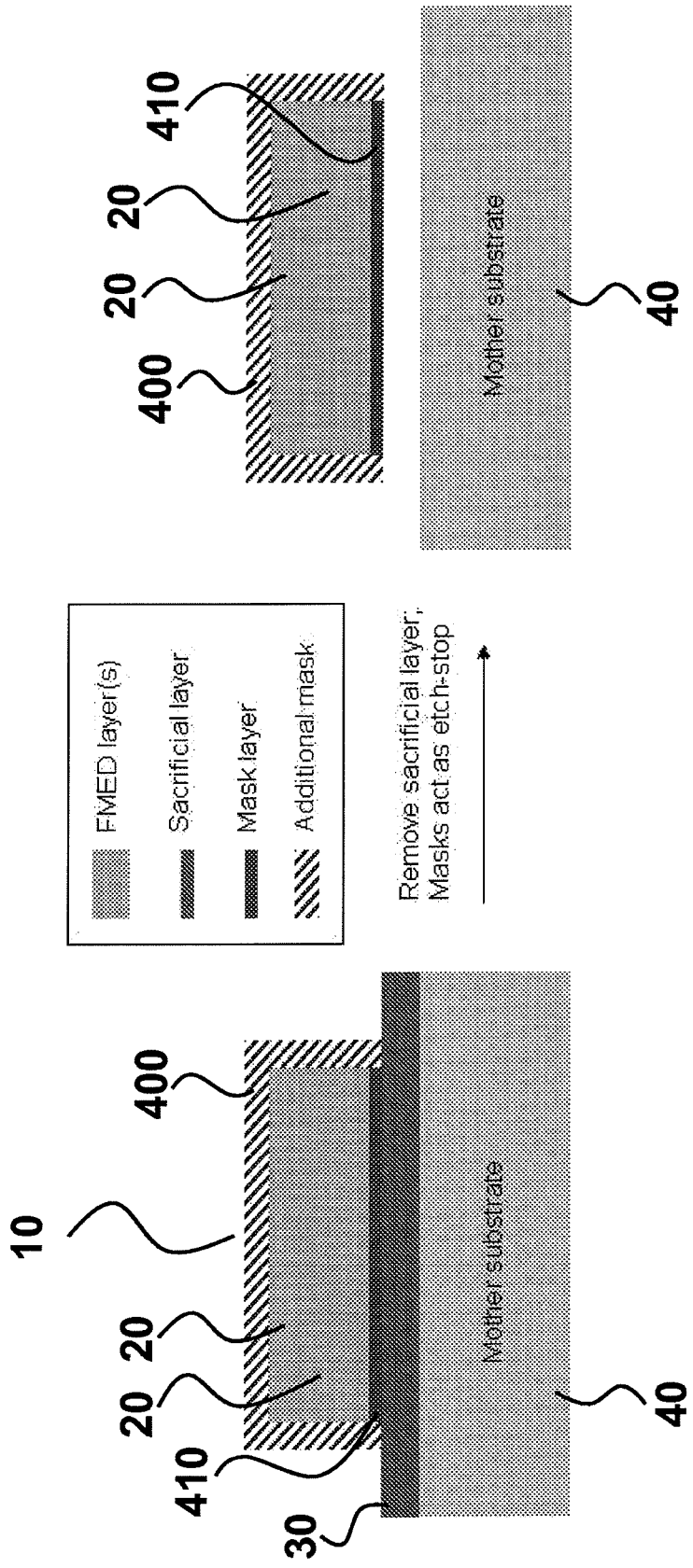

10
400
20
20
410
30
Mother substrate
40
Remove sacrificial layer;
Masks act as etch-stop
FMED layer(s)
Sacrificial layer
Mask layer
Additional mask
410
20
20
400
Mother substrate
40

Figure 2A

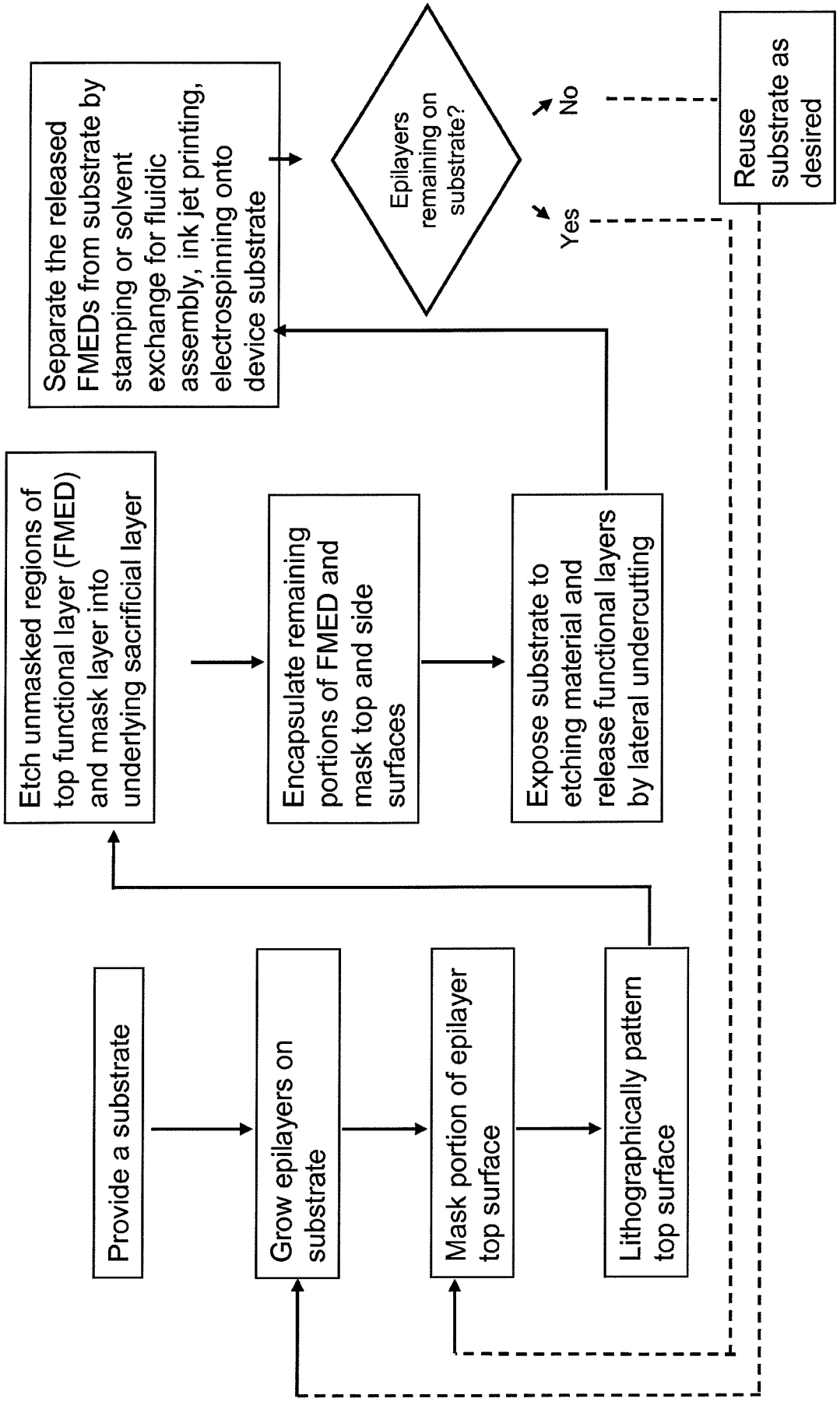

Provide a substrate
Grow epilayers on substrate
Mask portion of epilayer top surface
Lithographically pattern top surface
Etch unmasked regions of top functional layer (FMED) and mask layer into underlying sacrificial layer
Encapsulate remaining portions of FMED and mask top and side surfaces
Expose substrate to etching material and release functional layers by lateral undercutting
Separate the released FMEDs from substrate by stamping or solvent exchange for fluidic assembly, ink jet printing, electrospinning onto device substrate
Epilayers remaining on substrate?
No
Yes
Reuse substrate as desired

Figure 2B

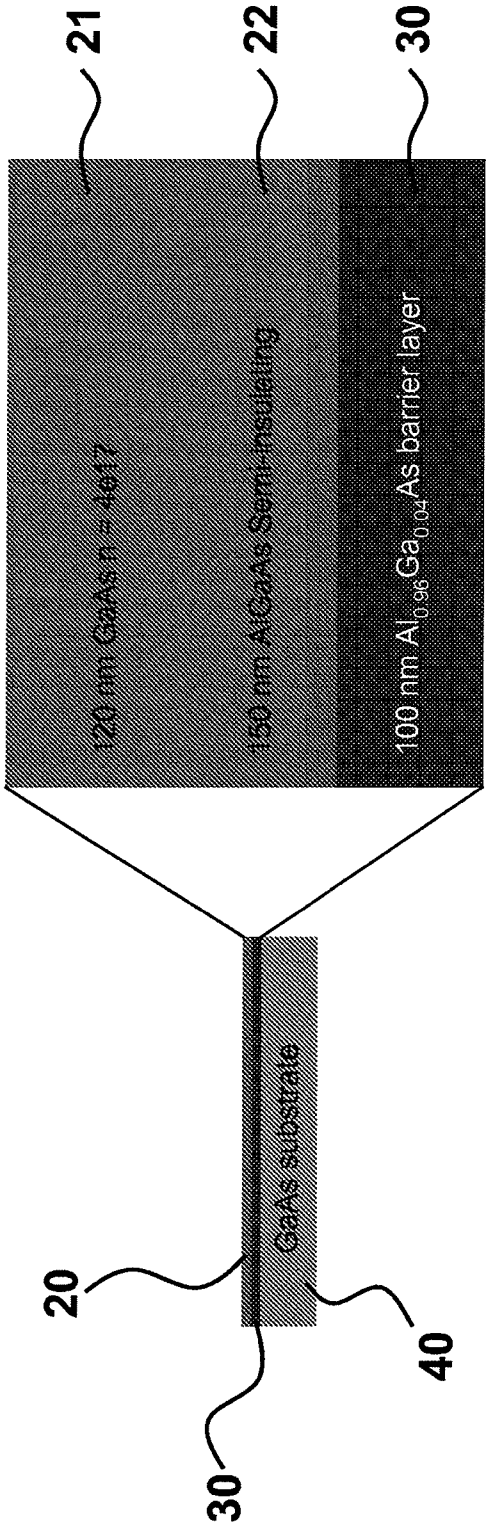
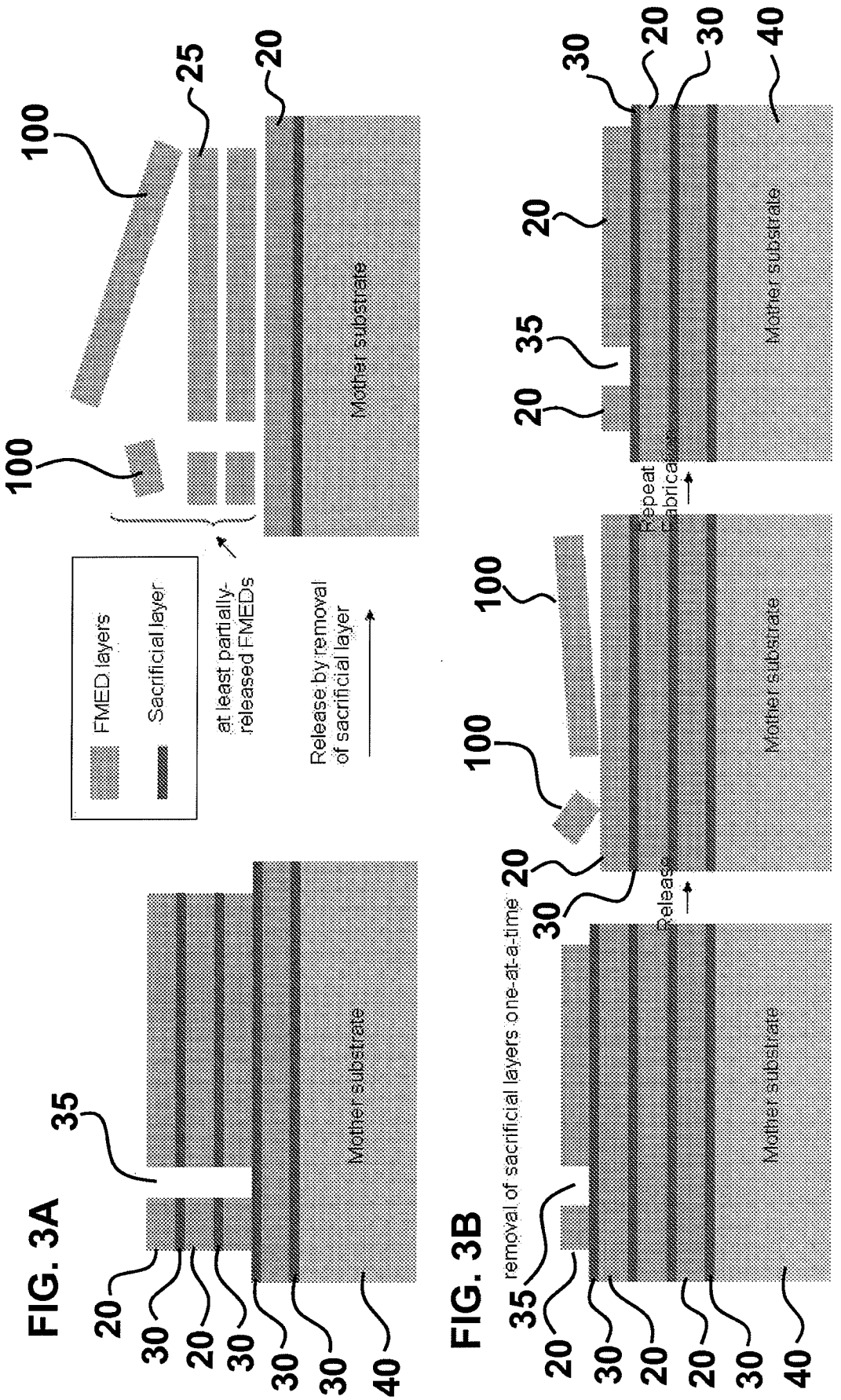

21
22
30
120 nm GaAs n = 4e17
150 nm AlGaAs Semi-insulating
100 nm $Al_{0.96}Ga_{0.04}As$ barrier layer
GaAs substrate
20
30
40

Figure 2C


FIG. 3A
FIG. 3B
FMED layers
Sacrificial layer
at least partially-released FMEDs
Release by removal of sacrificial layer
Mother substrate
removal of sacrificial layers one-at-a-time
Repeat fabrication
Release
20
25
30
35
40
100

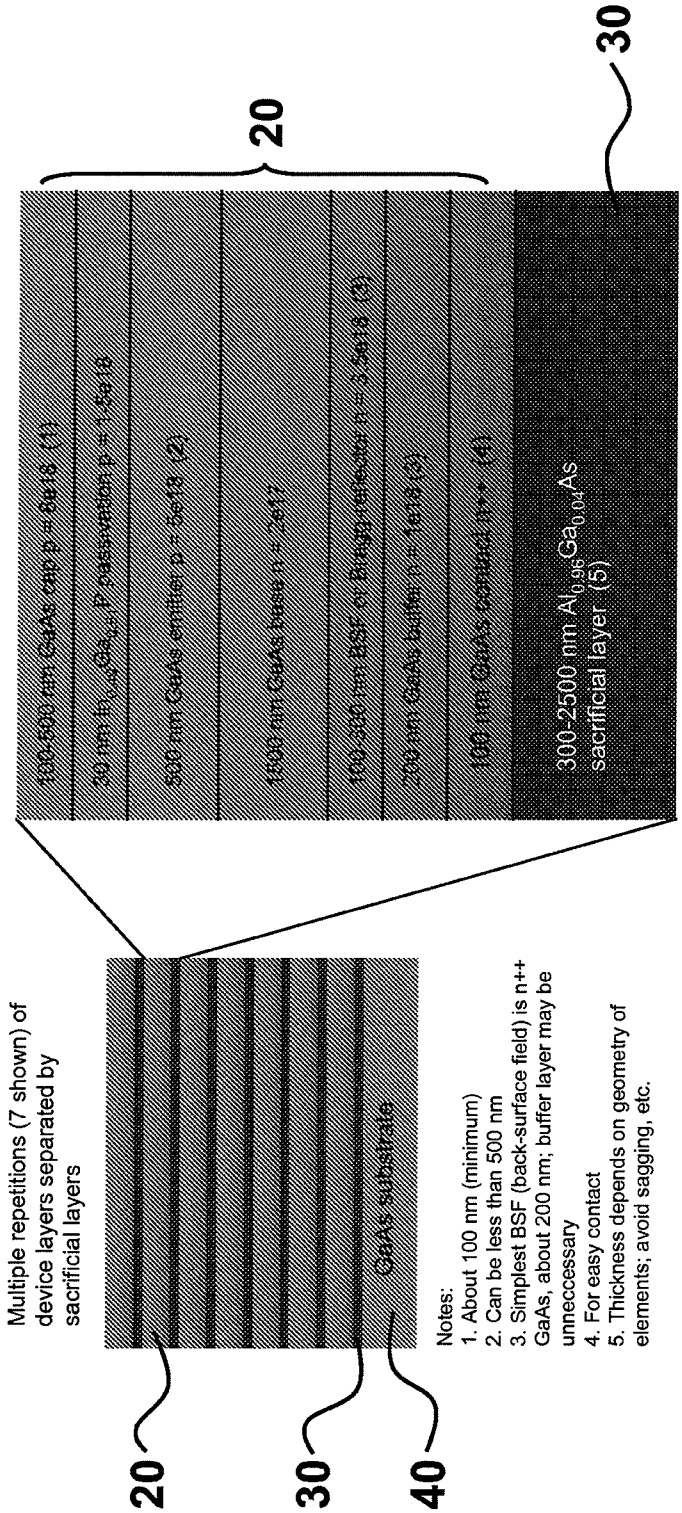

20
30
40
GaAs substrate
Multiple repetitions (7 shown) of device layers separated by sacrificial layers
100-500 nm GaAs cap p = 6e19 (1)
30 nm In0.49Ga0.51P passivation p = 1.5e18
500 nm GaAs emitter p = 5e18 (2)
4000 nm GaAs base n = 2e17
100-300 nm BSF or Bragg reflector n = 3.5e18 (3)
200 nm GaAs buffer n = 1e18 (3)
100 nm GaAs contact n++ (4)
300-2500 nm Al0.96Ga0.04As sacrificial layer (5)
Notes:
1. About 100 nm (minimum)
2. Can be less than 500 nm
3. Simplest BSF (back-surface field) is n++ GaAs, about 200 nm; buffer layer may be unneccessary
4. For easy contact
5. Thickness depends on geometry of elements; avoid sagging, etc.

FIG. 3C

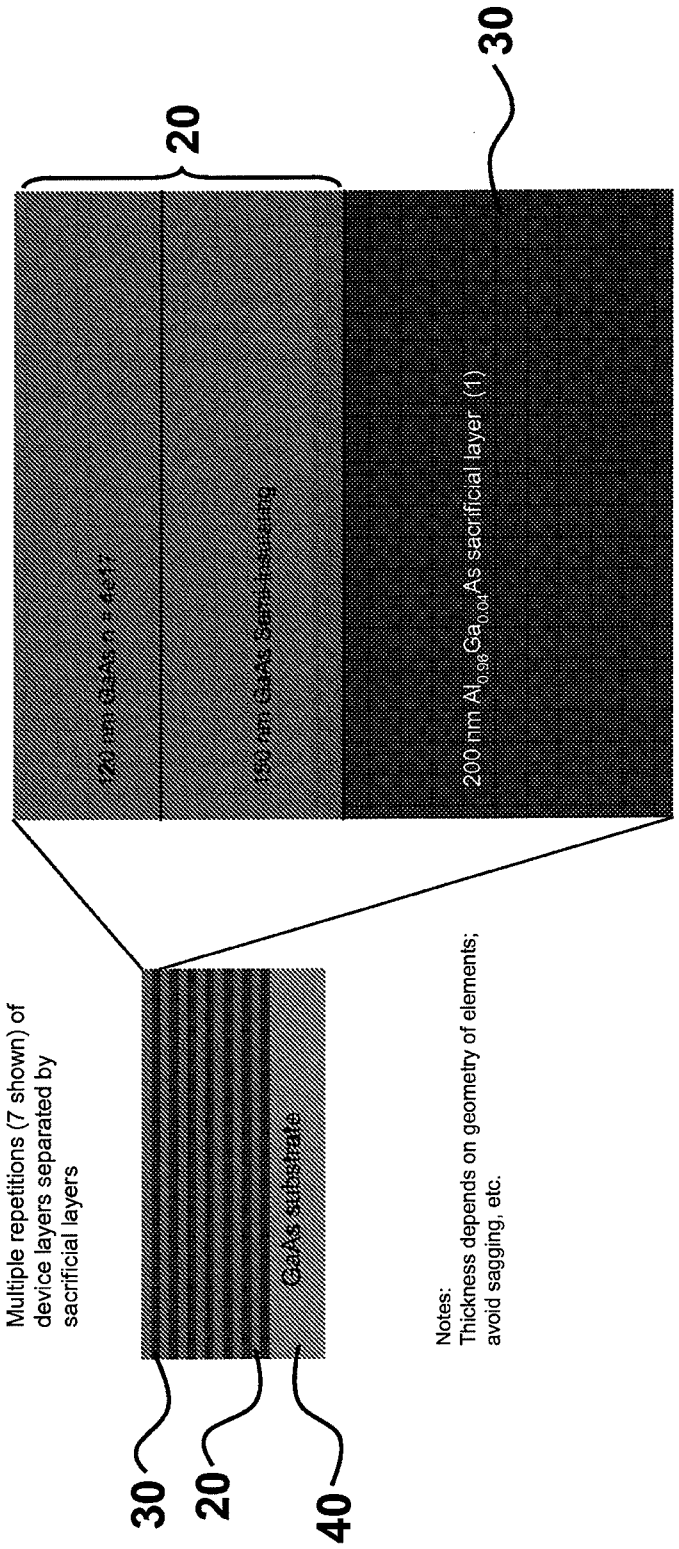

20
30
120 nm GaAs, n = 4e17
150 nm GaAs barrier/etch
200 nm Al0.98Ga0.04As sacrificial layer (1)
Multiple repetitions (7 shown) of device layers separated by sacrificial layers
GaAs substrate
30
20
40
Notes:
Thickness depends on geometry of elements; avoid sagging, etc.

FIG. 3D

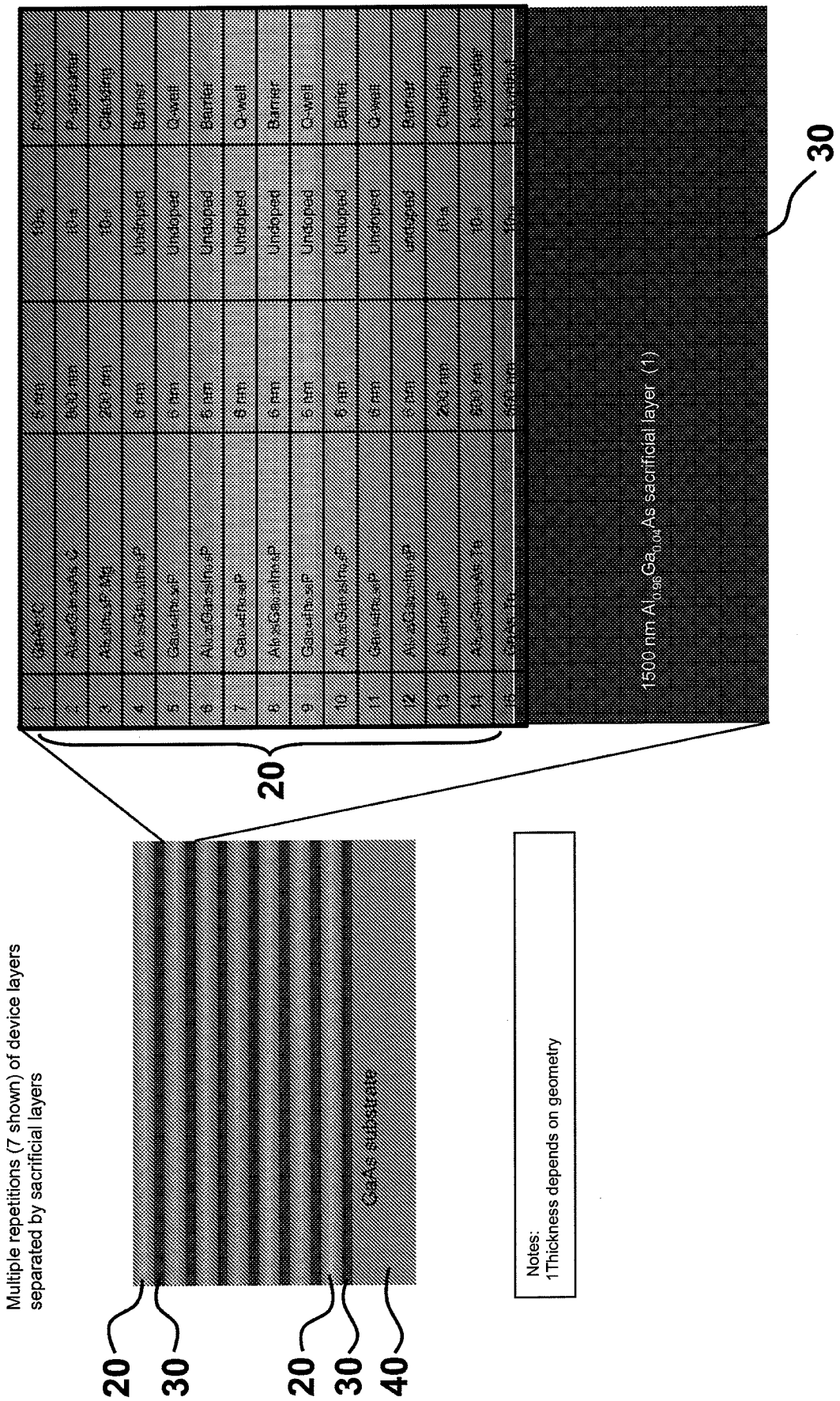

1500 nm $Al_{0.96}Ga_{0.04}As$ sacrificial layer (1)
30
20
Multiple repetitions (7 shown) of device layers separated by sacrificial layers
GaAs substrate
20
30
20
30
40
Notes:
1Thickness depends on geometry

FIG. 3E

Process flow 1: release of FMEDs for photovoltaics, "multiple-layers-at-a-time" with optional re-use of substrate
See also FIG. 3A
Here shown for epitaxially grown semiconductors. Also works for amorphous or polycrystalline materials similar to what's described in FIG. 12 (process flow 6)

1. obtain GaAs substrate
2. Grow epilayers described by FIG. 3C on GaAs substrate by MOCVD, MBE, etc. (similar process for FIGs 3D and 3E for transistors, LEDs, respectively). Pre-treat substrate prior to growth as needed (CMP may be required, but not likely. Likely will need to grow ~200 nm buffer layer of GaAs adjacent to substrate before functional and sacrificial layers).
3. mask portion of the surface of the top epilayer with SiO_2 by Plasma-Enhanced Chemical Vapor Deposition (PECVD) and some form of lithography for patterning.
4. Etch unmasked regions of epilayers using Cl/Ar/H plasma from surface to some distance into any $Al_{0.96}Ga_{0.04}As$ sacrificial layer (for example, into the sacrificial layer closest to the substrate). The sacrificial layer should not be the one farthest from the substrate (in that case, the release would happen "one-at-a-time" as in FIG. 5 (process flow 2)).
5. Expose the substrate to concentrated HF to at least partially remove the exposed sacrificial layers and release the functional epilayers above the sacrificial layers by lateral undercutting. (HF attacks the functional epilayers more slowly (less than 1/10 etch rate) than it does the sacrificial layer.)
6. Separate the released FMEDs from substrate by stamping or do solvent exchange for fluidic assembly or ink jet printing, electrospinning, etc.
7. use HF to remove any remaining portions of the sacrificial layers; wash/rub away any remaining portions of the overlying functional epilayers (anchoring structures, etc.) the Functional layers that were originally directly underneath the first sacrificial layer are now exposed and on the surface of the substrate
8. Repeat steps 3 through 7, releasing sets of functional layers (each set separated by sacrificial layers) one set at a time until no sacrificial layers remain on the substrate.
9. (optional, for re-use of substrate) Repeat steps 2 through 8 as desired.

FIG. 4

Process flow 2: release of FMEDs for photovoltaics, "one-layer-at-a-time" with optional re-use of substrate
See also FIG. 3B.
Here shown for epitaxially grown semiconductors. Also works for amorphous or polycrystalline materials similar to what's described in process flow 6

1. obtain GaAs substrate
2. Grow epilayers described by FIG. 3C on GaAs substrate by MOCVD, MBE, etc. (similar process for FIGs 3D and 3E for transistors, LEDs, respectively) Pre-treat substrate prior to growth as needed (CMP may be required, but not likely. Likely will need to grow ~200 nm buffer layer of GaAs adjacent to substrate before functional and sacrificial layers).
3. mask portion of the surface of the top epilayer with ~500 nm of SiO_2 by Plasma-Enhanced Chemical Vapor Deposition (PECVD) and some form of lithography for patterning.
4. Etch unmasked regions of epilayers using Cl/Ar/H plasma from surface to some distance into the first $Al_{0.96}Ga_{0.04}As$ sacrificial layer.
5. Expose the substrate to concentrated HF to at least partially remove the exposed sacrificial layer (one) and release the epilayers above the sacrificial layer (functional layers) by lateral undercutting. (HF attacks the functional epilayers more slowly (less than 1/10 etch rate) than it does the sacrificial layer.)
6. Separate the released FMEDs from substrate by stamping or do solvent exchange for fluidic assembly or ink jet printing, electrospinning, etc.
7. use HF to remove any remaining portions of the sacrificial layer; wash/rub away any remaining portions of the overlying functional epilayers (anchoring structures, etc.) the Functional layers that were originally directly underneath the first sacrificial layer are now exposed and on the surface of the substrate
8. Repeat steps 3 through 7, releasing individual functional layers (each layer separated by sacrificial layers) one layer at a time until no sacrificial layers remain on the substrate.
9. (optional, for re-use of substrate) Repeat steps 2 through 8 as desired.

FIG. 5

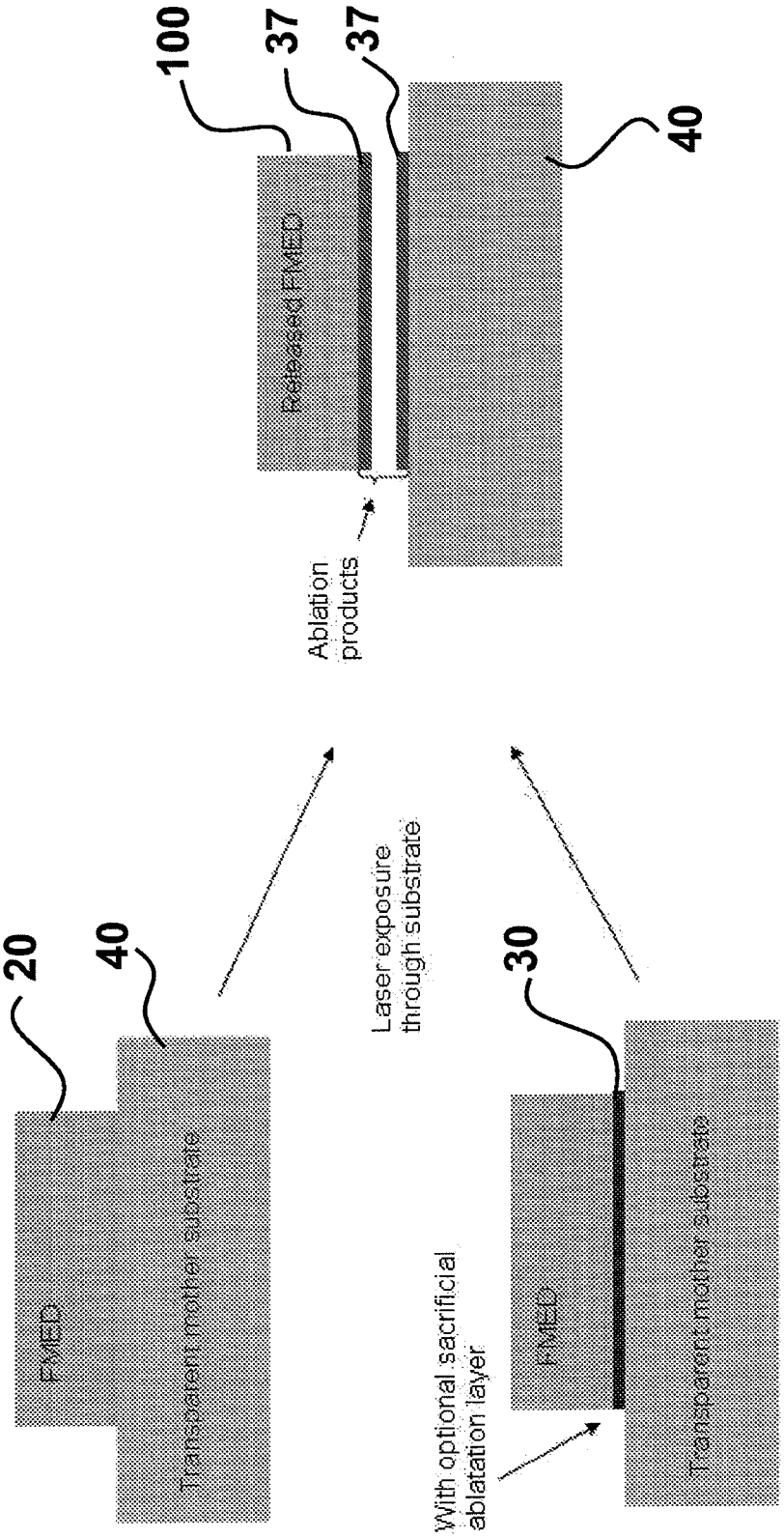

100
37
37
40
Released FMED
Ablation products
Laser exposure through substrate
20
40
30
FMED
Transparent mother substrate
With optional sacrificial ablation layer
FMED
Transparent mother substrate

FIG. 6A

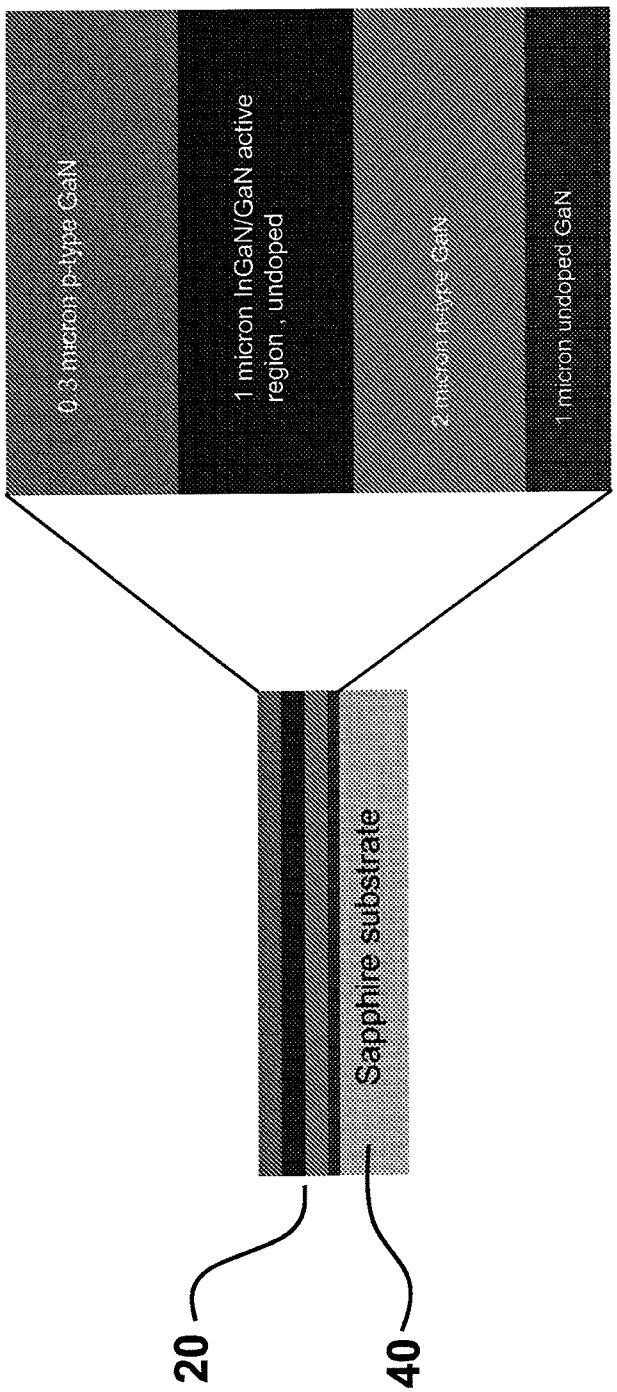

0.3 micron p-type GaN
1 micron InGaN/GaN active region , undoped
2 micron n-type GaN
1 micron undoped GaN
Sapphire substrate
20
40

FIG. 6B

Process flow 4: release of FMEDs for LEDs by laser ablation

See also FIG. 6 (from: Tan, B. S., Yuan, S. & Kang, X. J. Performance enhancement of InGaN light-emitting diodes by laser lift-off and transfer from sapphire to copper substrate. Applied Physics Letters 84, 2757-2759 (2004)).

1. obtain GaN/InGaN on sapphire substrate similar to that shown in FIG. 6B.

2. mask portion of the surface of the top epilayer with SiO_2 by Plasma-Enhanced Chemical Vapor Deposition (PECVD) and some form of lithography for patterning.

3. Etch unmasked regions of epilayers using BCl_3/Cl/Ar/H plasma from surface through epilayers

4. Expose some portion of the epilayers through sapphire substrate with KrF laser (248 nm) to decompose the GaN adjacent to the sapphire to Ga (metal) and N_2 (gas).

5. Heat the substrate to 30°C, thereby (combined with step 4) releasing at least a portion of the epilayers from the substrate.

6. Separate the released FMEDs from substrate by stamping or perform solvent exchange for fluidic assembly or ink jet printing, electrospinning, etc.

FIG. 6C

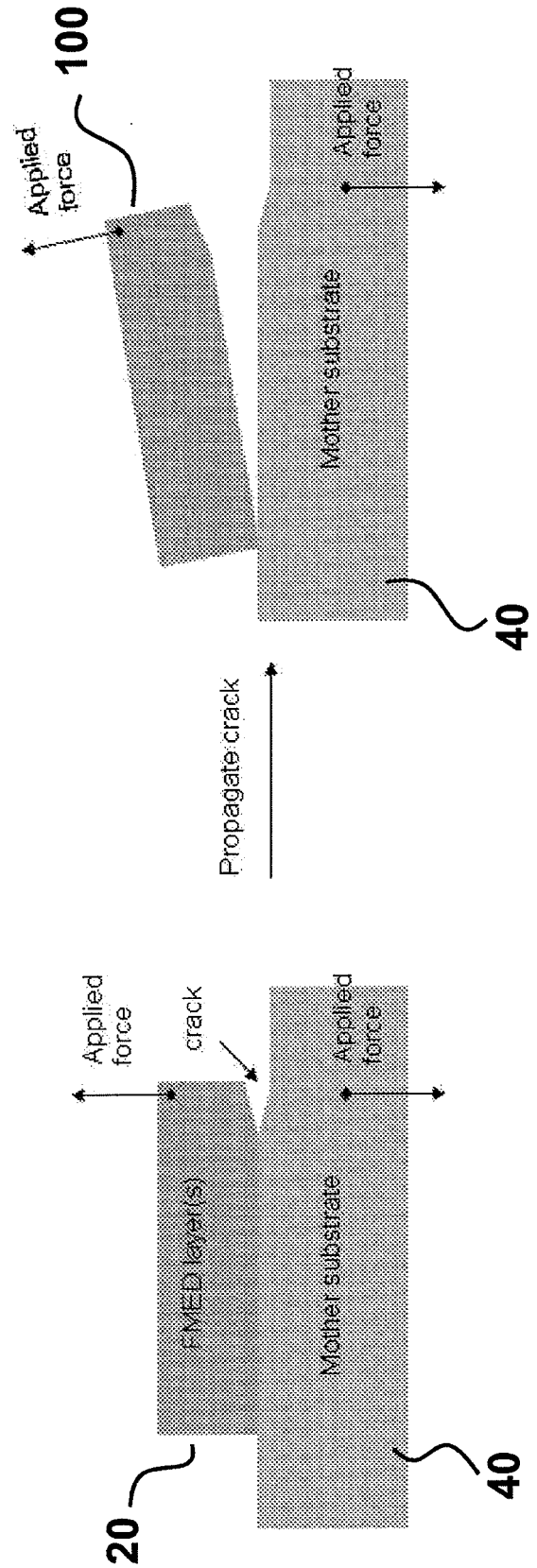

100
Applied force
Applied force
Mother substrate
40
Propagate crack
Applied force
crack
Applied force
FMED layer(s)
Mother substrate
20
40

FIG. 7A

Process flow 7: release of FMEDs by propagating a crack introduced by chemical means.
See also FIG. 7A

1. obtain silicon substrate
2. deposit SiO_2 by PECVD on substrate
3. do photolithography and wet etching in buffered oxide etch (BOE) to generate sloped sidewalls in SiO_2 features (see FIG. 11)
4. do photolithography and evaporation (lift-off) to deposit about 100 nm of gold across gaps between SiO_2 features, overlapping them, as shown in FIG. 11.
5. remove remaining SiO_2 using BOE or HF to introduce cracks chemically.
6. apply mechanical force to gold film (with stamps, tweezers, etc.) to separate gold film from substrate

FIG. 7B

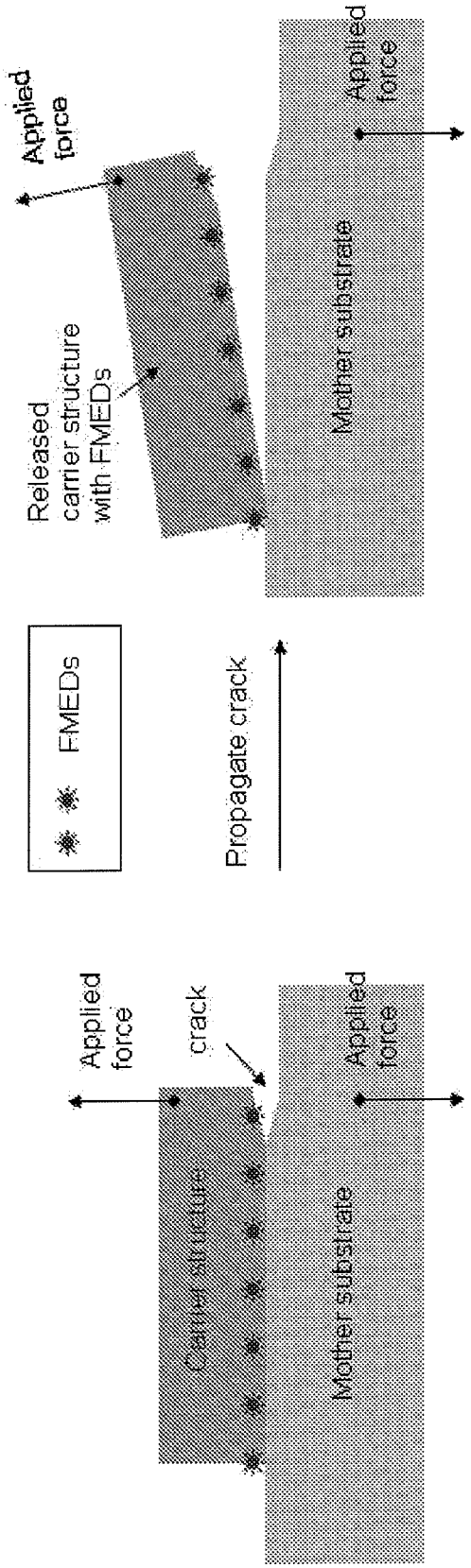

Applied force
Released carrier structure with FMEDs
Mother substrate
Applied force
FMEDs
Propagate crack
Applied force
crack
Carrier structure
Mother substrate
Applied force

FIG. 8A

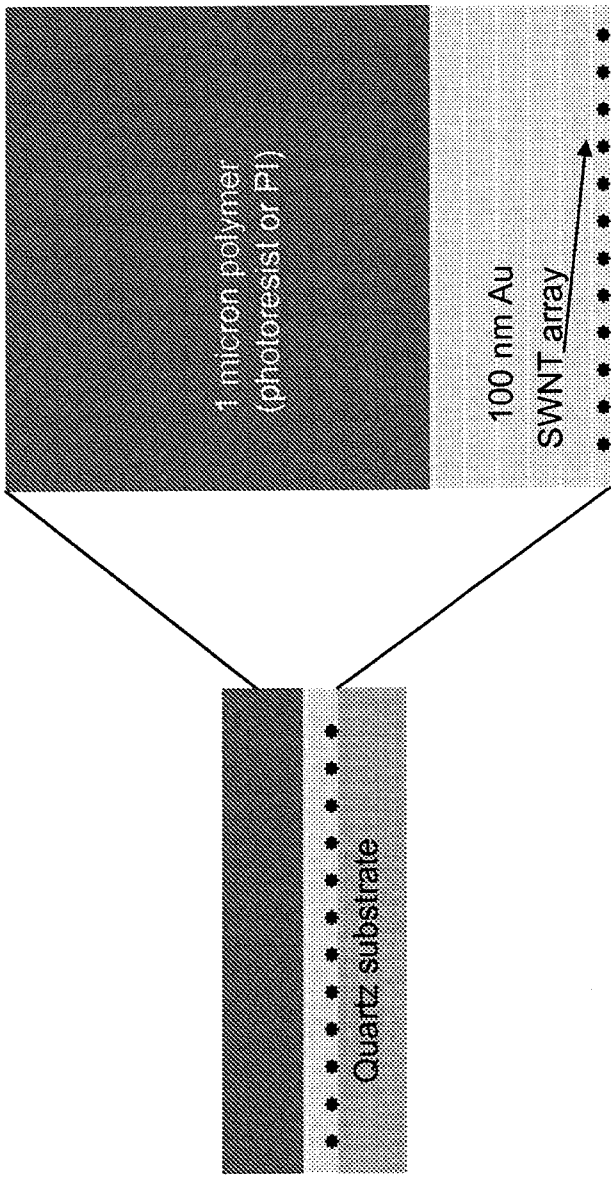

1 micron polymer
(photoresist or PI)
100 nm Au
SWNT array
Quartz substrate

FIG. 8B

Process flow 5: release of FMEDs (array of SWNTs) using a carrier film and the separation of a crack introduced mechanically

See FIGs 7A and 8A

1. obtain substrate with structure described by FIG. 8B by growing SWNTs on quartz by CVD, then evaporating Au, then spinning on polymer. The polymer and the gold make-up the carrier film for the FMEDs (SWNTs).

2. use a razor blade to cut a line through the polymer and gold film to the quartz substrate, thereby introducing a crack

3. separate the carrier film and the SWNT array by applying a mechanical force via a PDMS stamp, tweezers, etc.

FIG. 8C

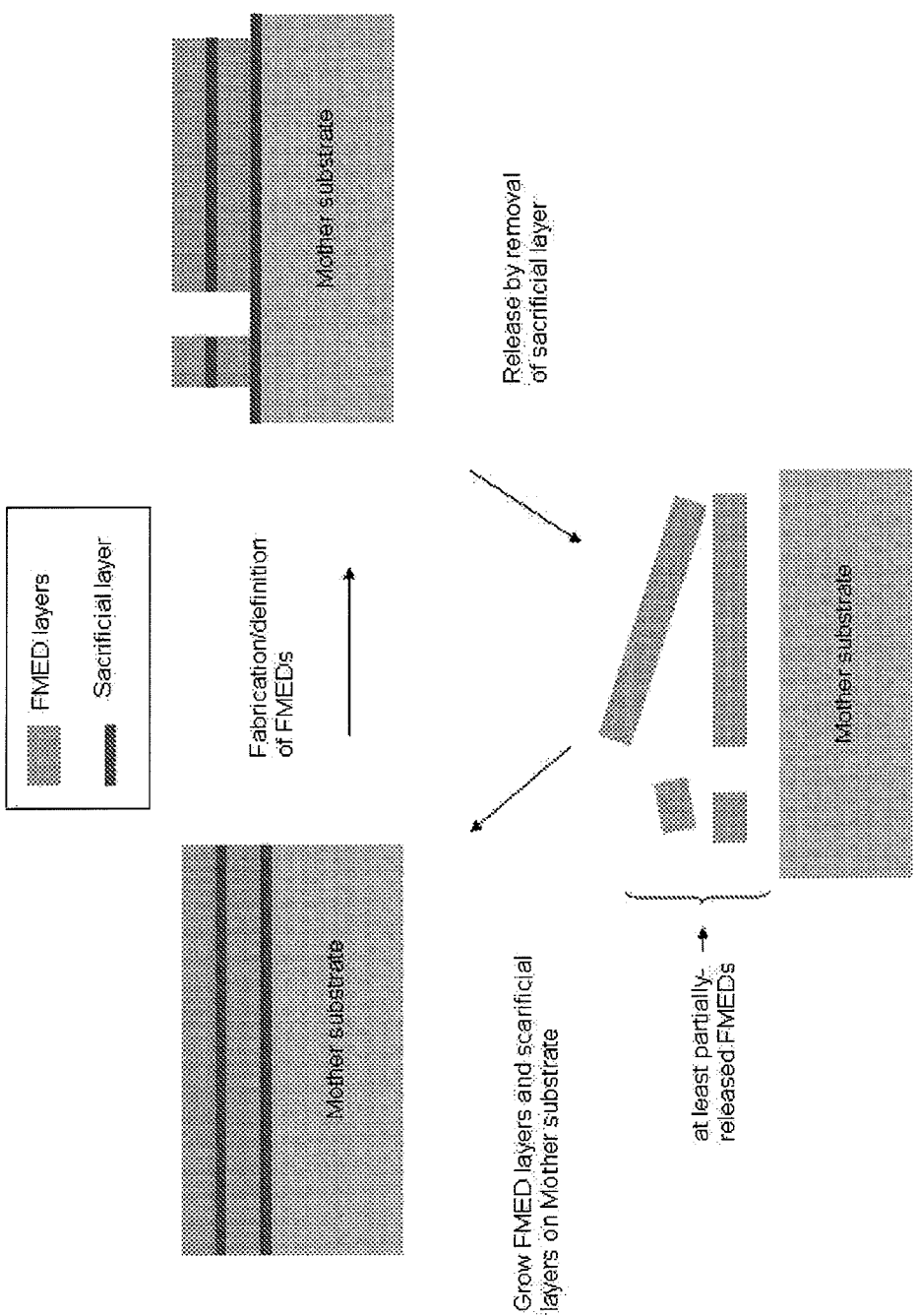

FMED layers
Sacrificial layer
Mother substrate
Fabrication/definition of FMEDs
Mother substrate
Release by removal of sacrificial layer
Grow FMED layers and scarificial layers on Mother substrate
at least partially-released FMEDs
Mother substrate

FIG. 9A

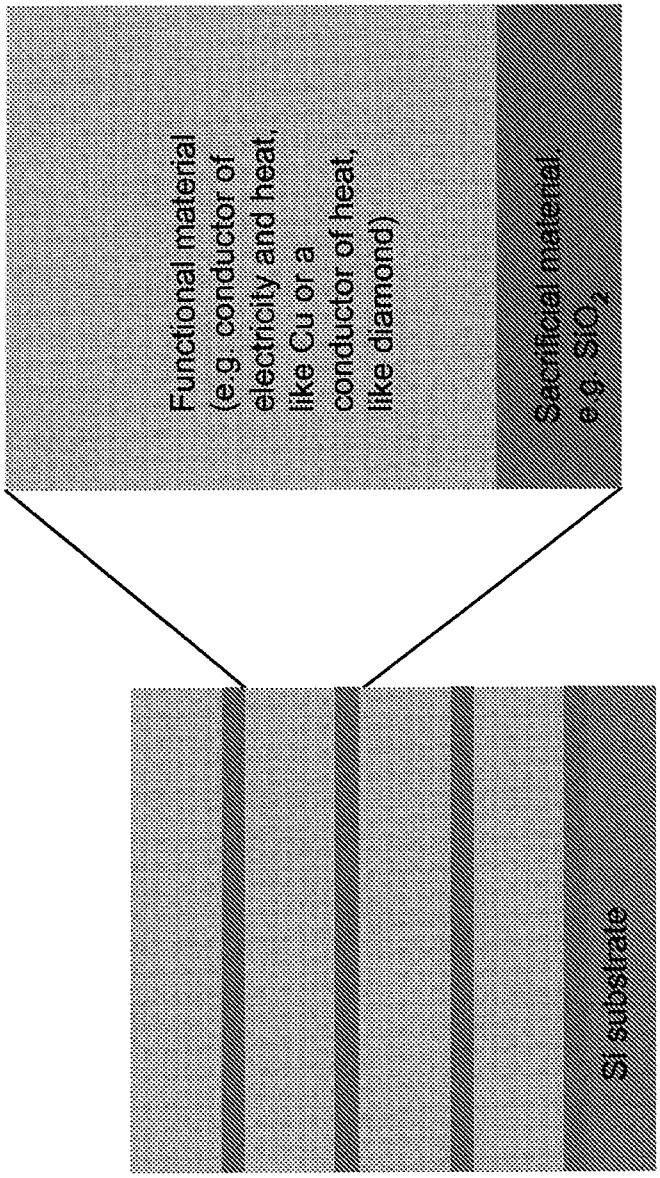

Functional material
(e.g. conductor of
electricity and heat,
like Cu or a
conductor of heat,
like diamond)
Sacrificial material,
e.g. SiO_2
Si substrate

FIG. 10

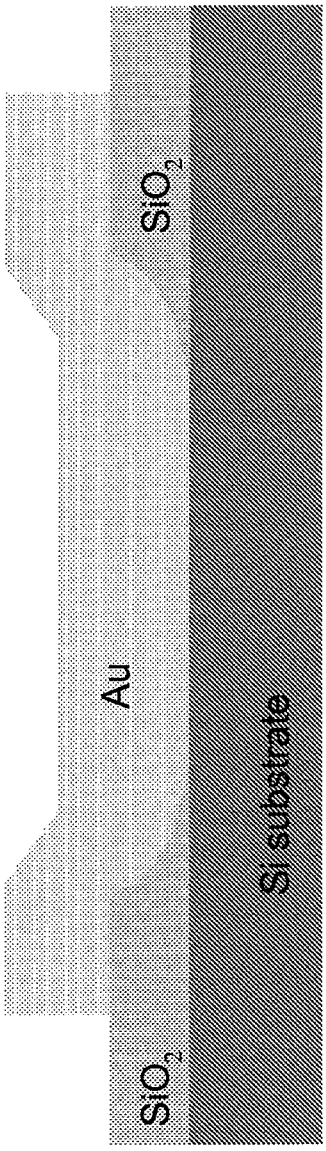


FIG. 11

Process flow 6: release of amorphous or polycrystalline FMED structures by removal of sacrificial layers.
See also FIG. 3B.

Can be done multiple layers at a time similar to FIG. 4 (process flow 1); here described as "one-layer-at-a time" similar to FIG. 5 (process flow 2).

1. obtain Si substrate

2. Grow layers described by FIG. 10 by sequential evaporation or CVD.

3. mask portion of the surface of the top layer with photoresist and some form of lithography for patterning.

4. Etch unmasked regions of top layer using the appropriate wet or dry etching to etch the functional material (e.g. $KI/I_2/H_2O$ for Au, oxygen plasma for diamond).

5. Expose the substrate to concentrated HF to at least partially remove the exposed sacrificial layer (SiO_2) and release the functional materials above the sacrificial layer (functional layers) by lateral undercutting. (HF attacks the functional functional materials (noble metals, diamond, silicon) more slowly (less than 1/10 etch rate) than it does the sacrificial layer.)

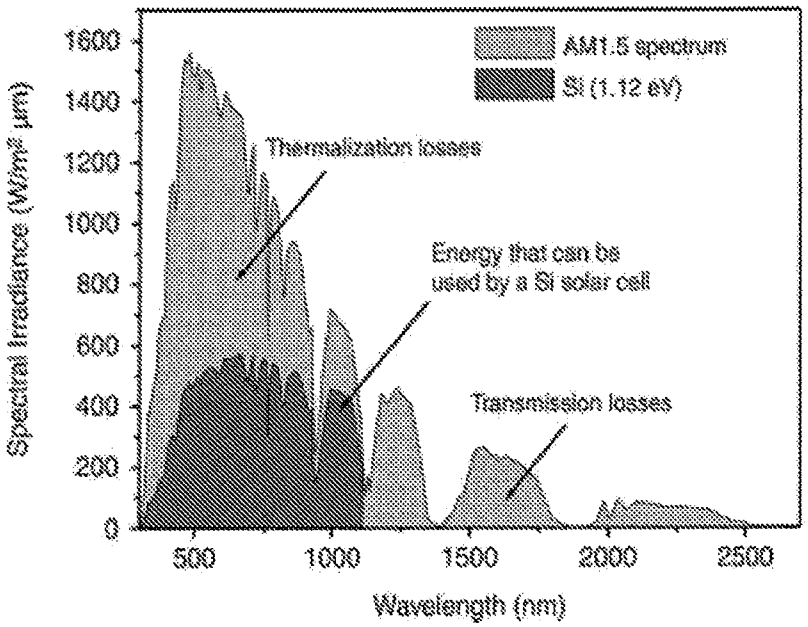
6. Separate the released FMEDs from substrate by stamping or do solvent exchange for fluidic assembly or ink jet printing, electrospinning, etc.

7. use HF to remove any remaining portions of the sacrificial layer; wash/rub away any remaining portions of the overlying functional epilayers (anchoring structures, etc.) the Functional layers that were originally directly underneath the first sacrificial layer are now exposed and on the surface of the substrate

8. Repeat steps 3 through 7, releasing sets of functional layers (each set separated by sacrificial layers) one at a time until no sacrificial layers remain on the substrate.

9. (optional, for re-use of substrate) Repeat steps 2 through 8 as desired.

FIG. 12


AM1.5 spectrum
Si (1.12 eV)
Thermalization losses
Energy that can be used by a Si solar cell
Transmission losses
Spectral Irradiance (W/m² μm)
Wavelength (nm)
0
200
400
600
800
1000
1200
1400
1600
500
1000
1500
2000
2500

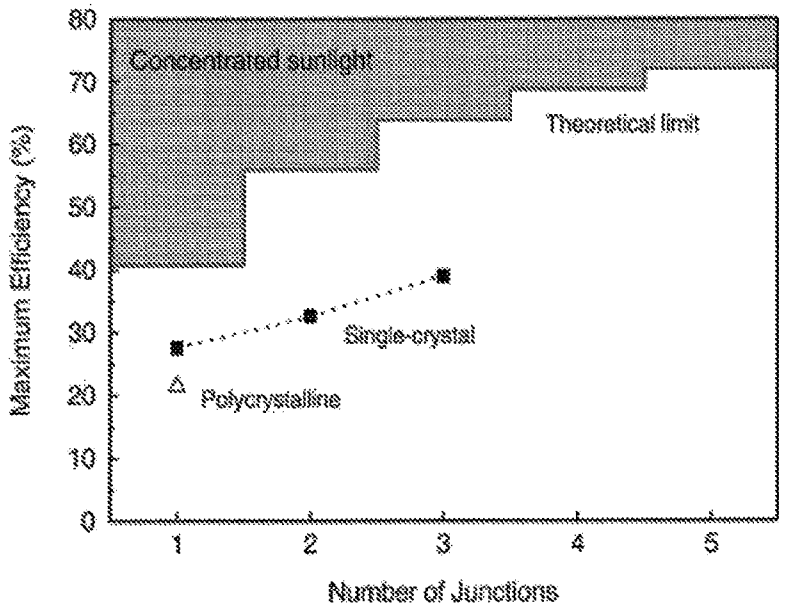

Concentrated sunlight
Theoretical limit
Single-crystal
Polycrystalline
Maximum Efficiency (%)
Number of Junctions
0
10
20
30
40
50
60
70
80
1
2
3
4
5

FIG. 13

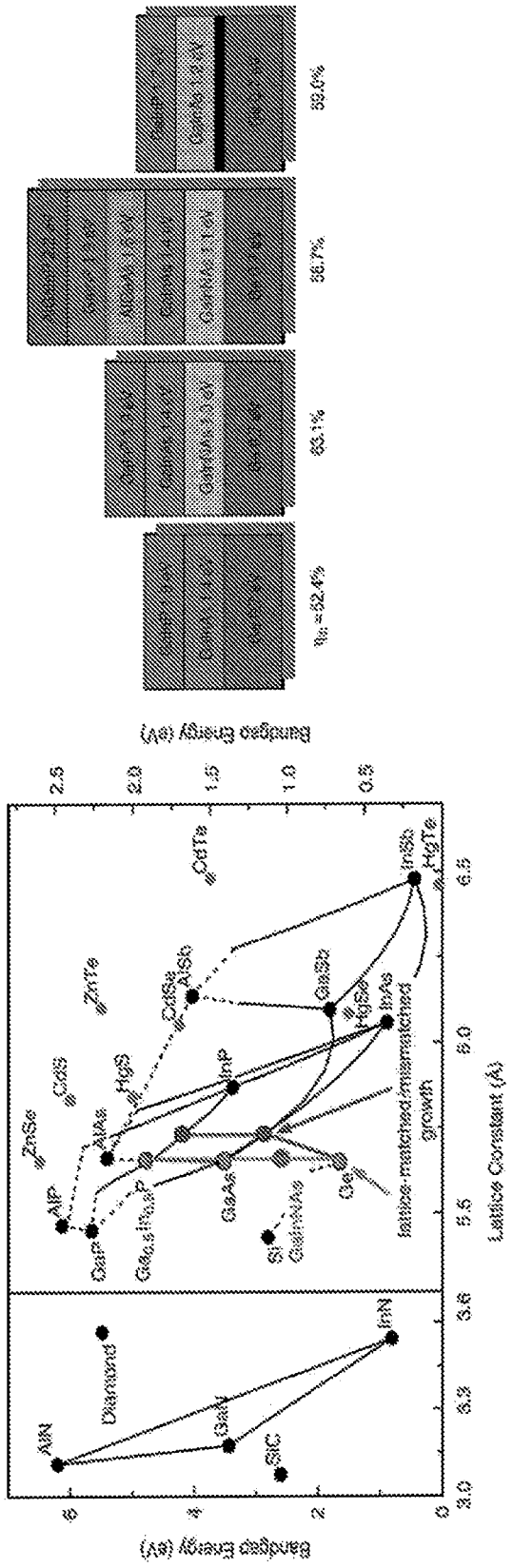

Bandgap Energy (eV)
Lattice Constant (Å)
AlN
Diamond
GaN
InN
SiC
AlP
GaP
ZnSe
CdS
AlAs
HgS
InP
ZnTe
CdSe
AlSb
CdTe
GaSb
HgSe
InAs
InSb
HgTe
Si
GaInNAs
GaAs
Ge
lattice-matched/mismatched growth
Bandgap Energy (eV)
η_{tc} = 52.4%
63.1%
36.7%
39.6%

FIG. 14

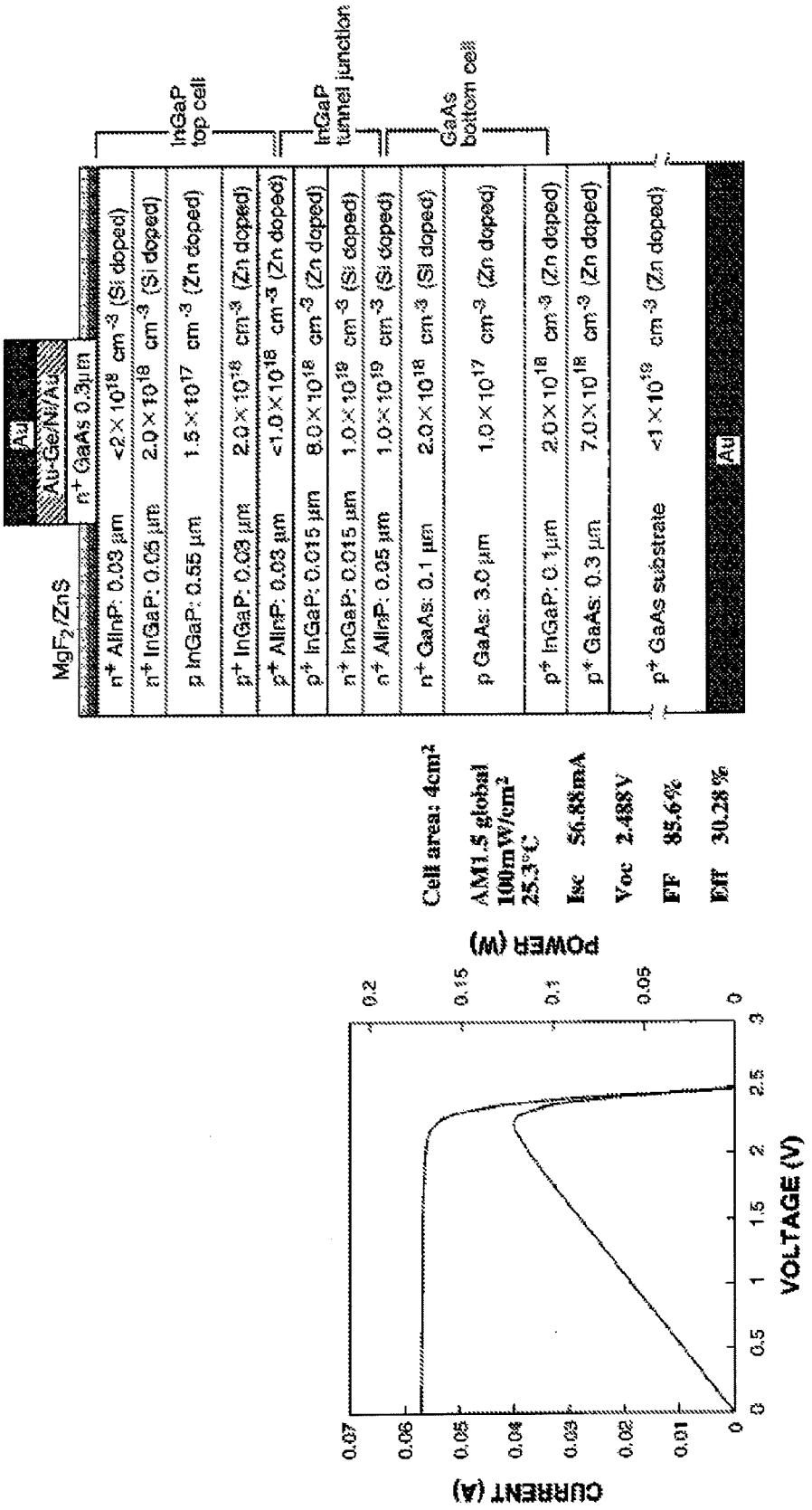

MgF2/ZnS
Au
Au-Ge/Ni/Au
n+ GaAs 0.3μm
n+ AlInP: 0.03 μm <2×10^18 cm^-3 (Si doped)
n+ InGaP: 0.05 μm 2.0×10^18 cm^-3 (Si doped)
p InGaP: 0.55 μm 1.5×10^17 cm^-3 (Zn doped)
InGaP top cell
p+ InGaP: 0.03 μm 2.0×10^18 cm^-3 (Zn doped)
p+ AlInP: 0.03 μm <1.0×10^18 cm^-3 (Zn doped)
InGaP tunnel junction
p+ InGaP: 0.015 μm 8.0×10^18 cm^-3 (Zn doped)
n+ InGaP: 0.015 μm 1.0×10^19 cm^-3 (Si doped)
n+ AlInP: 0.05 μm 1.0×10^19 cm^-3 (Si doped)
n+ GaAs: 0.1 μm 2.0×10^18 cm^-3 (Si doped)
p GaAs: 3.0 μm 1.0×10^17 cm^-3 (Zn doped)
GaAs bottom cell
p+ InGaP: 0.1μm 2.0×10^18 cm^-3 (Zn doped)
p+ GaAs: 0.3 μm 7.0×10^18 cm^-3 (Zn doped)
p+ GaAs substrate <1×10^19 cm^-3 (Zn doped)
Au
Cell area: 4cm²
AM1.5 global
100mW/cm²
25.3°C
Isc 56.88mA
Voc 2.488V
FF 85.6%
Eff 30.28%
POWER (W)
CURRENT (A)
VOLTAGE (V)

FIG. 15

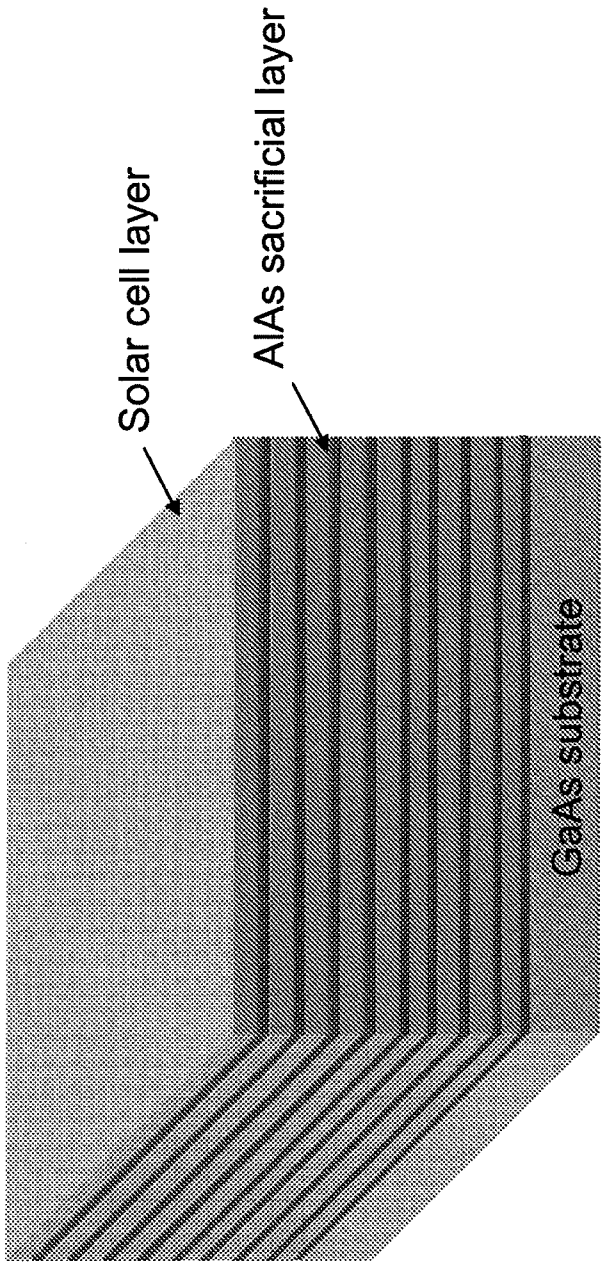


FIG. 16

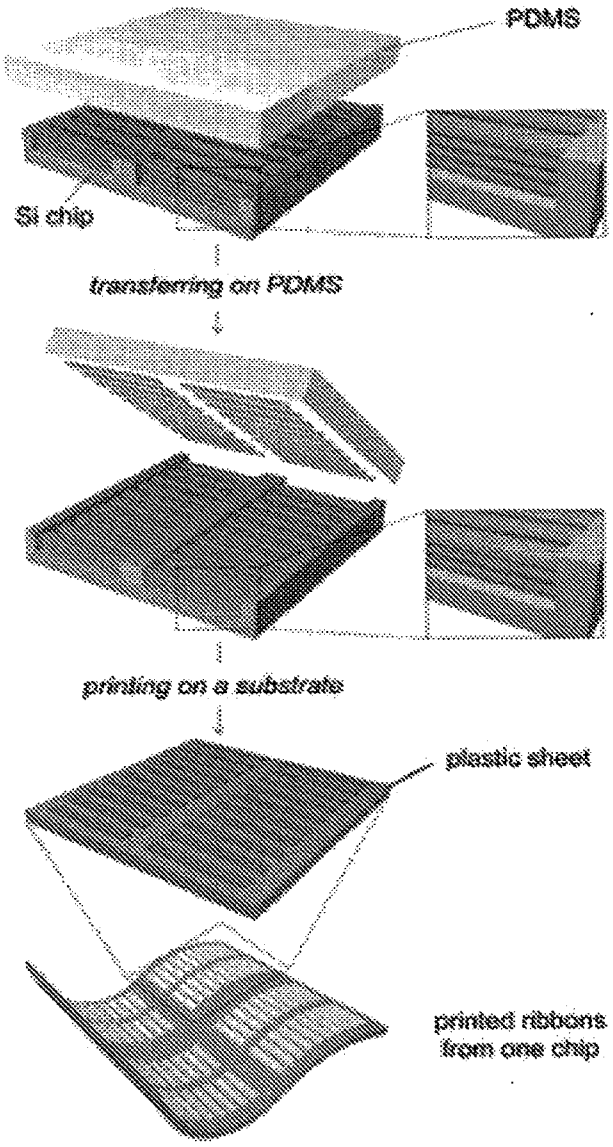

PDMS
Si chip
transferring on PDMS
printing on a substrate
plastic sheet
printed ribbons
from one chip

FIG. 17

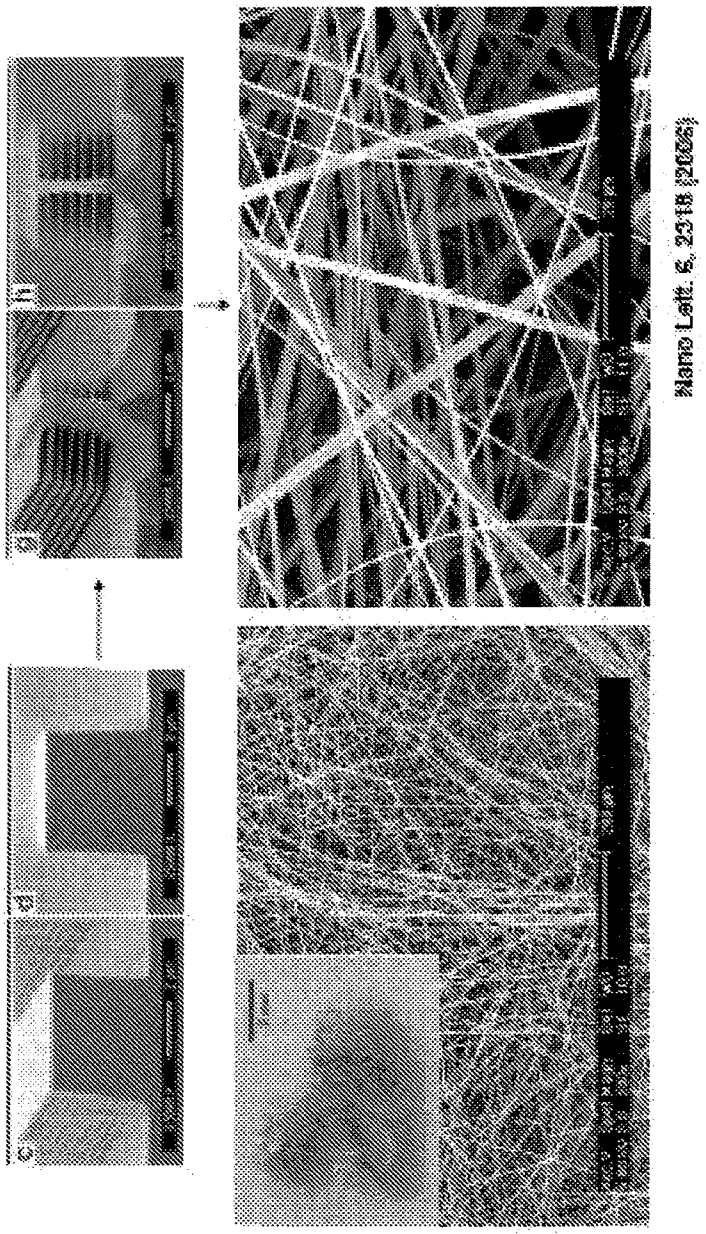
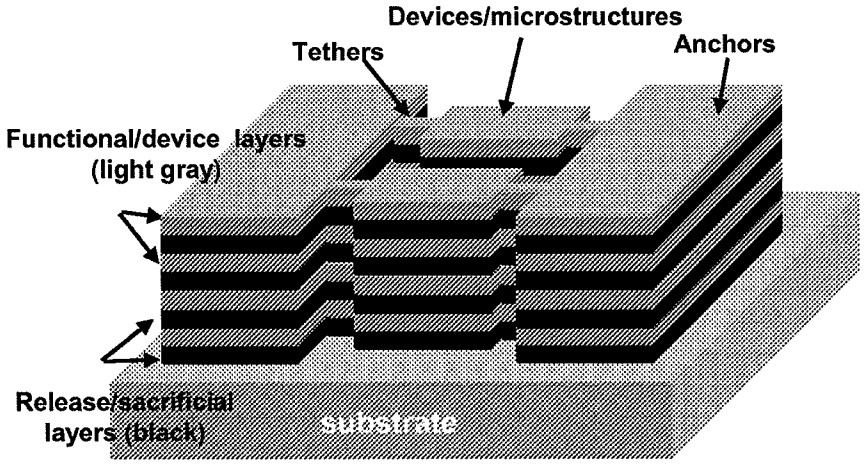


FIG. 18

Step 1: Define devices, tethers and anchors in multilayer structure (e.g. by photolithography and etching)



Step 2: Partially release functional layers by partially removing sacrificial release layers laterally (e.g. by etching), undercutting tethers and devices but not anchors.

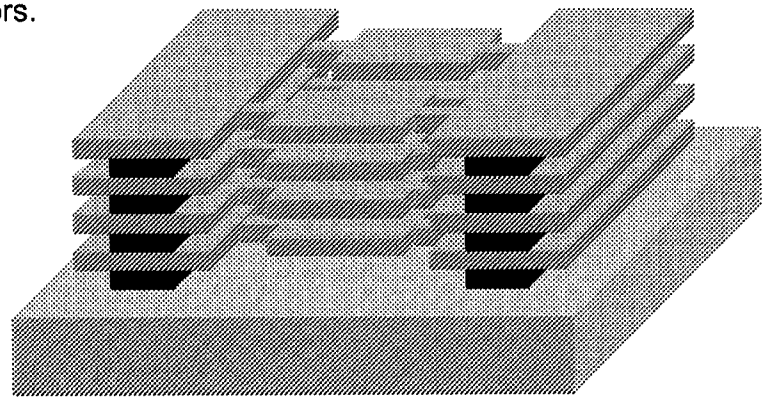
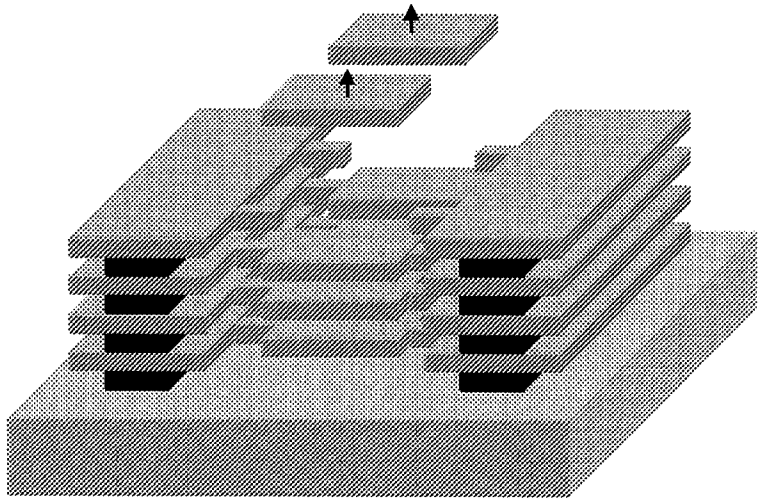


FIG. 19

Step 3: Remove top devices by fracture at tethers, e.g. using a rubber stamp.



Step 4: Repeat step three to remove the remainder of devices.

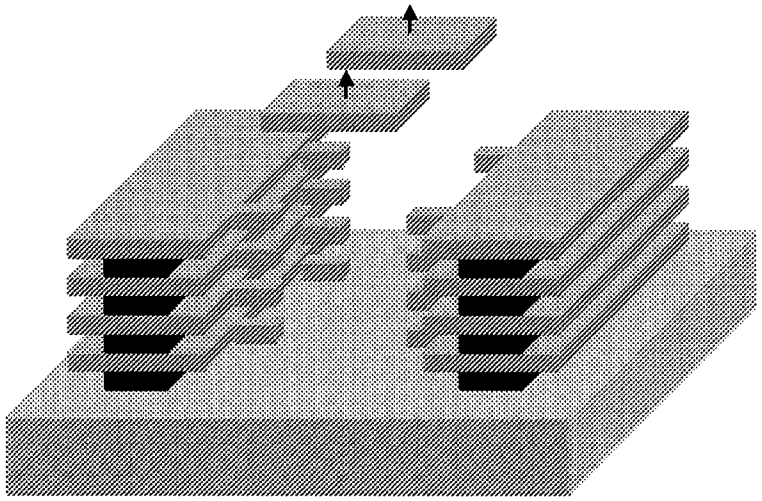
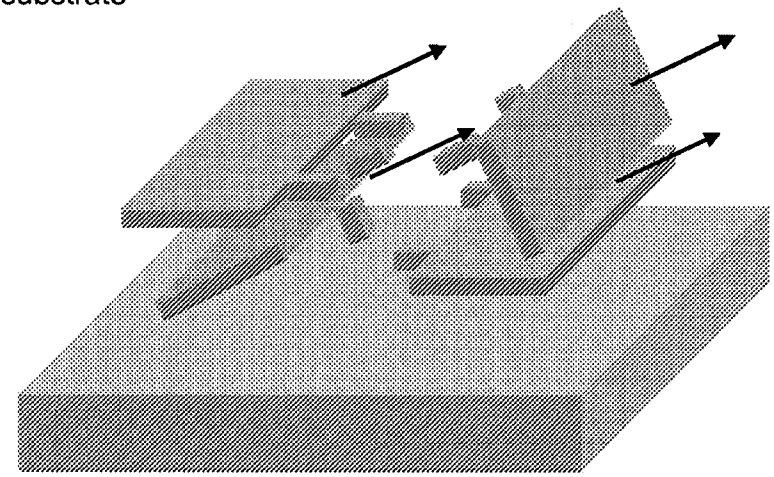


FIG. 19 (cont'd)

Step 5: Apply a combination of etching, scrubbing, and optionally polishing, to remove anchoring structures from substrate



Step 6: ***(optional)*** Re-grow multilayer stack. The system is now ready for repetition of steps 1 through 5

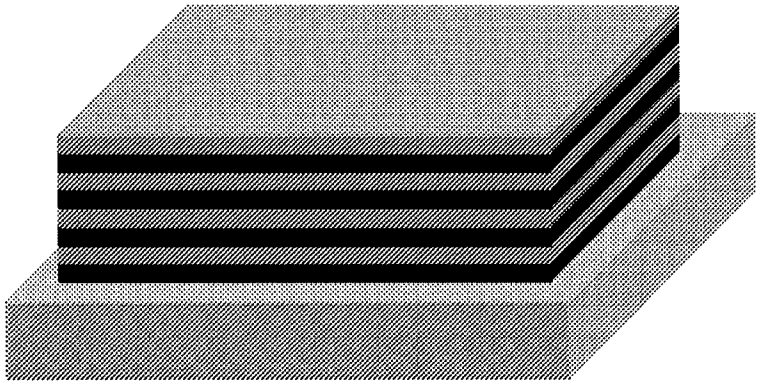
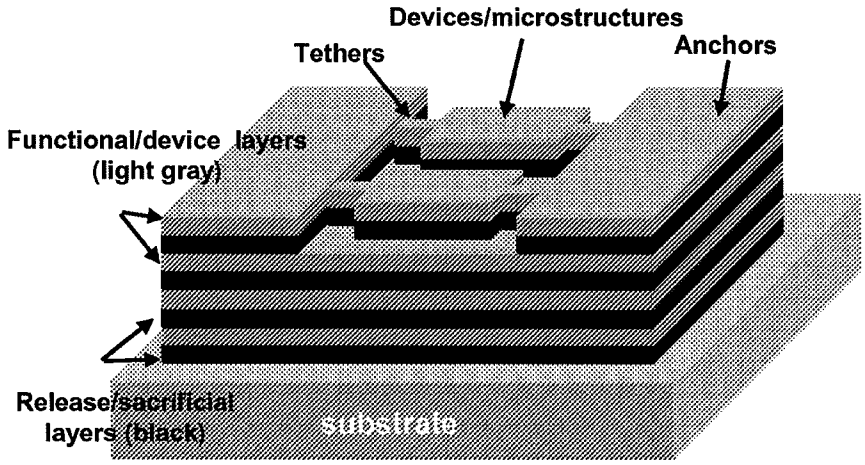


FIG. 19 (cont'd)

Step 1: Define devices, tethers and anchors in top functional layer (and optionally underlying release layer) of multilayer structure (e.g. by photolithography and etching)



Step 2: Partially release top functional layer by partially removing underlying sacrificial release layer laterally (e.g. by etching), undercutting tethers and devices but not anchors.

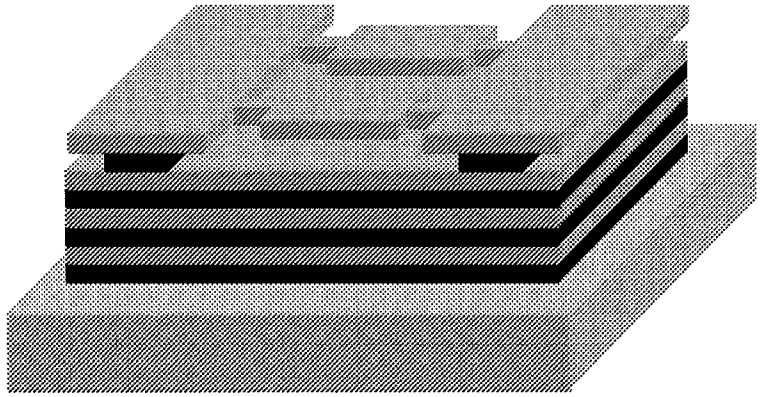
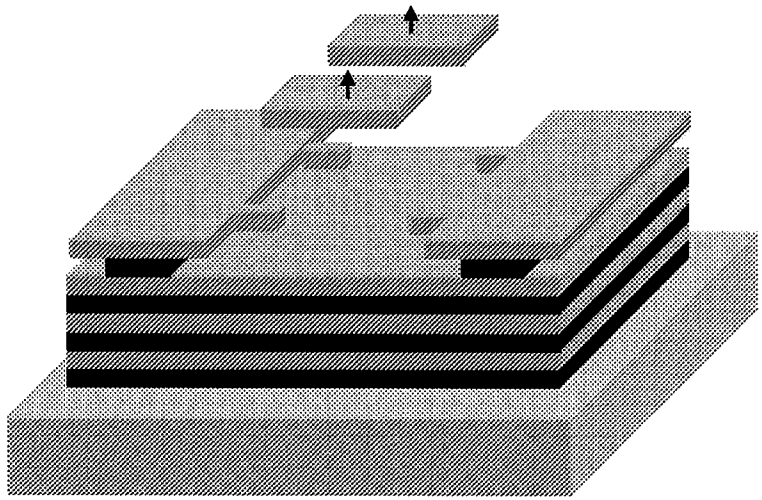


FIG. 20

Step 3: Remove top devices by fracture at tethers, e.g. using a rubber stamp.



Step 4: Apply a combination of etching and scrubbing to remove anchoring structures from substrate

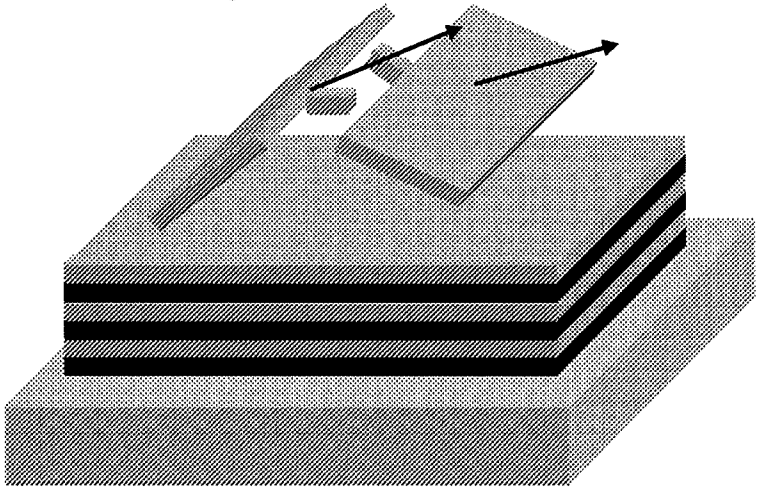


FIG. 20 (cont'd)

Step 5: Repeat steps 1 through 4 until all functional layers and release layers are removed from substrate

Step 6: ***(optional)*** Re-grow multilayer stack. The system is now ready for repetition of steps 1 through 5

FIG. 20 (cont'd)

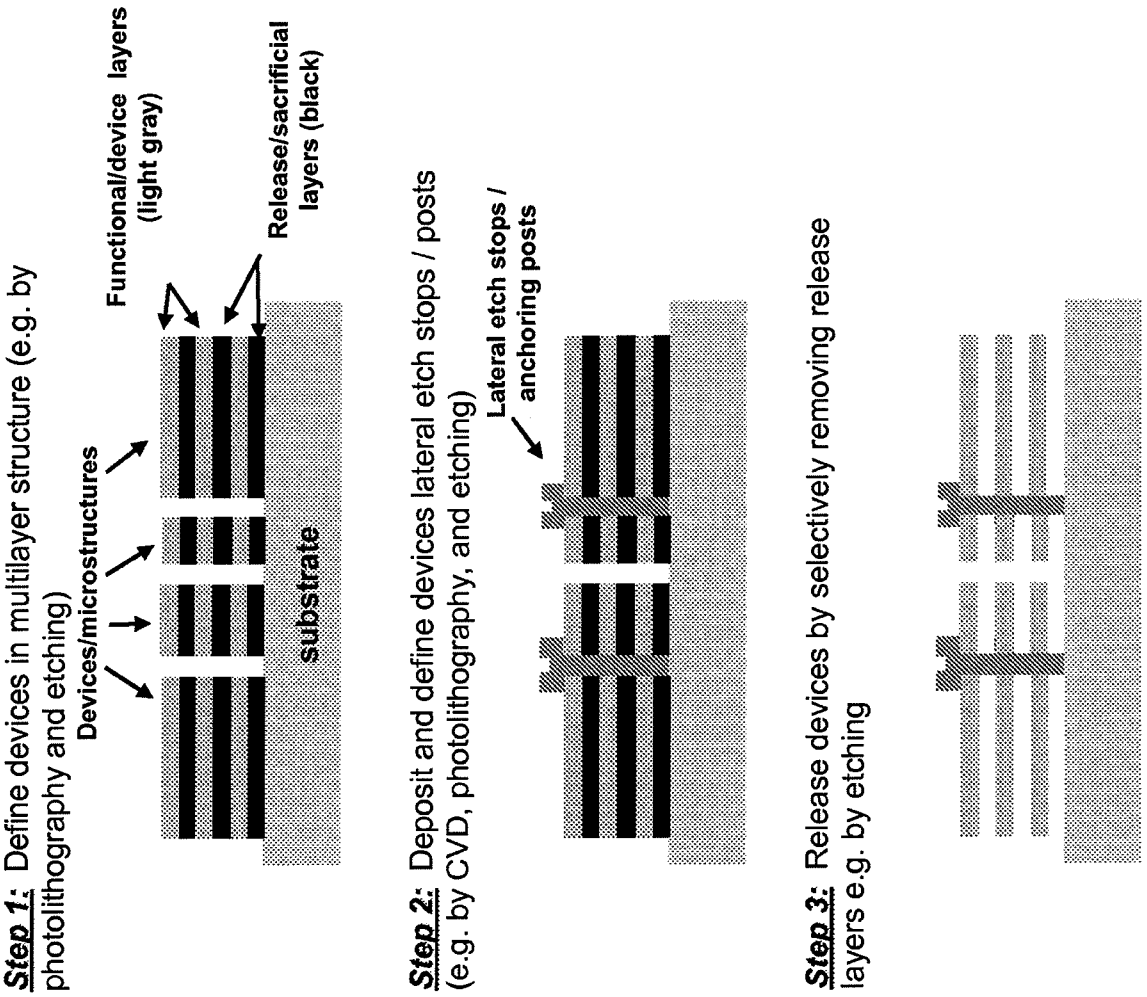
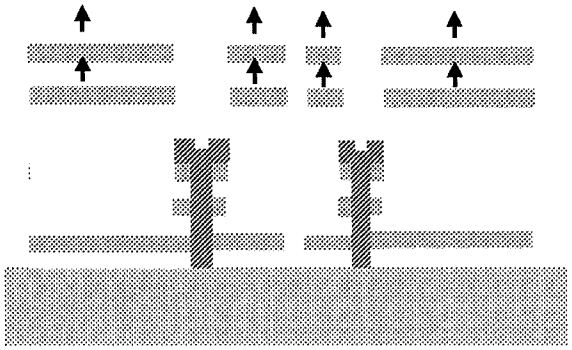
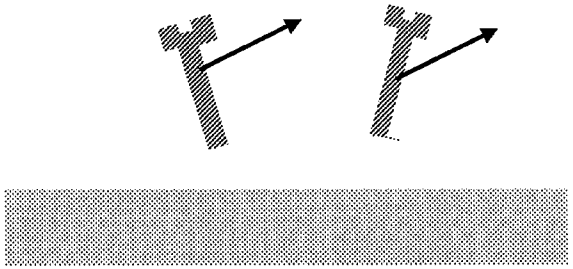

Step 1: Define devices in multilayer structure (e.g. by photolithography and etching)
Devices/microstructures
Functional/device layers (light gray)
Release/sacrificial layers (black)
substrate
Step 2: Deposit and define devices lateral etch stops / posts (e.g. by CVD, photolithography, and etching)
Lateral etch stops / anchoring posts
Step 3: Release devices by selectively removing release layers e.g. by etching

FIG. 21

Step 4: Sequentially remove layers of devices, e.g. using a rubber stamp, or relase into solution for printing.



Step 5: Apply a combination of etching and scrubbing (optionally polishing or grinding) to remove lateral etch stop/ anchoring posts from substrate.



Step 6 (optional): Grow multilayer on substrate; repeat steps 1 through 5

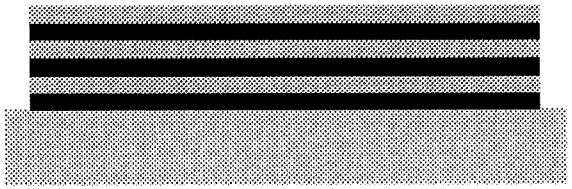
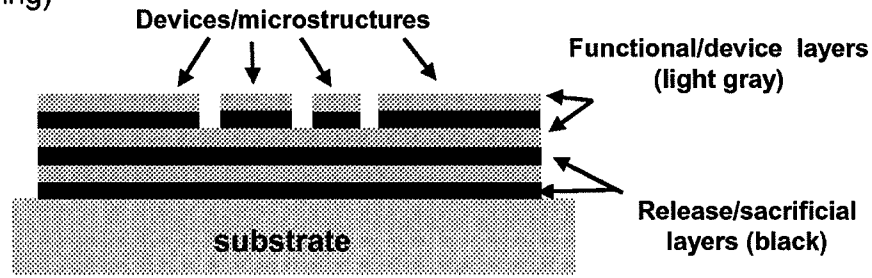
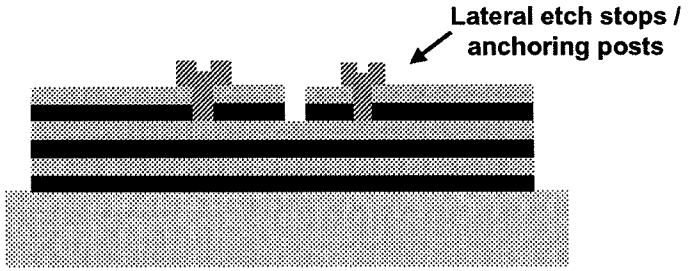


FIG. 21 (cont'd)

Step 1: Define devices in top functional layer and underlying release layer of multilayer structure (e.g. by photolithography and etching)



Step 2: Deposit and define devices lateral etch stops / posts (e.g. by CVD, photolithography, and etching)



Step 3: Release devices by selectively removing release layers e.g. by etching

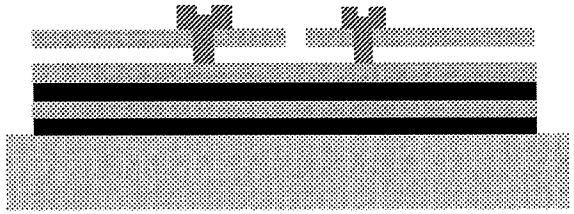
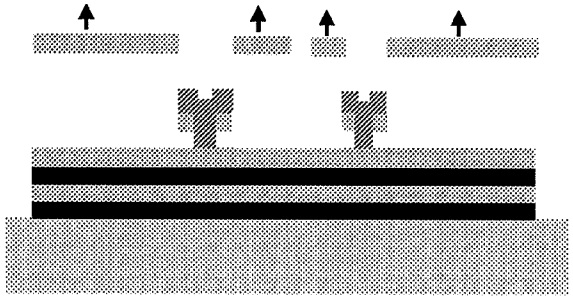
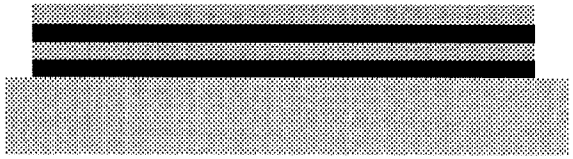


FIG. 22

Step 4: Remove released devices, e.g. using a rubber stamp, or relase into solution for printing.



Step 5: Apply a combination of etching and scrubbing to remove lateral etch stop/ anchoring posts from substrate.



Step 6 : repeat steps 1 through 5 until multilayer is entirely removed from substrate; optionally grow new multilayer stack and repeat steps.

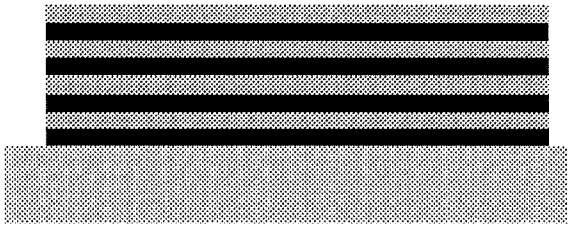
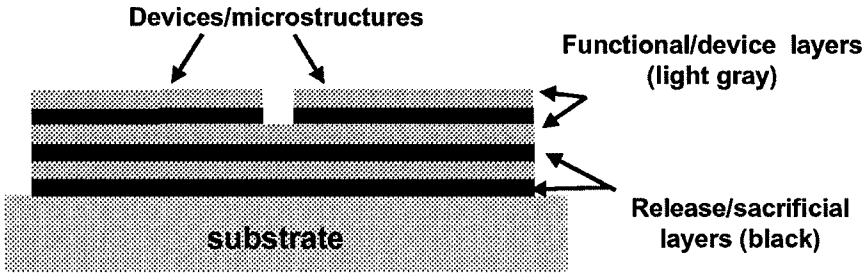
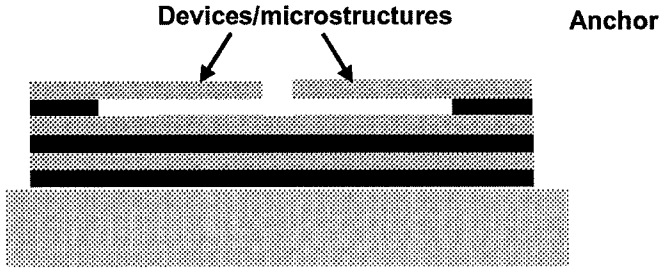


FIG. 22 (cont'd)

Step 1: Define devices in top functional layer and underlying release layer of multilayer structure (e.g. by photolithography and etching)



Step 2: Release devices partially, leaving anchored regions, by laterally removing sacrificial layer



Step 3: Deposit/generate anti-stiction or activation layer (e.g. self-assembled monolayer) by vapor or solution methods

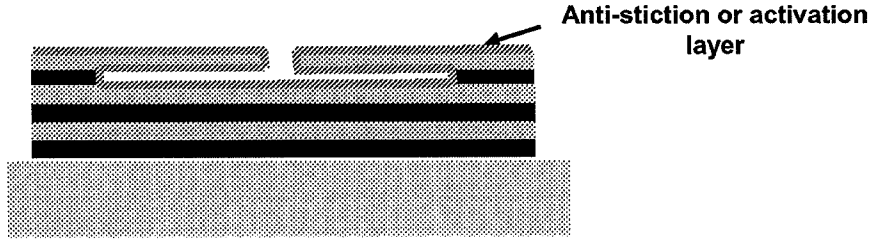


FIG. 23

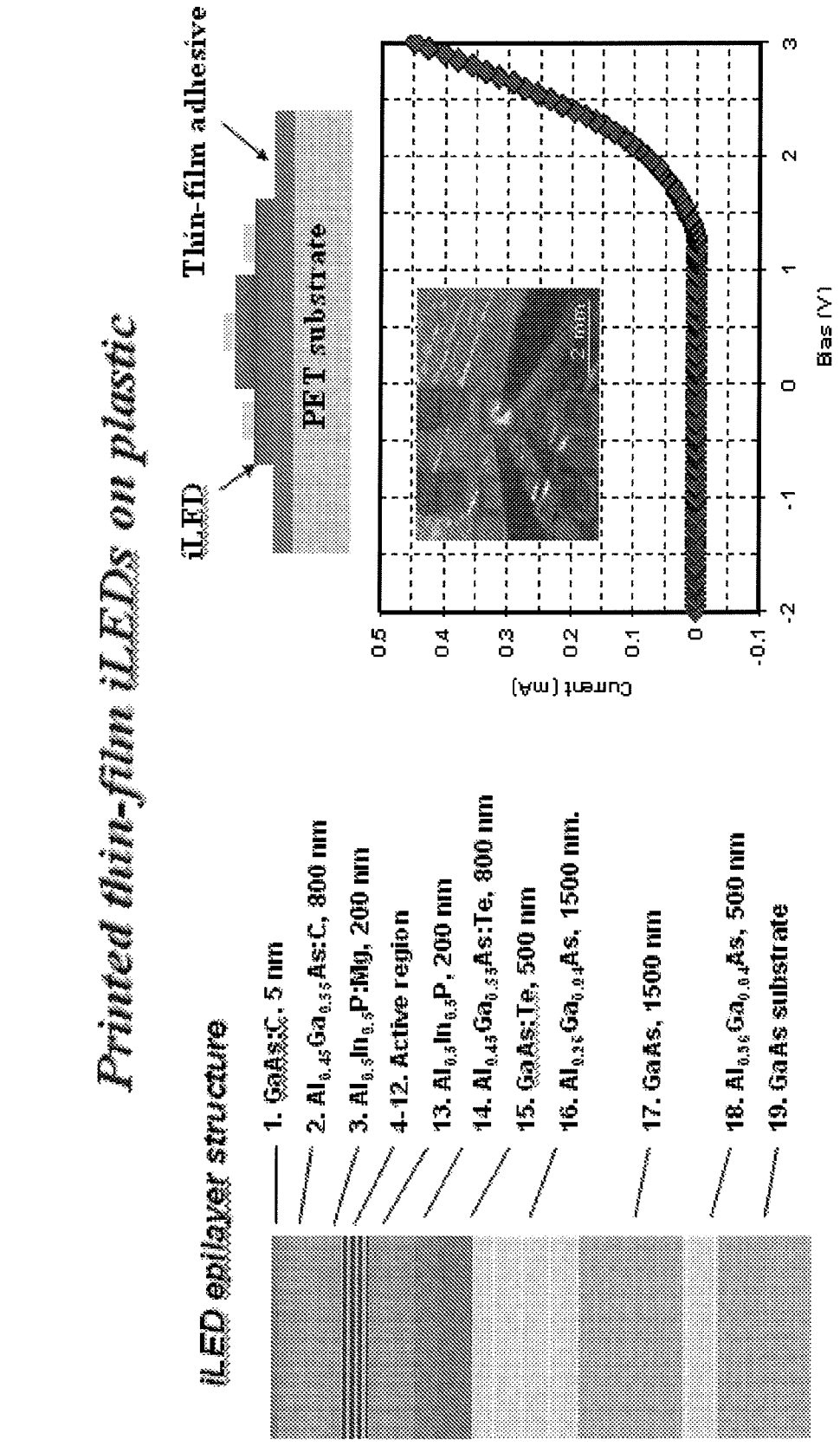

Printed thin-film iLEDs on plastic
iLED epilayer structure
1. GaAs:C, 5 nm
2. $Al_{0.45}Ga_{0.55}As$:C, 800 nm
3. $Al_{0.5}In_{0.5}P$:Mg, 200 nm
4-12. Active region
13. $Al_{0.5}In_{0.5}P$, 200 nm
14. $Al_{0.45}Ga_{0.55}As$:Te, 800 nm
15. GaAs:Te, 500 nm
16. $Al_{0.25}Ga_{0.4}As$, 1500 nm.
17. GaAs, 1500 nm
18. $Al_{0.36}Ga_{0.4}As$, 500 nm
19. GaAs substrate
iLED
Thin-film adhesive
PET substrate
24 um
Current (mA)
Bias (V)

FIG. 24

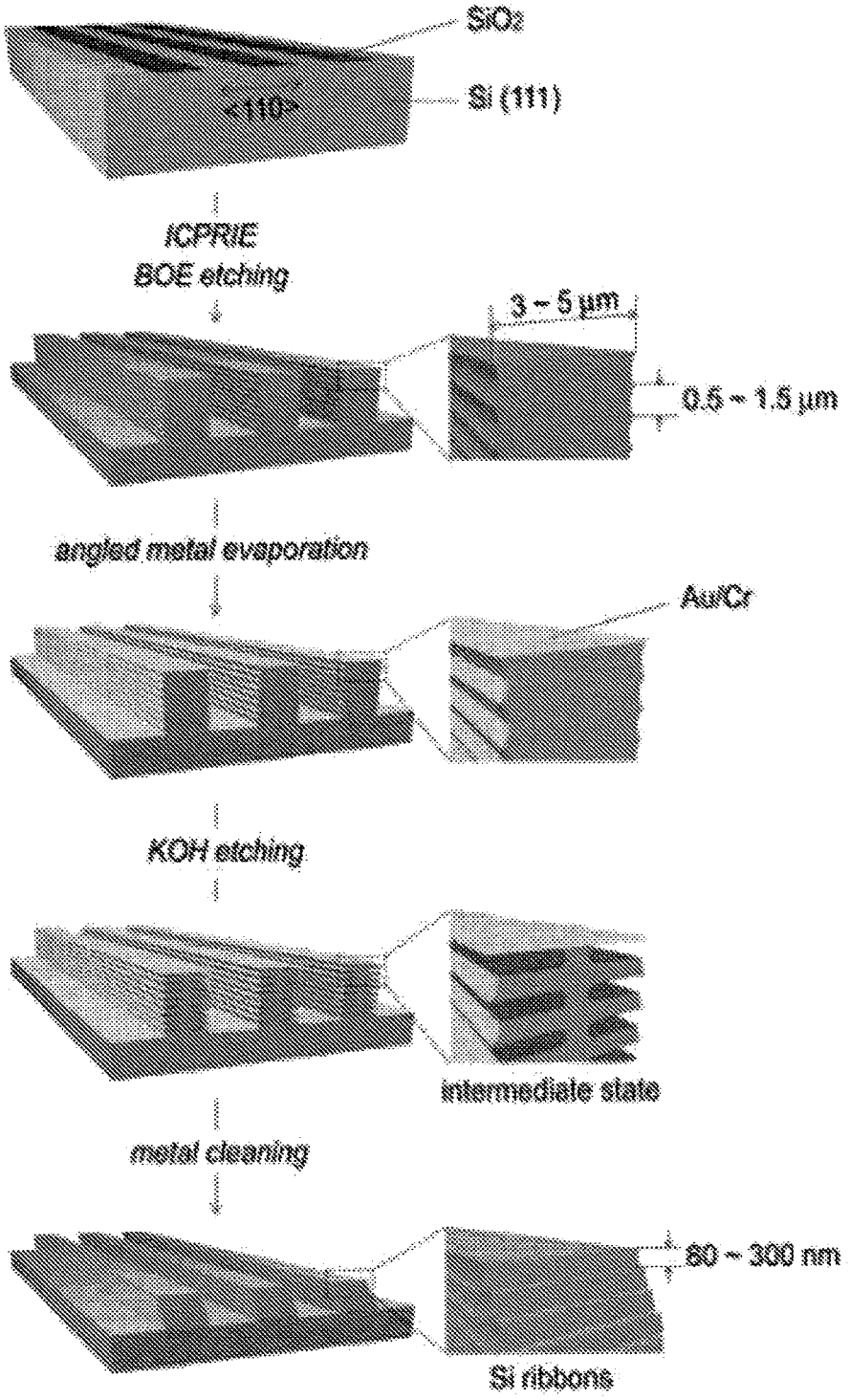

SiO2
Si (111)
<110>
ICPRIE
BOE etching
3 ~ 5 μm
0.5 ~ 1.5 μm
angled metal evaporation
Au/Cr
KOH etching
intermediate state
metal cleaning
80 ~ 300 nm
Si ribbons

FIG. 25

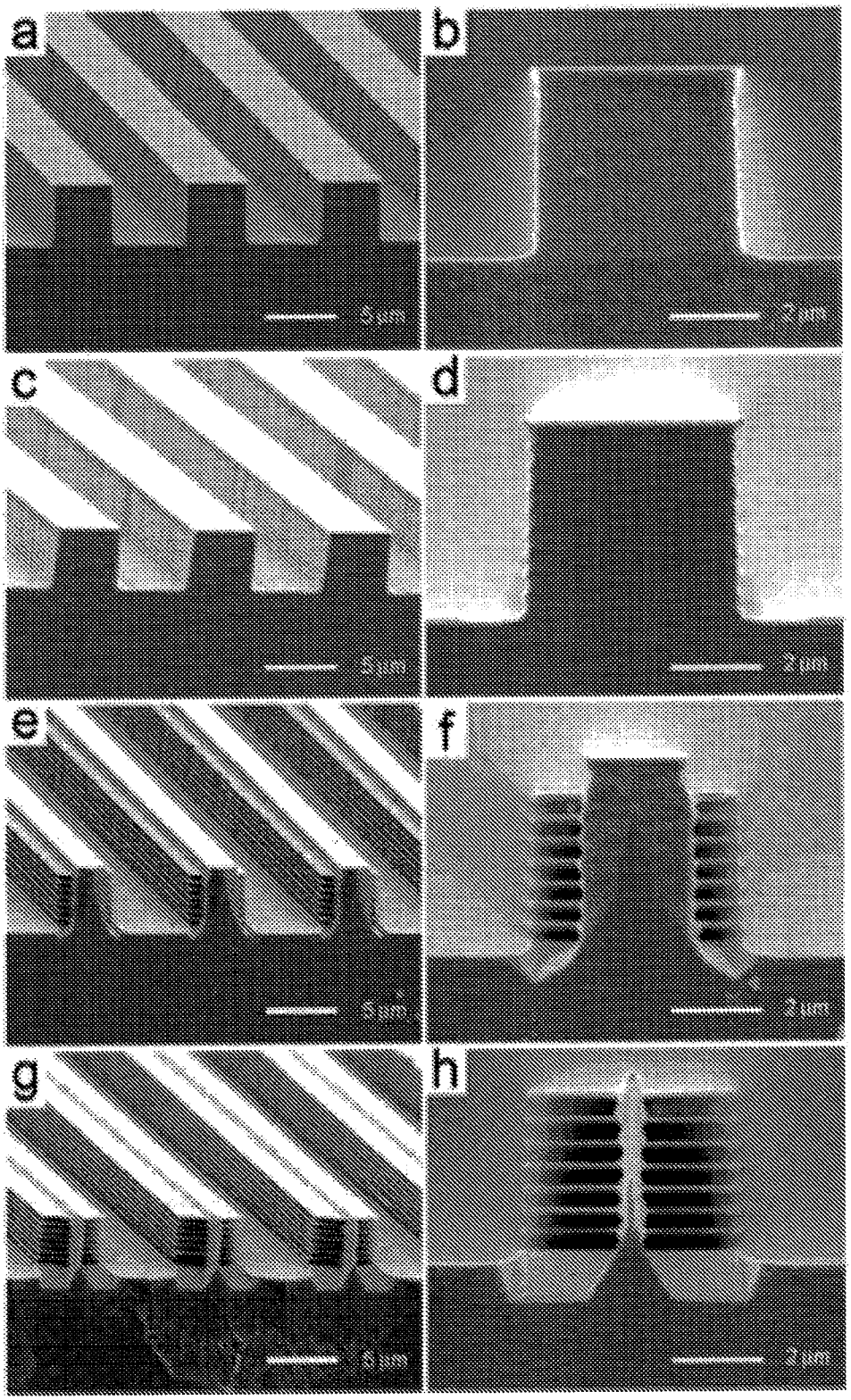


FIG. 26

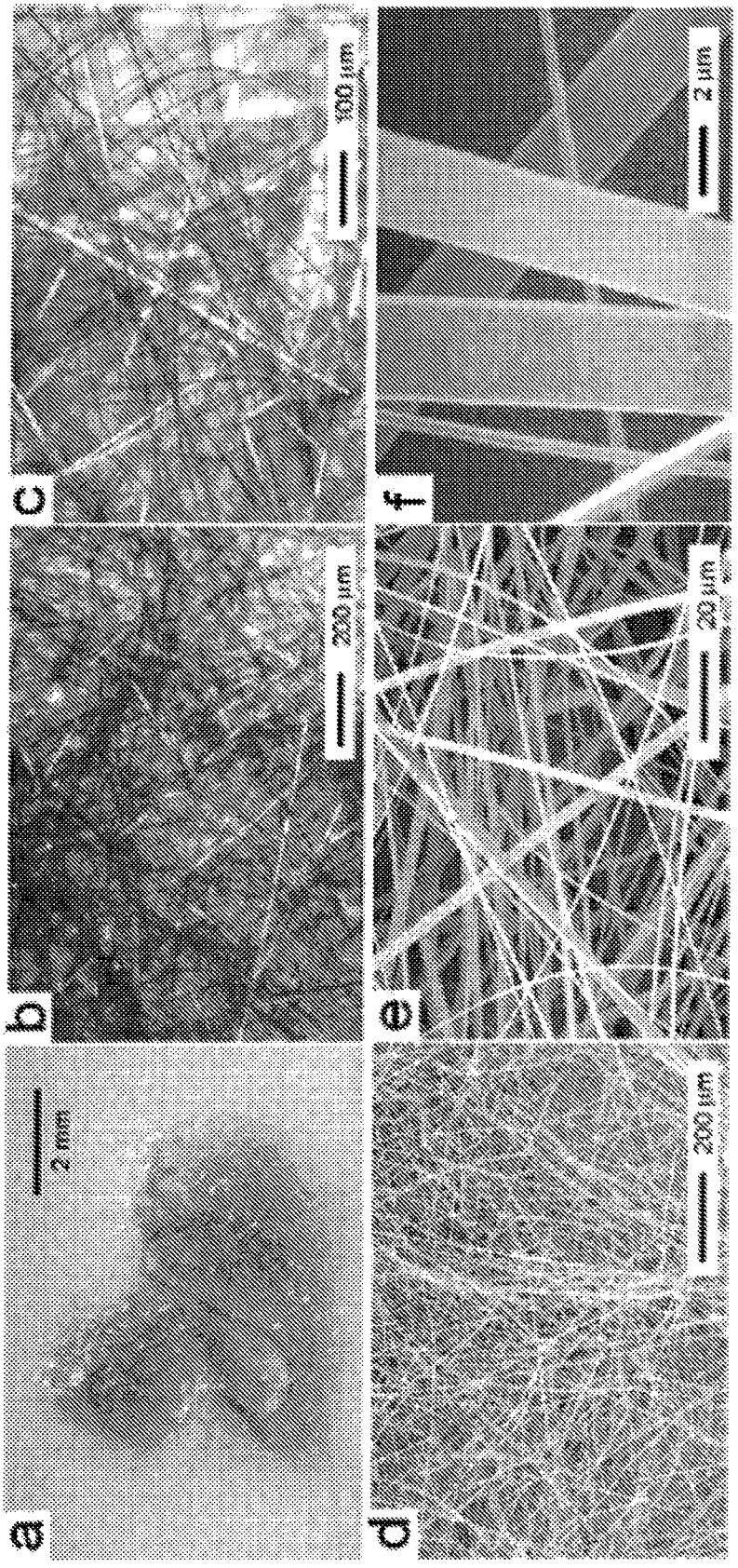


FIG. 27

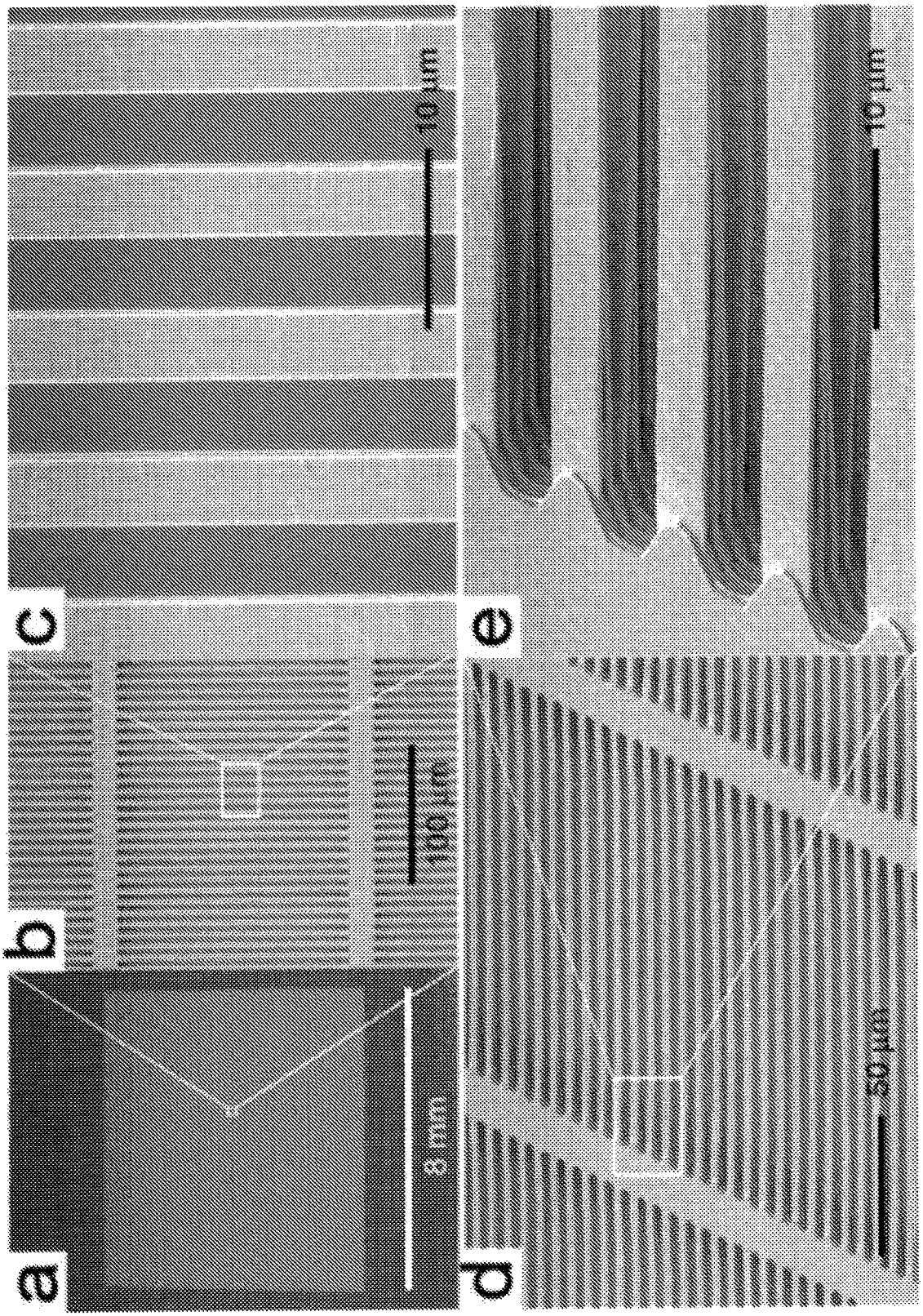


FIG. 28

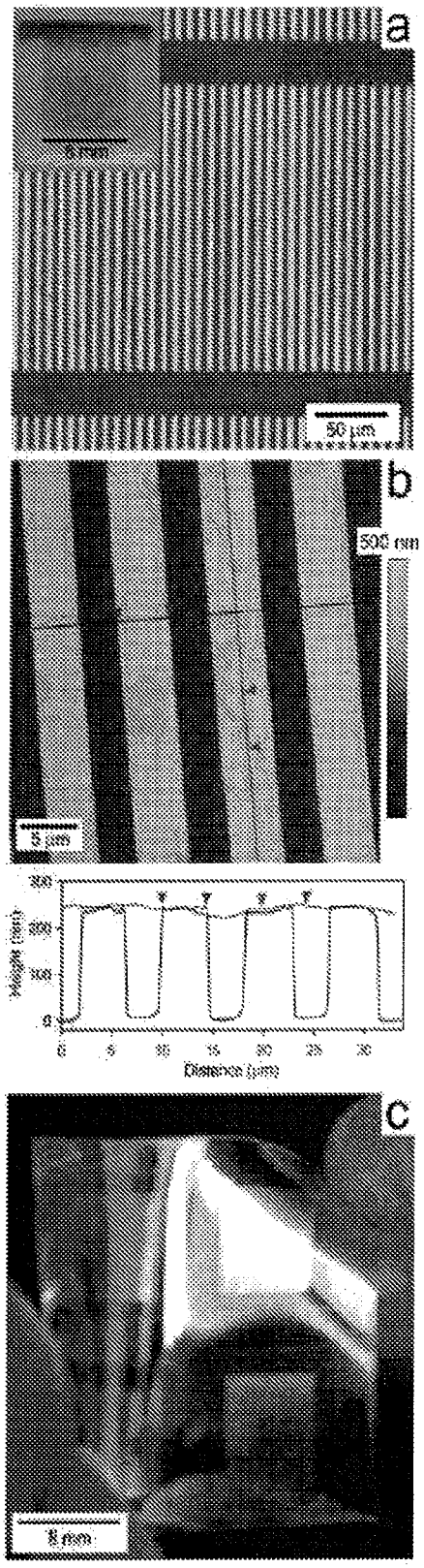


FIG. 29

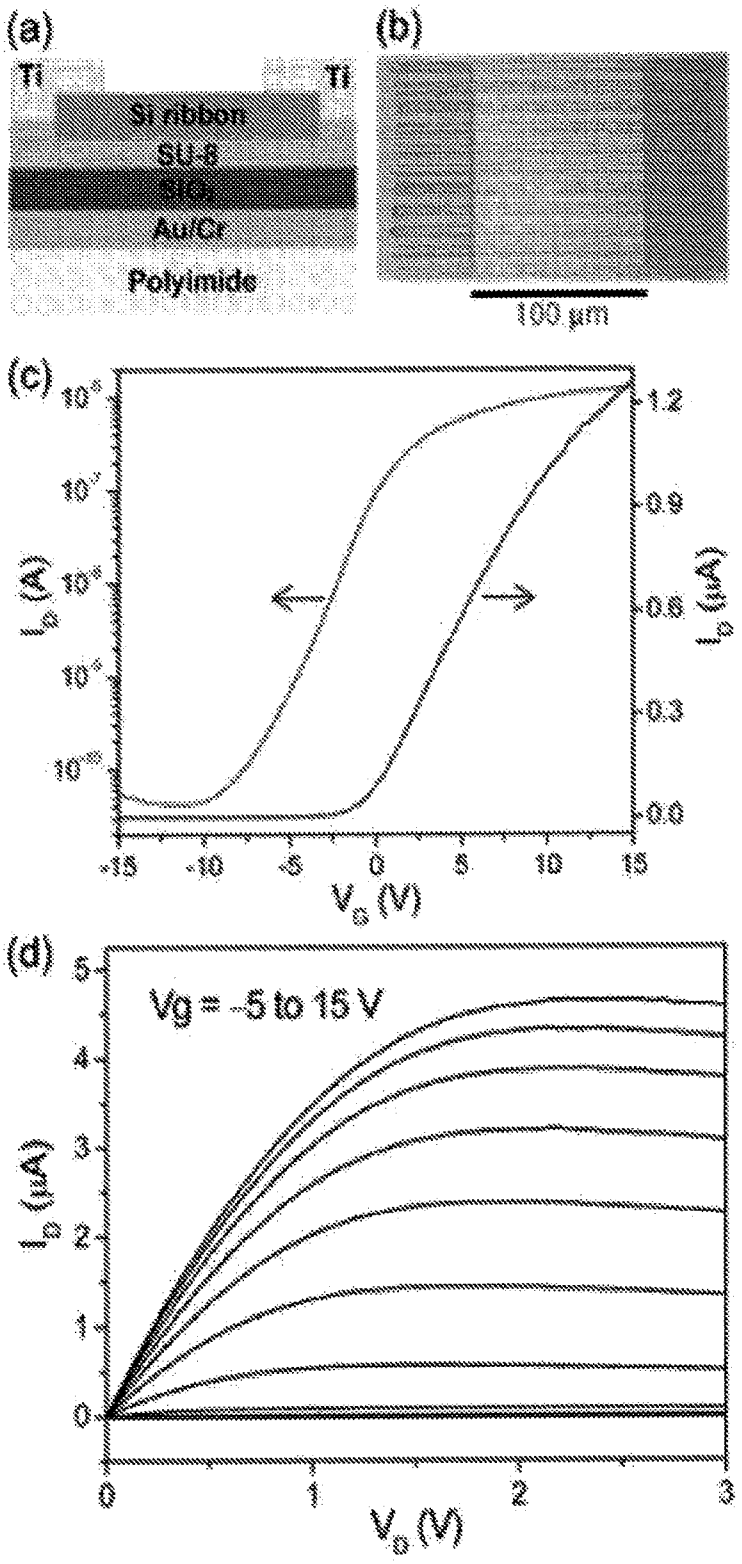

(a)
Ti
Ti
Si ribbon
SU-8
SiO2
Au/Cr
Polyimide
(b)
100 μm
(c)
I_{ds} (A)
I_D (μA)
V_G (V)
(d)
Vg = -5 to 15 V
I_D (μA)
V_D (V)

FIG. 30

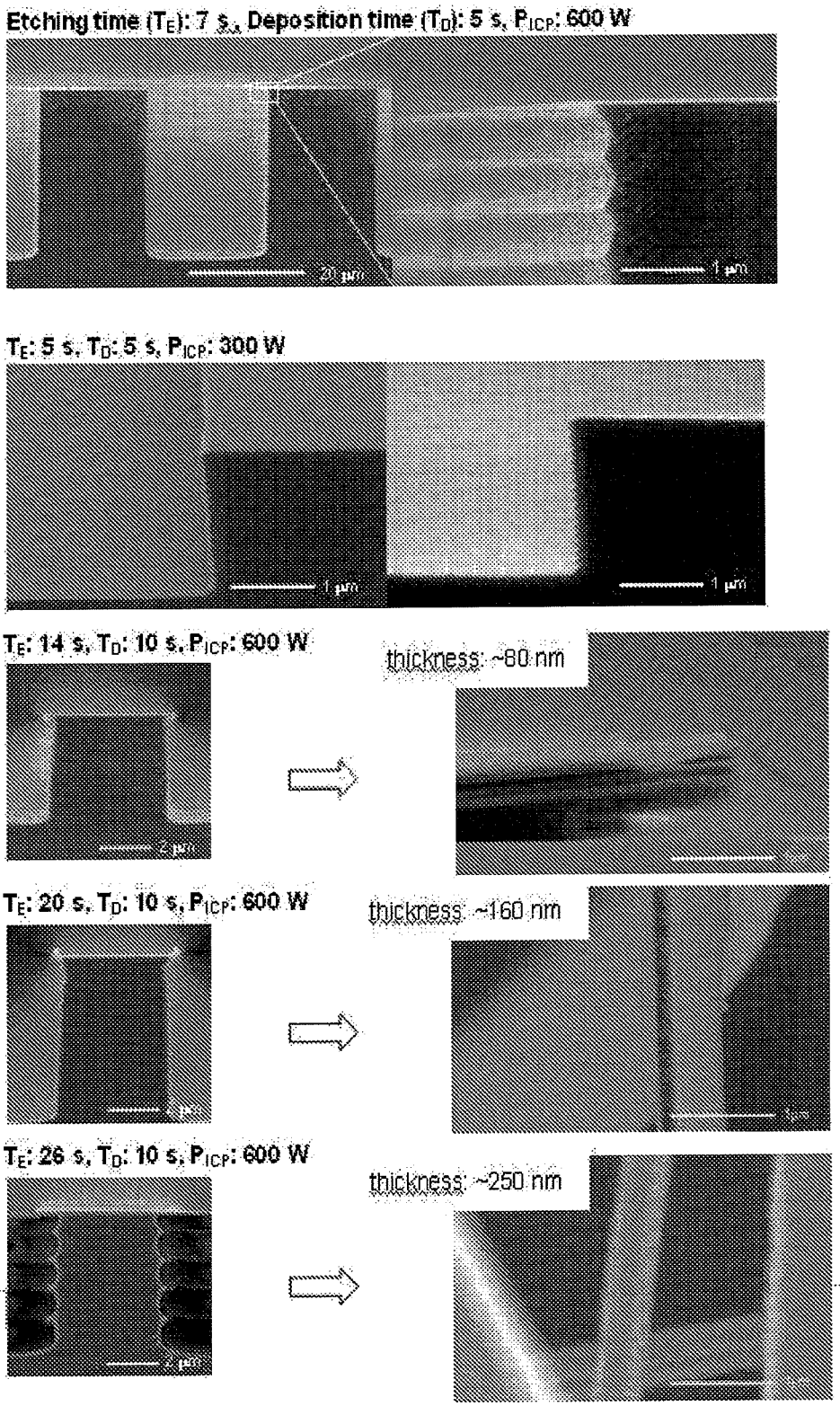

Etching time (T_E): 7 s, Deposition time (T_D): 5 s, P_{ICP}: 600 W
T_E: 5 s, T_D: 5 s, P_{ICP}: 300 W
T_E: 14 s, T_D: 10 s, P_{ICP}: 600 W
thickness: ~80 nm
T_E: 20 s, T_D: 10 s, P_{ICP}: 600 W
thickness: ~160 nm
T_E: 26 s, T_D: 10 s, P_{ICP}: 600 W
thickness: ~250 nm

FIG. 31

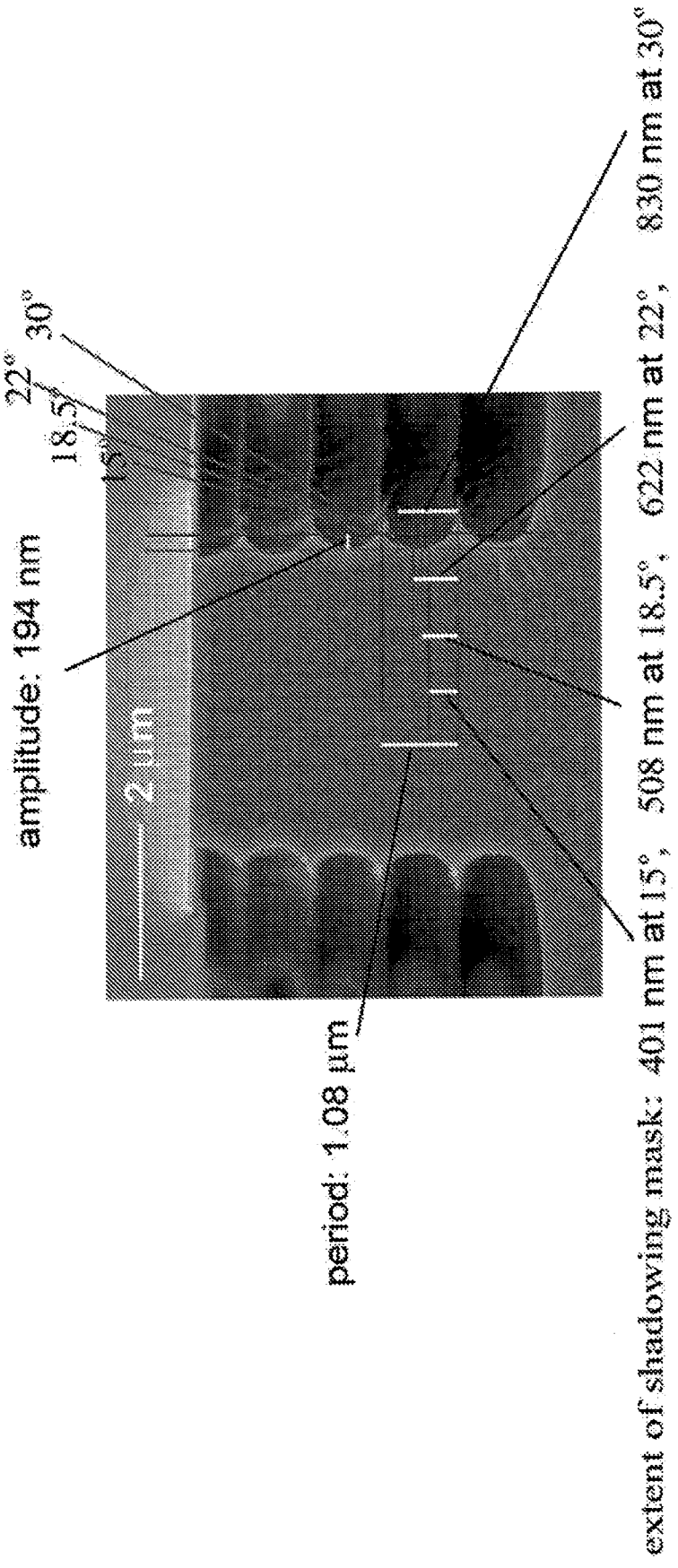

22°
30°
18.5°
15°
amplitude: 194 nm
2 μm
period: 1.08 μm
extent of shadowing mask: 401 nm at 15°, 508 nm at 18.5°, 622 nm at 22°, 830 nm at 30°

FIG. 32



FIG. 33A

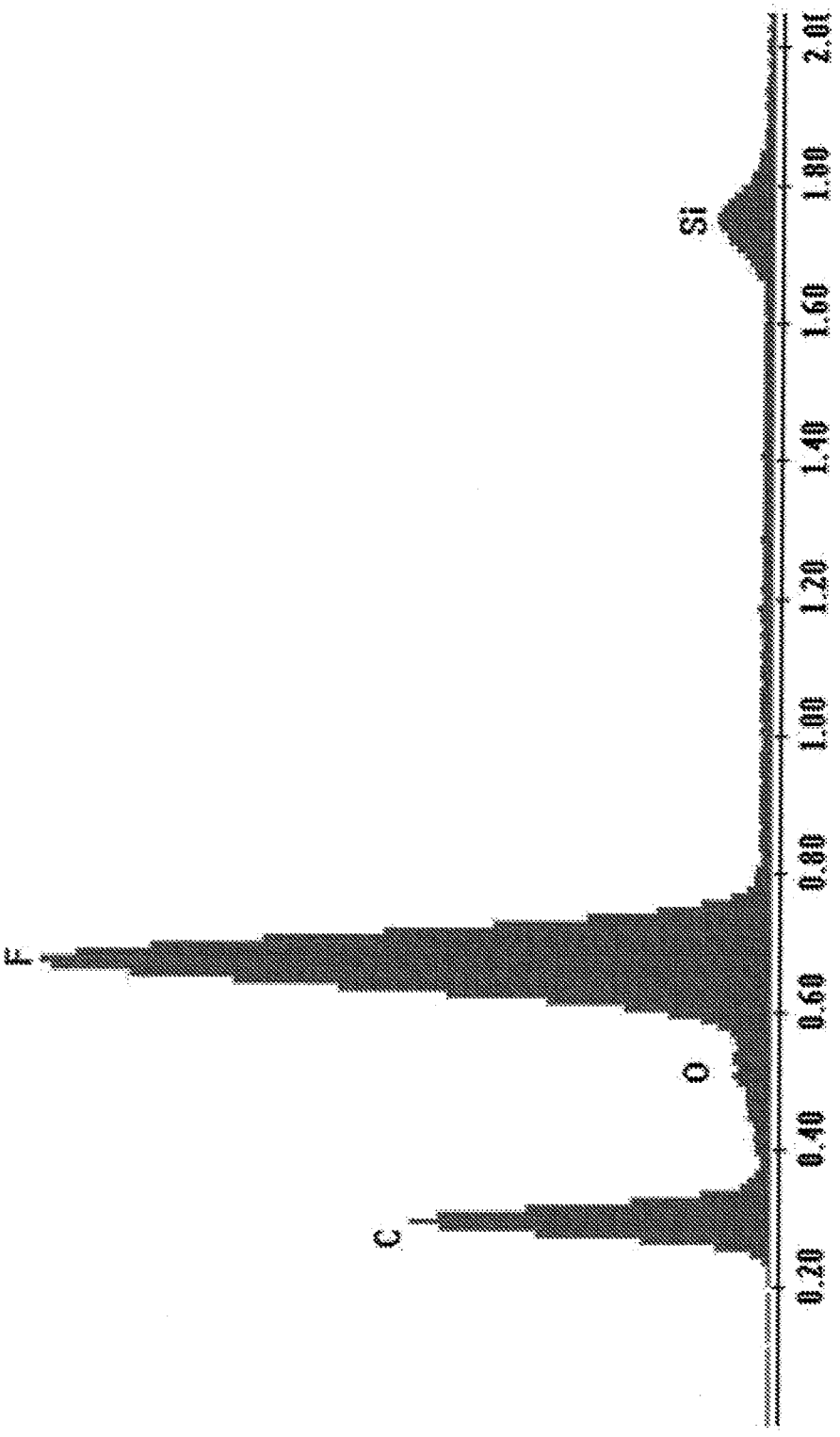


FIG. 33B

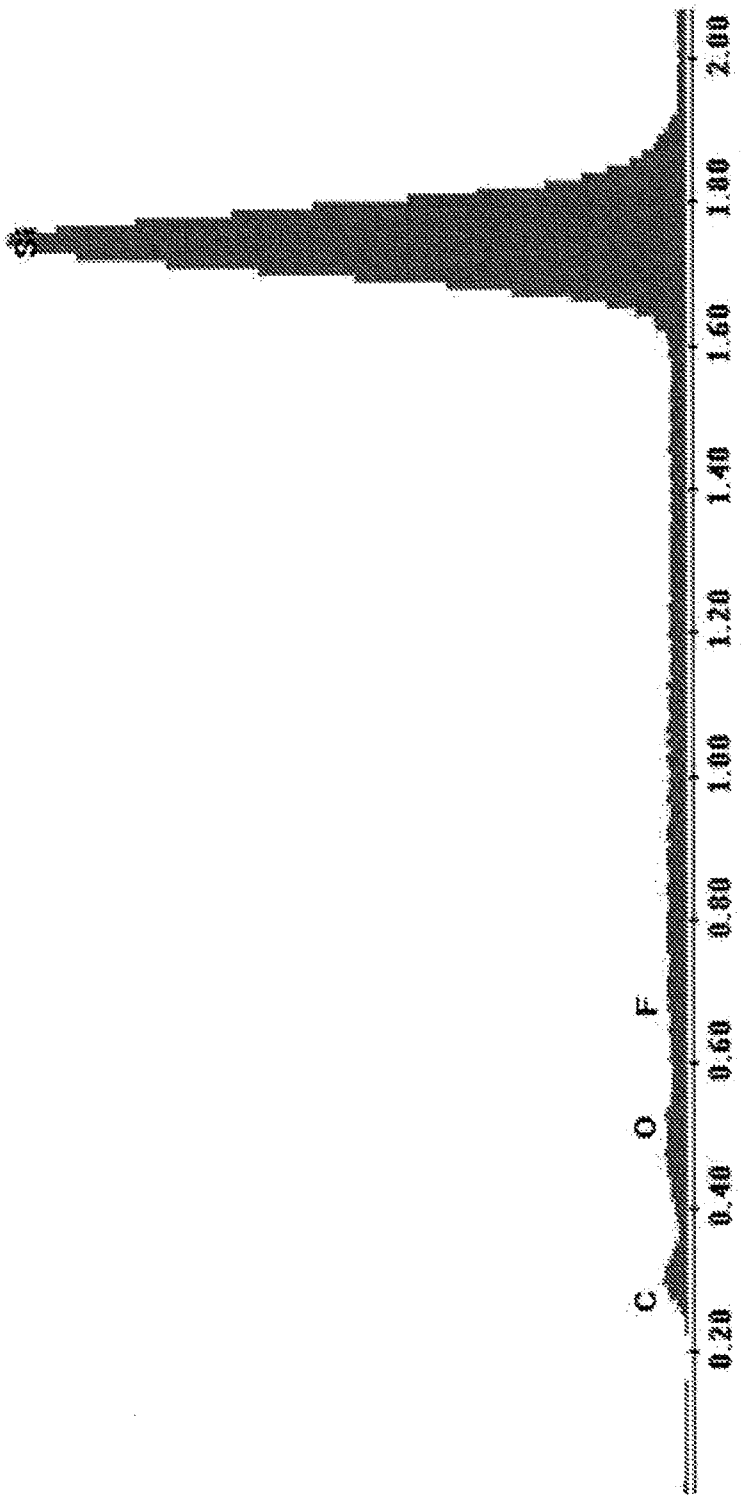


FIG. 33C

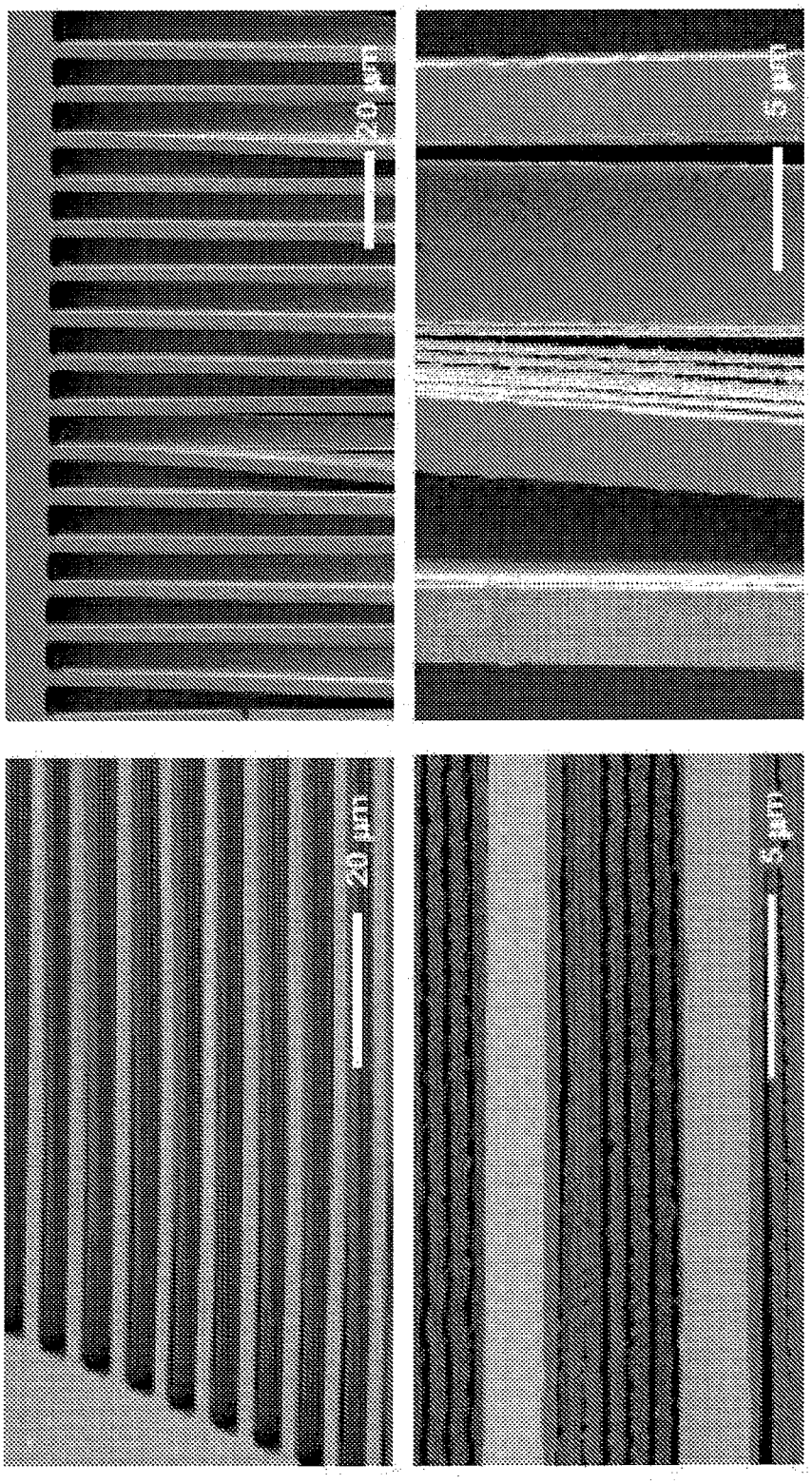


FIG. 34

Anchored release using patterned sacrificial structures:

i. Grow sacrificial layer on substrate



ii. Pattern sacrificial layer



iii. Deposit and pattern functional material layer(s)



iv. Remove sacrificial layer; release overlying functional structures, leaving anchors fixed to substrate, tethering released structures

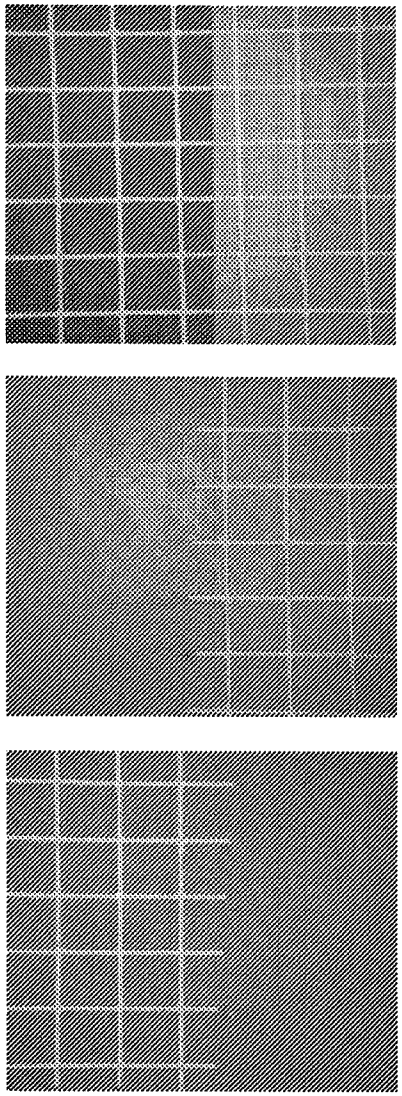


v. Retrieve/print released structures (e.g. using a stamp to break functional structures from anchors)



FIG. 35

Anchored release using patterned sacrificial structures example: Au released from PECVD SiO_x



Functional layer (150 nm Au mesh, 1.5 nm Ti adhesion layer) on a patterned SiO_x (300 nm) sacrificial layer (blue).

Retrieval of mesh overlying sacrificial layer using PDMS stamp after 15 sec. of HF exposure to substrate to remove sacrificial PECVD SiO_x. Where no sacrificial layer was present (right), the mesh remains anchored to the substrate.

Mesh printed onto PET substrate coated with PDMS (1-2 microns) as an adhesive layer

FIG. 36

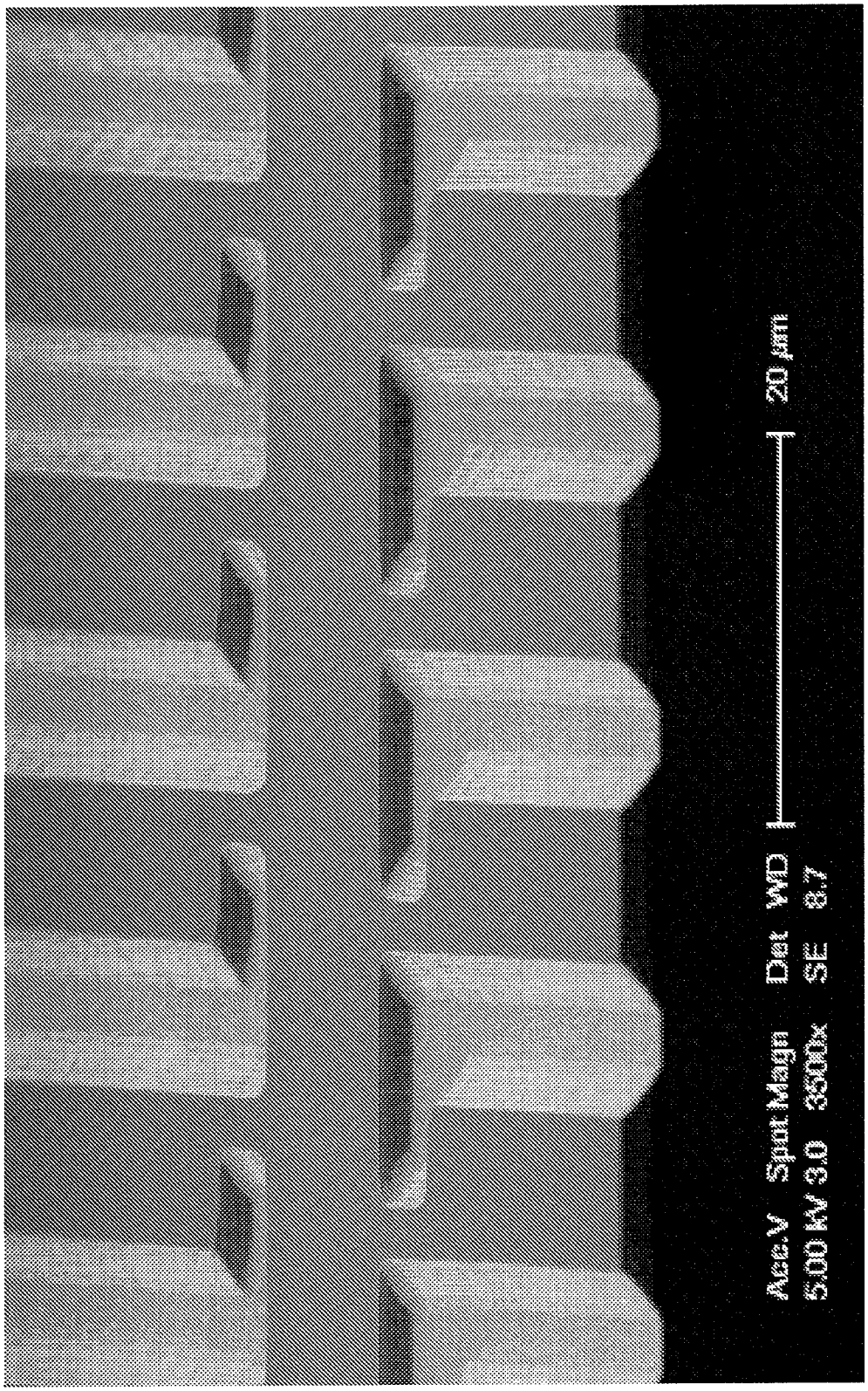


FIG. 37A

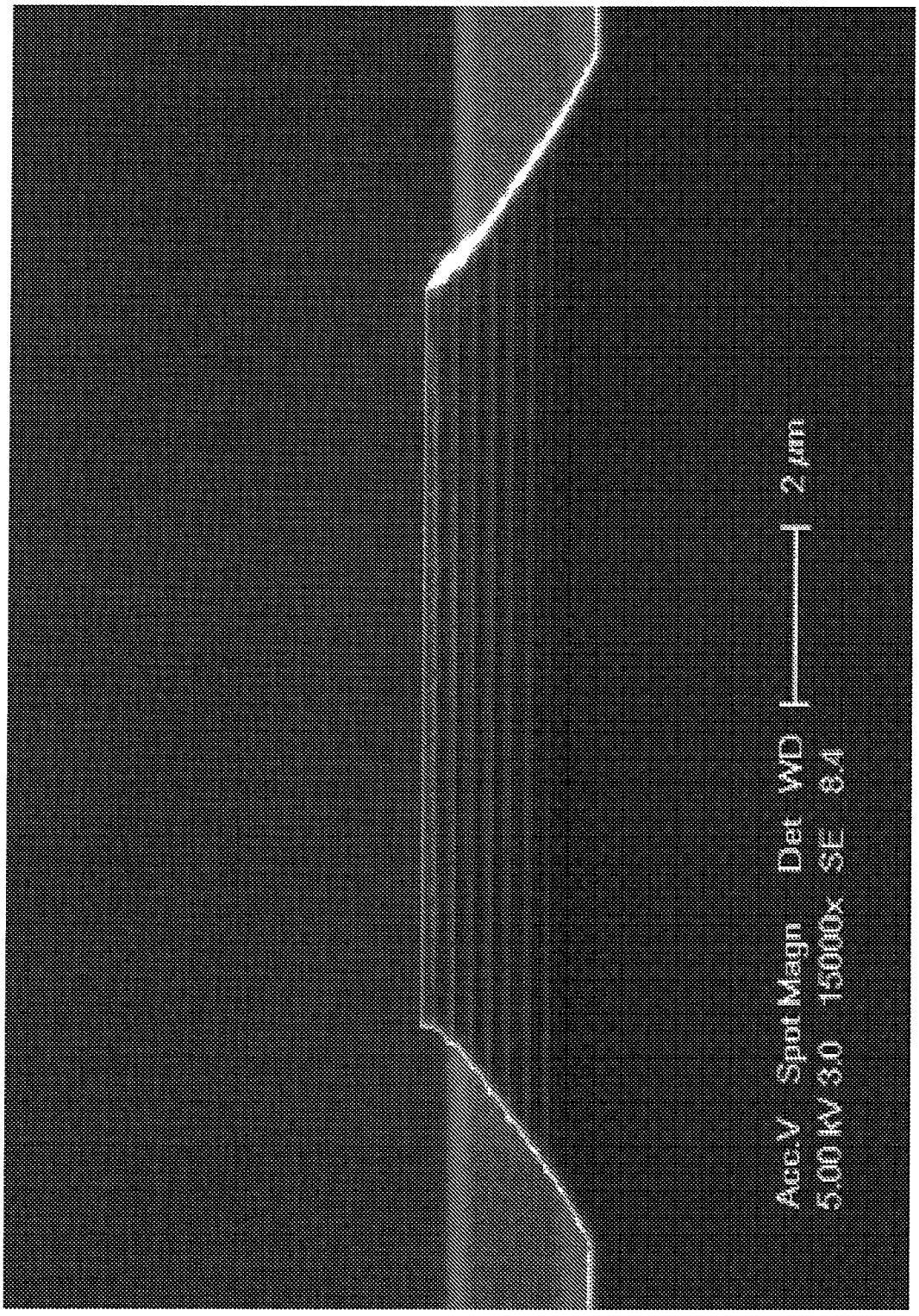


FIG. 37B

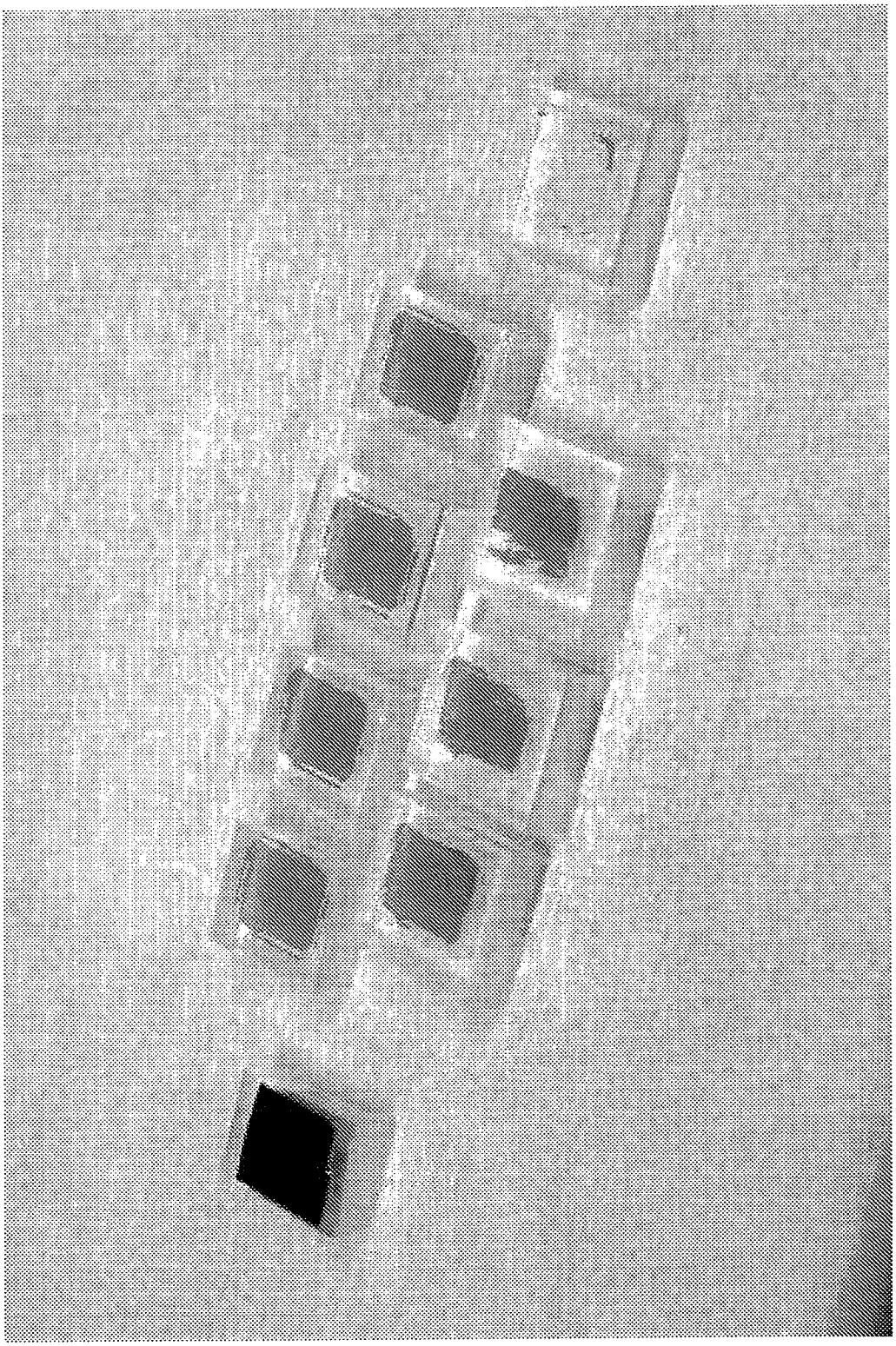


FIG. 38

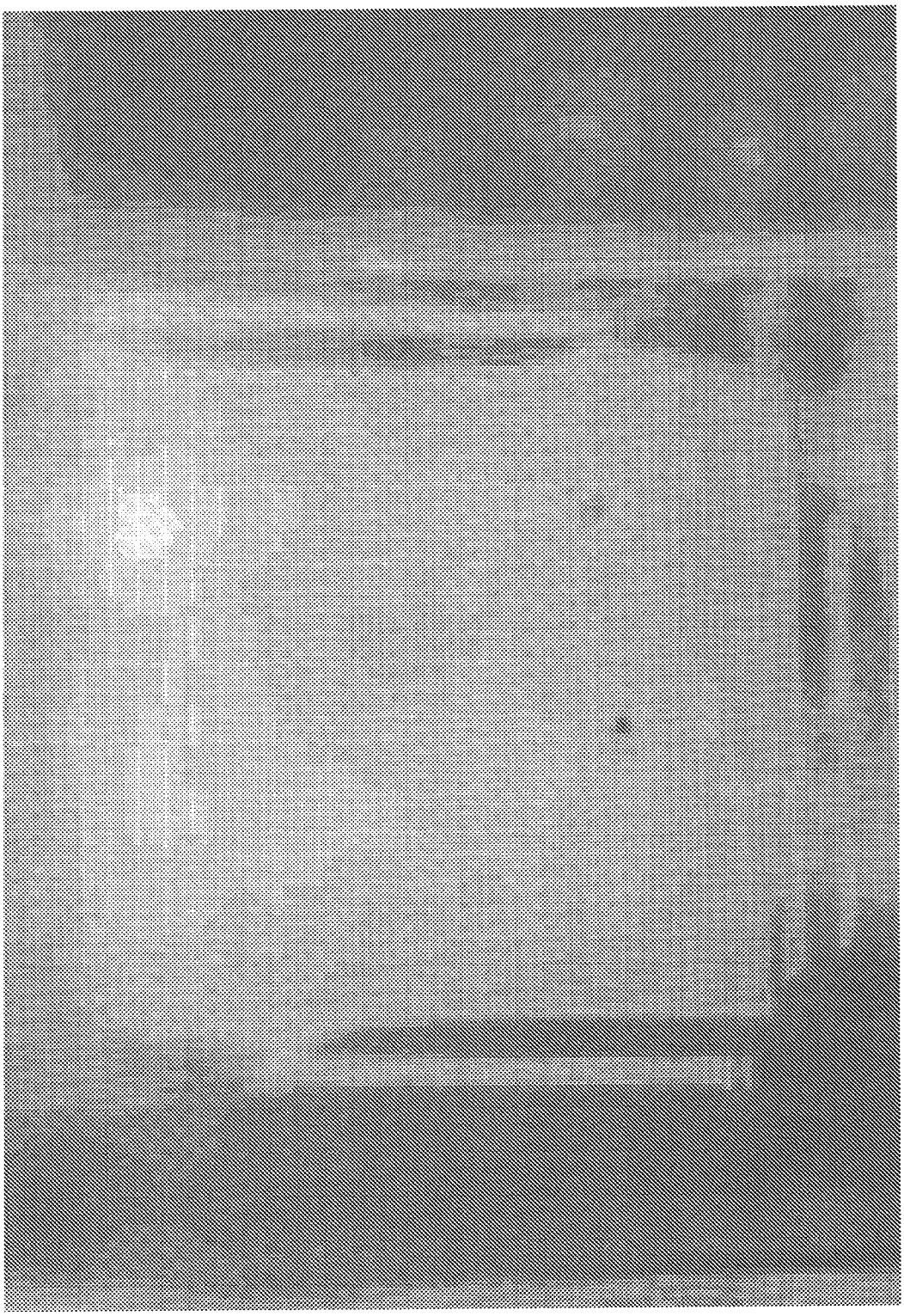


FIG. 39A

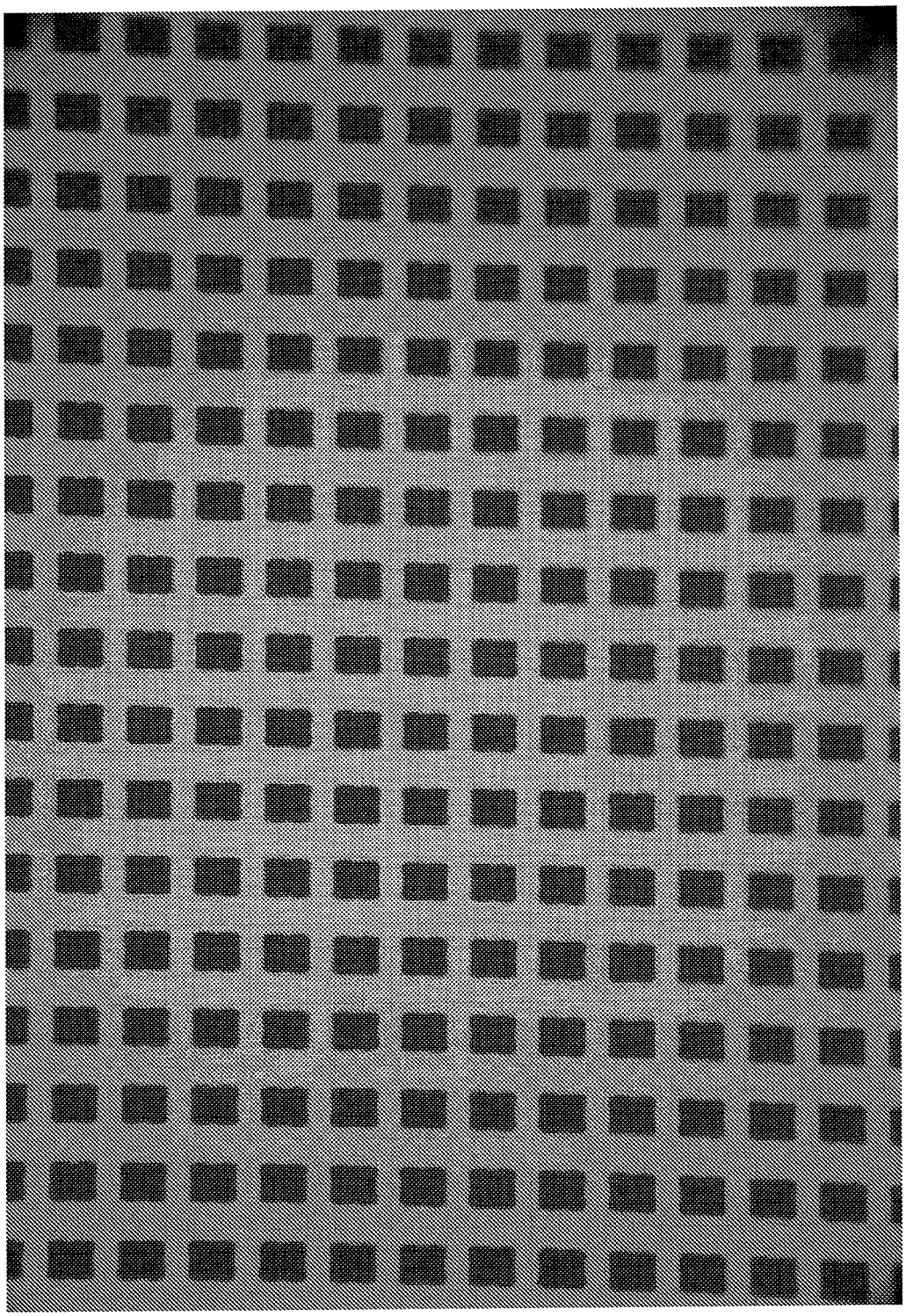


FIG. 39B