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(54) ELECTRONIC ALARM TIMEPIECE

(71) We, KABUSHIKI KAISHA DAINI SEIKOSHA, a Japanese Company of 6-31-1 Kameido, Koto-ku Tokyo, Japan, do hereby declare the invention for which we pray that a patent may be granted to us and the method by which it is to be performed to be particularly described in and by the following statement:—

This invention relates to electronic alarm timepieces, e.g. watches.

Conventional electronic alarm watches produce an alarm when the actual time of day indication coincides with each of a number of set alarm times. Such watches are convenient to use when an alarm is required at the same specified time each day, but when an alarm is required only once they have the disadvantage that the alarm time must be cleared by means of a manually operable switch.

According to the present invention there is provided an electronic alarm timepiece comprising: timekeeping means for producing an actual time of day indication; first alarm means for memorising a first alarm time; second alarm means means for memorising the presence of an alarm time set in each of the first and second alarm means; for memorising a second alarm time: coincidence means for producing a coincidence signal when each alarm time coincides with the actual time of day indication; and an alarm device arranged to be energised in response to the coincidence signal, the first alarm means being such that the alarm device is energised on a once only basis when the first alarm time and the actual time of day indication coincide whereupon the first alarm time is cleared from the first alarm means and the second alarm means being such that the alarm device is energised each time the second alarm time and the actual time of day indication coincide.

The timepiece may include reset means for each alarm means, the reset means being connected to switch means to permit resetting thereof.

The timepiece may include gate means for sequentially passing the contents of the alarm means to the coincidence means for comparison therein with the actual time of day

indication. Preferably the gate means comprises a logic switch circuit connected to be controlled by a sampling signal.

The timepiece in the preferred embodiment, includes an AND gate connected to receive the coincidence signal and the sampling signal and to reset the first alarm means when the alarm time memorised therein coincide with the actual time of day indication.

The invention is illustrated, merely by way of example, in the accompanying drawings in which:—

Figure 1 is a block diagram of an embodiment of an electronic alarm timepiece according to the present invention; and

Figure 2 illustrates wave forms for various signals occurring in the timepiece of Figure 1.

Referring to the drawings, there is illustrated an embodiment of an electronic alarm timepiece, e.g. a watch, according to the present invention. The timepiece has a timekeeping circuit (not shown) a seconds counter 6, an hours and minutes counter 1, a repeat alarm memory 2, a repeat alarm setting memory 20, a single alarm memory 3, a single alarm setting memory 21, a detecting circuit 12, a switch circuit 4, a coincidence circuit 5, and an alarm driver 23.

The above timepiece operates as follows. An oscillating output signal produced by a quartz oscillator (not shown) forming part of the timekeeping circuit, is frequency divided by a frequency divider (not shown) to produce a standard time signal *a* which has a frequency of 1 Hz., and which is fed to the counter 6. The output signal from the counter 6 is a pulse signal *b* having a frequency of 1/60 Hz. The pulse signal *b* is shaped into a single pulse signal *c* having a 500 millisecond pulse width by a latch circuit 11. The pulse signal *c* is fed to the counter 1. The memory 2 and the memory 3 may consist of counters similar to the counter 1, so that any desired alarm time can be set therein by means of clock signals applied to terminals IN-1 and IN-2. The clock signals applied to the terminals IN-1 and IN-2 are also fed to set terminals of the memory 20 and the memory 21 respectively.

Therefore, the memories 20, 21 memorise the presence of an alarm time set in the memories 2, 3 respectively.

A signal *e* is a sampling signal having a frequency of 2Hz and is produced by the frequency divider. The signal *e* alternately passes the contents of the memories 2, 3 of the switch circuit 4. The switch circuit 4 consists of NAND circuits or transmission gates and produces output signals which are fed to the coincidence circuit 5 together with the output of the counter 1.

The coincidence circuit 5 consists of exclusive OR circuits NOR circuits and a NAND circuit. The output of the coincidence circuit 5 is at a relatively low level only when coincidence between the contents of the counter 1 and the contents of either the memory 2 or the memory 3 occurs and at other times is at a relatively high level.

For example, if an alarm time set in the memory 3 coincides with the contents of the counter 1 at time *T* the output of the coincidence circuit 5 changes from relatively high level to relatively low level and produces a pulse coincidence signal *f*. The signal *c* is inverted by an inverter 10 whose output is a signal *d*. The signals *d* and *f* are fed to a NOR circuit 11 whose output is a pulse signal *g*. The pulse signal *g* is transmitted to the alarm driver 23 and causes the latter to produce an alarm. The pulse signal *g* is also fed to one input of the detecting circuit 12 for detecting when the coincidence signal *f* is produced by the coincidence circuit 5. The other input of the detecting circuit 12, which is an AND circuit is the sampling pulse signal *e* inverted by an inverter 40. The detecting circuit 12 produces a single pulse *h* only when coincidence between the contents of the counter 1 and the memory 3 occurs. On the other hand, when coincidence between the contents of the memory 2 and the counter 1 occurs, the detecting circuit 12 does not produce any output. The signal *h* resets the memory 21. Since the output of a NOR circuit 30 is connected to a reset terminal of the memory 3, the contents of the memory 3 are cleared to 0 hours, 00 minutes.

On the other hand, the output of a NOR circuit 31 is maintained at a relatively low level being inverted from a relatively high level, therefore the output of a reset-detecting circuit 13 forming part of the switch circuit 4, is always at a relatively high level *K* when the contents of the counter 1 and the contents of the memory 3 coincide. The output of the circuit 13 is always at a relatively low level being inverted by a NAND circuit 14, so that the signal *f* from the coincidence circuit 5 comes to a relatively high level and thereafter does not cause an alarm to be produced. If the counter 1 comes to 0 hours 00 minutes again, no alarm is produced because the

signal *g* is not produced by the NOR circuit 11. However, to set a new desired alarm time into memory 3, a clock signal is applied to the input terminal IN-2 of the memory 3. The memory 21 maintains a condition such that an alarm is produced when the new alarm time is reached. To clear the memory 2, a single pulse signal is applied to a reset terminal R-1 of the memory 20 by means of a manually operable switch (not shown). Similarly, the memory 3 can be reset by applying a single pulse to a terminal R-2 by means of a manually operable switch (not shown).

The timepiece described above has the advantage that although there are a number of alarm channels, only one coincidence circuit is used, and so the circuitry is simplified. By using one AND circuit for detecting synchronisation between the sampling signals *e* and the signal *g* it can be determined relatively easily whether the coincidence circuit 5 has detected coincidence between the contents of the counter 1 and the memory 2 or the memory 3.

We direct attention to our Application Nos. 42173/76 (Serial No. 1523948), 42343/76 (Serial No. 1524086), and 44638/76 (Serial No. 1468984).

WHAT WE CLAIM IS:—

1. An electronic alarm timepiece comprising: timekeeping means for producing an actual time of day indication; first alarm means for memorising a first alarm time; second alarm means for memorising a second alarm time; means for memorising the presence of an alarm time set in each of the first and second alarm means; coincidence means for producing a coincidence signal when each alarm time coincides with the actual time of day indication; and an alarm device arranged to be energised in response to the coincidence signal, the first alarm means being such that the alarm device is energised on a once only basis when the first alarm time and the actual time of day indication coincide whereupon the first alarm time is cleared from the first alarm means and the second alarm means being such that the alarm device is energised each time the second alarm time and the actual time of day indication coincide.

2. A timepiece as claimed in claim 1 including reset means for each alarm means, the reset means being connected to switch means to permit resetting thereof.

3. A timepiece as claimed in claim 1 or 2 including gate means for sequentially passing the contents of the alarm means to the coincidence means for comparison therein with the actual time of day indication.

4. A timepiece as claimed in claim 3 in which the gate means comprises a logic switch circuit connected to be controlled by a sampling signal.

Therefore, the memories 20, 21 memorise the presence of an alarm time set in the memories 2, 3 respectively.

A signal *e* is a sampling signal having a frequency of 2Hz and is produced by the frequency divider. The signal *e* alternately passes the contents of the memories 2, 3 at the switch circuit 4. The switch circuit 4 consists of NAND circuits or transmission gates and produces output signals which are fed to the coincidence circuit 5 together with the output of the counter 1.

The coincidence circuit 5 consists of exclusive OR circuits NOR circuits and a NAND circuit. The output of the coincidence circuit 5 is at a relatively low level only when coincidence between the contents of the counter 1 and the contents of either the memory 2 or the memory 3 occurs and at other times is at a relatively high level.

For example, if an alarm time set in the memory 3 coincides with the contents of the counter 1 at time *T* the output of the coincidence circuit 5 changes from relatively high level to relatively low level and produces a pulse coincidence signal *f*. The signal *c* is inverted by an inverter 10 whose output is a signal *d*. The signals *d* and *f* are fed to a NOR circuit 11 whose output is a pulse signal *g*. The pulse signal *g* is transmitted to the alarm driver 23 and causes the latter to produce an alarm. The pulse signal *g* is also fed to one input of the detecting circuit 12 for detecting when the coincidence signal *f* is produced by the coincidence circuit 5. The other input of the detecting circuit 12, which is an AND circuit is the sampling pulse signal *e* inverted by an inverter 40. The detecting circuit 12 produces a single pulse *h* only when coincidence between the contents of the counter 1 and the memory 3 occurs. On the other hand, when coincidence between the contents of the memory 2 and the counter 1 occurs, the detecting circuit 12 does not produce any output. The signal *h* resets the memory 21. Since the output of a NOR circuit 30 is connected to a reset terminal of the memory 3, the contents of the memory 3 are cleared to 0 hours, 00 minutes.

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signal *g* is not produced by the NOR circuit 11. However, to set a new desired alarm time into memory 3, a clock signal is applied to the input terminal IN-2 of the memory 3. The memory 21 maintains a condition such that an alarm is produced when the new alarm time is reached. To clear the memory 2, a single pulse signal is applied to a reset terminal R-1 of the memory 20 by means of a manually operable switch (not shown). Similarly, the memory 3 can be reset by applying a single pulse to a terminal R-2 by means of a manually operable switch (not shown).

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2. A timepiece as claimed in claim 1 including reset means for each alarm means, the reset means being connected to switch means to permit resetting thereof.

3. A timepiece as claimed in claim 1 or 2 including gate means for sequentially passing the contents of the alarm means to the coincidence means for comparison therein with the actual time of day indication.

4. A timepiece as claimed in claim 3 in which the gate means comprises a logic switch circuit connected to be controlled by a sampling signal.



5. A timepiece as claimed in claim 4 including an AND gate connected to receive the coincidence signal and the sampling signal and to reset the first alarm means when the alarm time memorised therein coincides with the actual time of day indication.
- 5 6. An electronic alarm timepiece as claimed in claim 1 and substantially as herein

described with reference to and as shown in the accompanying drawings.

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J. MILLER & CO.,
Chartered Patent Agents,
Agents for the Applicants,
Lincoln House,
296/302 High Holborn,
London WC1V 7JH.

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