T10_x. Take the buffer 319_1 as an example, the first terminal of the transistor T9_1 receives the second clock signal CK2_1. The transistor T10_1 may be coupled as a diode configuration, and the anode of the diode configured is coupled to the second terminal of the transistor T9_1, and the cathode of the diode configured and the control terminal of the transistor T9_1 jointly receive the first bias voltage G_n, so that the buffer 319_1 can generate the corresponding gate driving signal GL_1 on the second terminal of the transistor T9_1 only according to the first bias voltage G_n. The buffer 319_1 may also maintain the voltage value of the gate driving signal GL_1 according to the gate driving signal GL_1 and the first bias voltage G_n through the transistor T10_1. The elements in the other buffers 319_2 to 319_x are coupled in the same manner, which is not repeated hereinafter.

[0029] In FIG. 3C, the signal output circuit 312 includes multi-stage voltage generators 320_1 to 320_x. The voltage generators 320_1 to 320_x respectively include transistors T9_1 to T9_x, T10_1 to T10_x, T11_1 to T11_x, T12_1 to T12_x, and capacitors C2_1 to C2_x. Take the voltage generator 320_1 as an example, the first terminal of the transistor T9_1 receives the second clock signal CK2_1. The first terminal of the transistor T10_1 is coupled to the second terminal of the transistor T9_1, and the control terminal of the transistor T9_1 and the second terminal of the transistor T10_1 jointly receive the first bias voltage G_n. The first terminals of the transistors T11_1 and T12_1 are jointly coupled to the control terminal of the transistor T10_1, and the second terminals of the transistors T11_1 and T12_1 jointly receive the third voltage V_{SSG}. The control terminals of the transistor T11_1 and the transistor T12_1 respectively receive the first bias voltage G_n and the start signal ST. The capacitor C2_1 is coupled between the first terminal of the transistor T9_1 and the control terminal of the transistor T10_1, so that the voltage generator 320_1 can generate the corresponding gate driving signal GL_1 on the second terminal of the transistor T9_1 according to the first bias voltage G_n. The

driving signal GL_X, the second terminal of the transistor T15 receives the third voltage V_{SSG}, and the control terminal of the transistor T15 receives the post-stage gate driving signal (for example, the post-five stage gate driving signal GL_{X+5} in this embodiment, but the disclosure is not limited thereto). In other words, the auxiliary circuit 523 may be a pull-down circuit, and may pull down the gate driving signal GL_X according to the post-stage gate driving signal GL_{X+5} based on the third voltage V_{SSG}.

[0037] In FIG. 5D, the auxiliary circuit 524 is configured to provide a voltage stabilizing path when the gate driving signal GL_X discharges the scan line, so as to prevent fluctuation generated due to the influence of crosstalk and thereby increase the speed of pulling down the gate driving signal GL_X to a low potential (the third voltage V_{SSG} in this embodiment, but the disclosure is not limited thereto). In this embodiment, the auxiliary circuit 524 is composed of multi-stage voltage controllers 524_1 and 524_2. The voltage controllers 524_1 and 524_2 respectively include transistors T16 to T22 and T23 to T29. Take the voltage controller 524_1 as an example, the first terminal of the transistor T16 receives the gate driving signal GL_X. The second terminal of the transistor T17 is coupled to the control terminal of the transistor T16. The first terminals of the transistors T18 and T20 are jointly coupled to the second terminal of the transistor T17. The first terminals of the transistors T19 and T22 are jointly coupled to the control terminal of the transistor T17. The transistor T21 may be coupled as a diode configuration, and the anode of the diode configured and the first terminal of the transistor T17 jointly receive the third clock signal CK3_1, and the cathode of the diode configured is coupled to the control terminal of the transistor T17. The control terminals of the transistors T18 and T19 jointly receive the gate driving signal GL_X. The control terminals of the transistors T20 and T22 jointly receive the fore-stage gate driving signal (for example, the fore-two stage gate driving signal GL_{X-2} in this embodiment, but the disclosure is not limited thereto). The second

terminals of the transistors T16, T18 to T20, and T22 jointly receive the third voltage V_{SSG}, so that the voltage controller 524_1 can compensate for the gate driving signal GL_X according to the fore-stage gate driving signal GL_{X-2} and the gate driving signal GL_X based on the third voltage V_{SSG}. The elements in the voltage controller 542_2 are coupled in the same manner, which is not repeated hereinafter.

[0038] Please note that, according to the design requirements, the disclosure may use combinations of different auxiliary circuits 521 to 524 in the above embodiments of FIG. 5A to FIG. 5D to form the first auxiliary circuit 420 and/or the second auxiliary circuit 430 shown in FIG. 4. The auxiliary circuits 521 and 522 can provide the auxiliary function of precharge on the scan line according to the fore-stage gate driving signal GL_{X-5}, so that the speed of pulling up the gate driving signal GL_X to a high potential can be increased. The auxiliary circuit 523 can provide the auxiliary function of rapid discharge on the scan line according to the post-stage gate driving signal GL_{X+5}, so that the speed of pulling down the gate driving signal GL_X to a low potential can be increased. The auxiliary circuit 524 can stabilize the gate driving signal GL_X according to the fore-stage gate driving signal GL_{X-2}, the gate driving signal GL_X, and the third clock signal CK3_1, so that the speed of pulling down the gate driving signal GL_X to a low potential can be increased. In this way, the first auxiliary circuit 420 and/or the second auxiliary circuit 430 can compensate for the gate driving signal GL_X according to the design requirements, thereby improving the charging and discharging capabilities of the gate driving circuit.

[0039] Please refer to FIG. 1 and FIG. 6. FIG. 6 is a timing diagram of clock signals according to an embodiment of the disclosure. The gate driving circuit 110 can sequentially drive the bias generators 111_1 and 111_2 and the corresponding signal output circuits 112_1 to 112_P by timing control to control the charging and discharging times of the gate driving signals GL_1 to GL_P for the scan lines. For example, the first clock signals CK1_1 to CK1_8 in FIG.

WHAT IS CLAIMED IS:

1. A display panel, comprising:

a plurality of scan lines arranged on the display panel along a first direction, and respectively providing a plurality of gate driving signals; and

a gate driving circuit arranged on a first side of the display panel along a second direction that intersects the first direction, the gate driving circuit comprising a plurality of bias generators and a plurality of signal output circuits, wherein the signal output circuits are divided into a plurality of groups, the bias generators respectively correspond to the groups, the bias generators generate a plurality of first bias voltages, the groups generate the gate driving signals respectively according to the first bias voltages, and each of the bias generators comprises:

a first pull-up circuit pulling up a first control voltage according to a fore-stage bias voltage based on a first voltage;

a second pull-up circuit pulling up a second control voltage according to a first clock signal;

a first pull-down circuit pulling down the first control voltage according to a start signal, the second control voltage and/or a post-stage bias voltage;

a second pull-down circuit pulling down the second control voltage according to the start signal and/or the first control voltage; and

an output stage circuit generating each of the first bias voltages corresponding to the groups according to the first control voltage and the second control voltage.

2. The display panel according to claim 1, wherein

the first pull-up circuit is a pull-up transistor, wherein a first terminal of the pull-up transistor receives the first voltage, and a control terminal of the pull-up transistor receives the fore-stage bias voltage for pulling up the first control voltage on a second terminal of the pull-up transistor;

the second pull-up circuit is a pull-up capacitor, wherein a first terminal of the pull-up capacitor receives the first clock signal for pulling up the second control voltage on a second terminal of the pull-up capacitor;

the first pull-down circuit comprises a plurality of first pull-down transistors, wherein first terminals of the first pull-down transistors receive the first control voltage, second terminals of the first pull-down transistors receive a second voltage, and control terminals of the first pull-down transistors respectively receive the start signal, the second control voltage, and the post-stage bias voltage to pull down the first control voltage;

the second pull-down circuit comprises a plurality of second pull-down transistors, wherein first terminals of the second pull-down transistors receive the second control voltage, second terminals of the second pull-down transistors receive the second voltage, and control terminals of the second pull-down transistors respectively receive the start signal and the first control voltage to pull down the second control voltage; and

the output stage circuit is a buffer, wherein the buffer receives the first clock signal and a third voltage to generate each of the first bias voltages corresponding to the groups according to the first control voltage and the second control voltage.

3. The display panel according to claim 1, wherein each of the bias generators further provides the second control voltage as a second bias voltage, wherein each group of the signal output circuits in a same group comprises:

a plurality of buffers respectively receiving a plurality of second clock signals, wherein the buffers respectively generate corresponding gate driving signals according to the first bias voltage and the second bias voltage.

4. The display panel according to claim 1, wherein each group of the signal output circuits in a same group comprises:

a plurality of buffers respectively receiving a plurality of second clock signals, wherein the buffers respectively generate corresponding gate driving signals only according to the

first bias voltage, and maintain voltage values of the gate driving signals according to the gate driving signals and the first bias voltage.

5. The display panel according to claim 1, wherein each group of the signal output circuits in a same group comprises:

multi-stage voltage generators respectively generating corresponding gate driving signals, wherein each of the voltage generators comprises:

a first transistor, wherein a first terminal of the first transistor receives a second clock signal, and a control terminal of the first transistor receives the first bias voltage;

a second transistor, wherein a first terminal of the second transistor is coupled to a second terminal of the first transistor, and a second terminal of the second transistor receives the first bias voltage;

a third transistor and a fourth transistor, wherein first terminals of the third transistor and the fourth transistor are both coupled to a control terminal of the second transistor, second terminals of the third transistor and the fourth transistor both receive a second voltage, a control terminal of the third transistor receives the first bias voltage, and a control terminal of the fourth transistor receives the start signal; and

a capacitor coupled between the first terminal of the first transistor and the control terminal of the second transistor.

6. The display panel according to claim 1, further comprising:

a first auxiliary circuit arranged on a second side of the display panel along the first direction, wherein the first auxiliary circuit is coupled to the scan lines for compensating for the gates driving signals generated by the signal output circuits.

7. The display panel according to claim 6, wherein the first auxiliary circuit comprises:

a plurality of first transistors pulling up the gate driving signals according to a plurality of fore-stage gate driving signals based on a first voltage or a first clock signal.

8. The display panel according to claim 7, wherein the first auxiliary circuit further

comprises:

a plurality of second transistors respectively coupled as a plurality of diodes, wherein the diodes respectively have a plurality of cathodes respectively coupled to control terminals of the first transistors, and a plurality of anodes of the diodes respectively receive the fore-stage gate driving signals; and

a plurality of capacitors respectively coupled between the control terminals and second terminals of the first transistors.

9. The display panel according to claim 6, wherein the first auxiliary circuit comprises:

a plurality of first transistors pulling down the gate driving signals according to a plurality of post-stage gate driving signals based on a first voltage.

10. The display panel according to claim 6, wherein the first auxiliary circuit comprises:

multi-stage voltage controllers compensating for the gate driving signals according to a fore-stage gate driving signal based on a plurality of first clock signals, wherein each of the voltage controllers comprises:

a first transistor, wherein a first terminal of the first transistor receives each corresponding gate driving signal;

a second transistor, wherein a second terminal of the second transistor is coupled to a control terminal of the first transistor;

a third transistor and a fourth transistor, wherein first terminals of the third transistor and the fourth transistor are both coupled to the second terminal of the second transistor;

a fifth transistor and a sixth transistor, wherein first terminals of the fifth transistor and the sixth transistor are both coupled to a control terminal of the second transistor;

a seventh transistor coupled as a diode configuration, and having a cathode coupled to the control terminal of the second transistor and having an anode, wherein the anode and a first terminal of the second transistor jointly receive each corresponding first clock signal,

wherein control terminals of the third transistor and the fifth transistor both receive corresponding gate driving signals, control terminals of the fourth transistor and the sixth transistor both receive the fore-stage gate driving signal, and second terminals of the first transistor, the third transistor, the fourth transistor, the fifth transistor, and the sixth transistor all receive a first voltage.

11. The display panel according to claim 6, further comprising:

a plurality of second auxiliary circuits arranged on a third side opposite to the second side of the display panel along the first direction, wherein the second auxiliary circuits are coupled to the scan lines for compensating for the gate driving signals generated by the signal output circuits.