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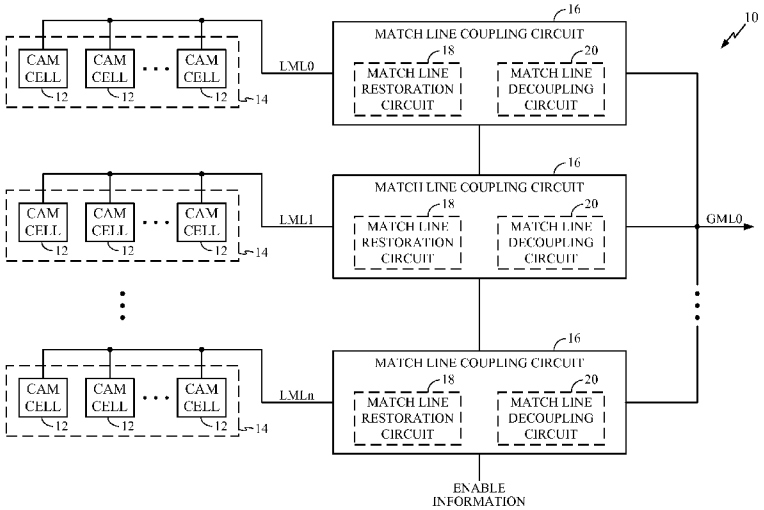
(54) Title: METHOD AND APPARATUS FOR REDUCING POWER CONSUMPTION IN A CONTENT ADDRESSABLE MEMORY



(57) Abstract: Power consumption in a multi-level hierarchical Content Addressable Memory (CAM) circuit is reduced without adversely impacting performance. According to one embodiment of a multi-level hierarchical CAM circuit, the CAM circuit comprises a plurality of lower-level match lines, a plurality of higher-level match lines and match line restoration circuitry. The lower-level match lines are configured to be restored to a pre-evaluation state during a pre-evaluation period. The higher-level match lines are configured to capture an evaluation state of respective groups of one or more of the lower-level match lines during an evaluation period and to be restored to a pre-evaluation state during the pre-evaluation period. The match line restoration circuitry is configured to prevent at least one of the lower-level match lines from being restored to the pre-evaluation state responsive to corresponding enable information, e.g., one or more bits indicating whether match line search results are to be utilized.

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