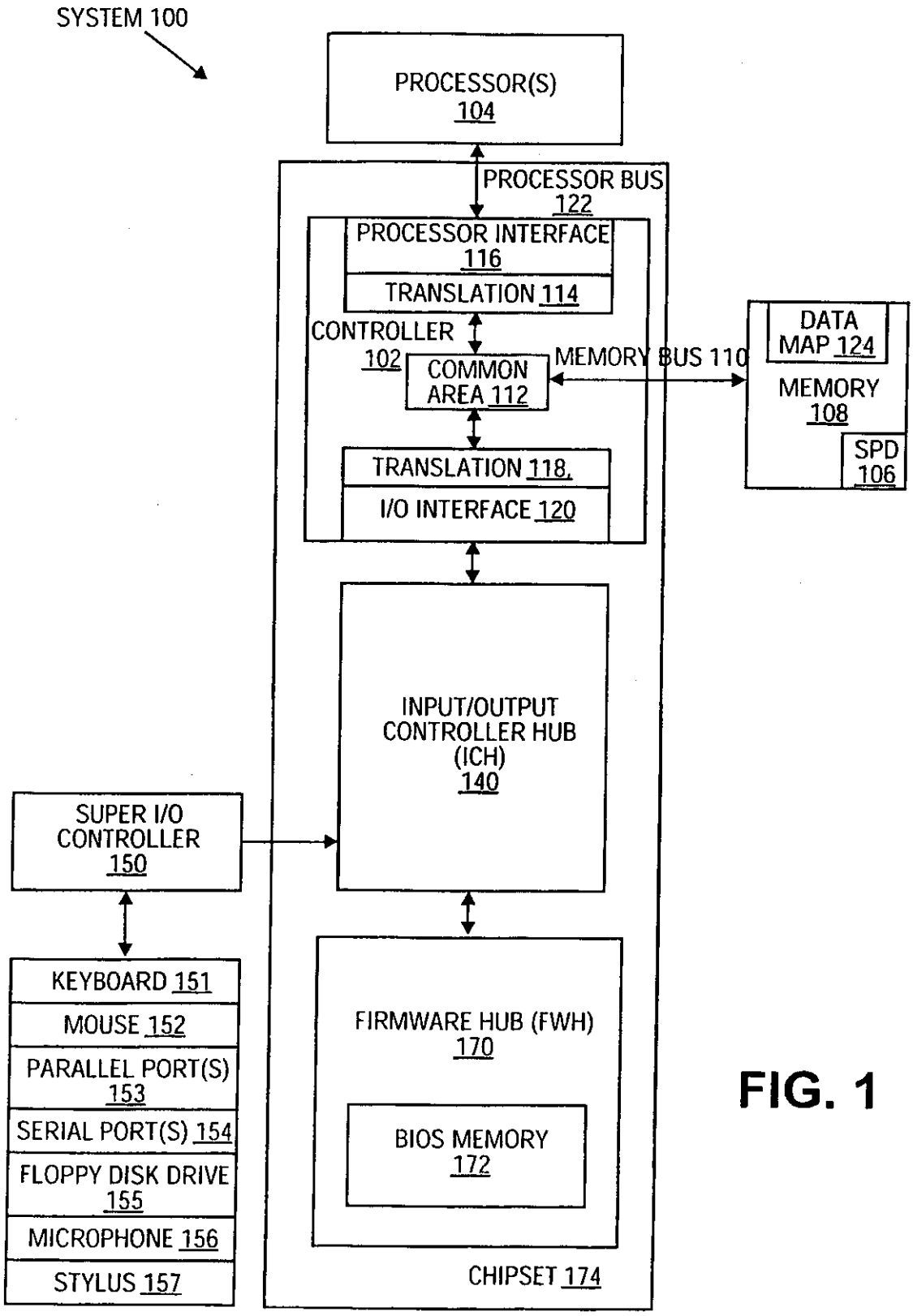

SYSTEM 100
PROCESSOR(S) 104
PROCESSOR BUS 122
PROCESSOR INTERFACE 116
TRANSLATION 114
CONTROLLER 102
COMMON AREA 112
MEMORY BUS 110
DATA MAP 124
MEMORY 108
SPD 106
TRANSLATION 118,
I/O INTERFACE 120
INPUT/OUTPUT CONTROLLER HUB (ICH) 140
SUPER I/O CONTROLLER 150
KEYBOARD 151
MOUSE 152
PARALLEL PORT(S) 153
SERIAL PORT(S) 154
FLOPPY DISK DRIVE 155
MICROPHONE 156
STYLUS 157
FIRMWARE HUB (FWH) 170
BIOS MEMORY 172
CHIPSET 174

FIG. 1

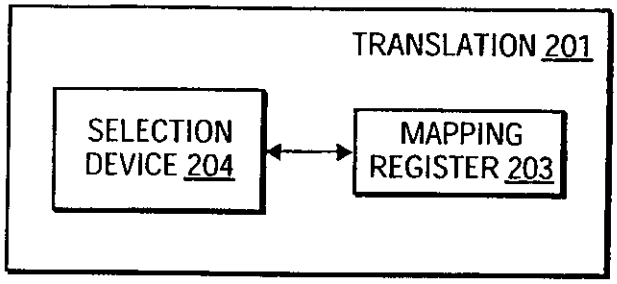

TRANSLATION 201
SELECTION DEVICE 204
MAPPING REGISTER 203

FIG. 2

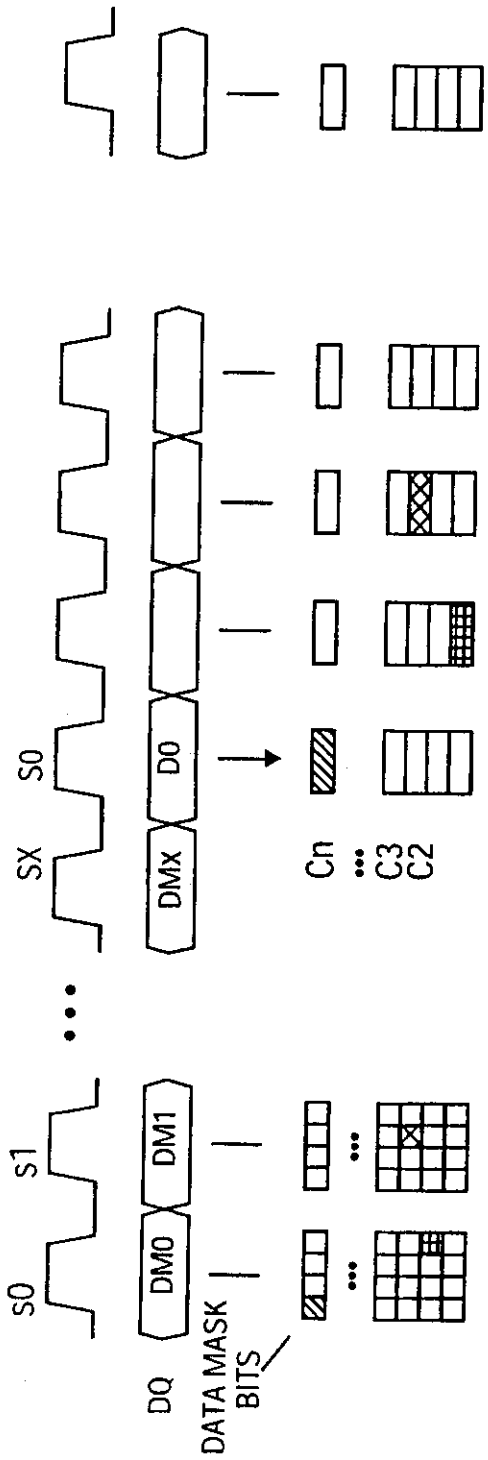


FIG. 3

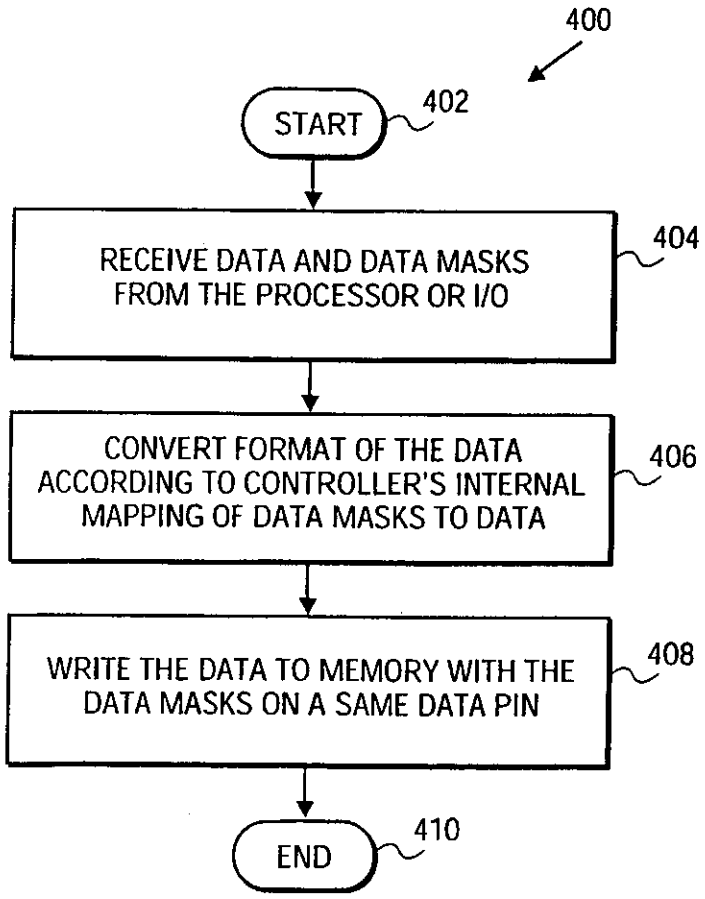

400
START
402
RECEIVE DATA AND DATA MASKS FROM THE PROCESSOR OR I/O
404
CONVERT FORMAT OF THE DATA ACCORDING TO CONTROLLER'S INTERNAL MAPPING OF DATA MASKS TO DATA
406
WRITE THE DATA TO MEMORY WITH THE DATA MASKS ON A SAME DATA PIN
408
END
410

FIG. 4

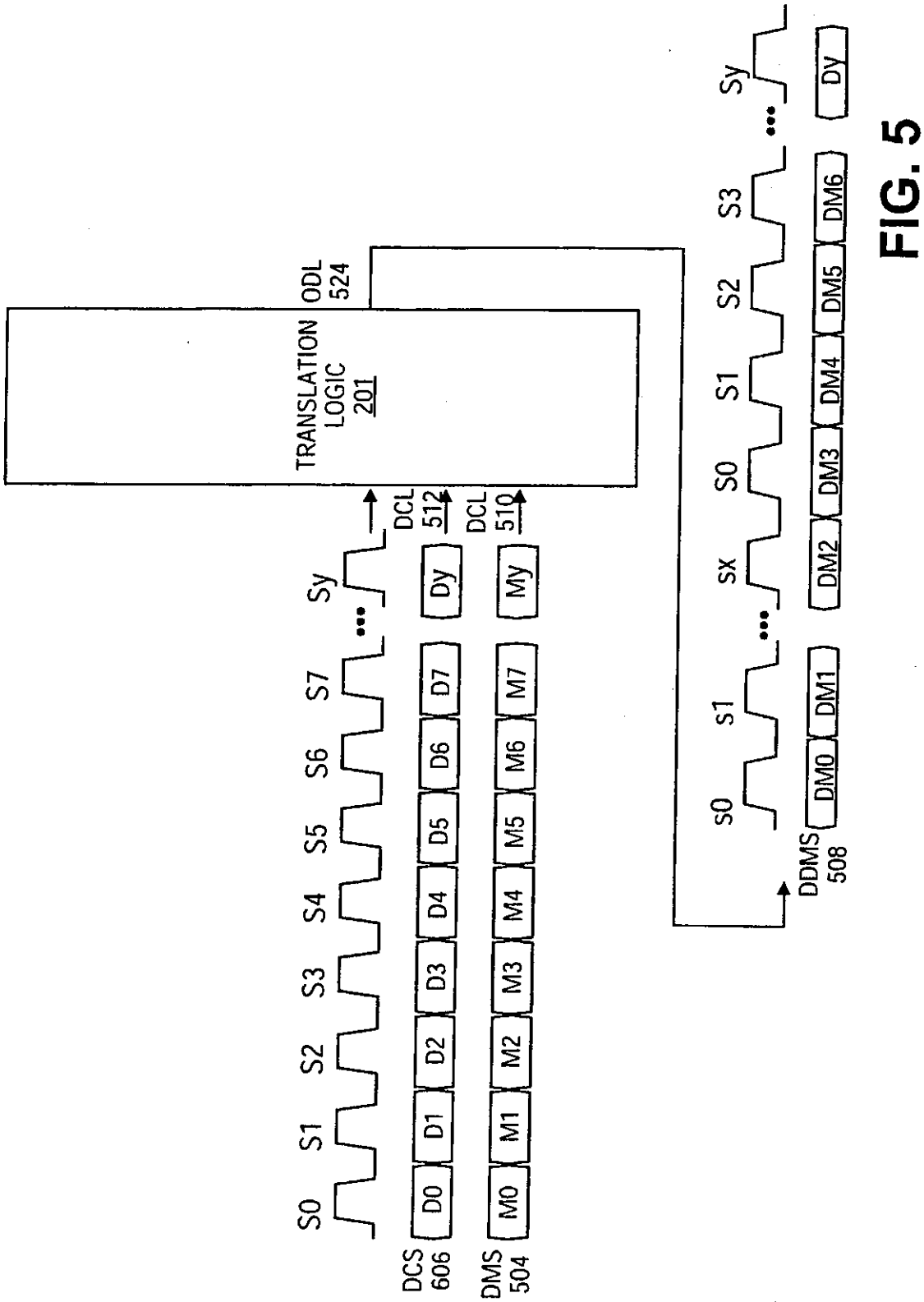

TRANSLATION LOGIC 201
ODL 524
DCL 512
DCL 510
DCS 606
DMS 504
DDMS 508
S0 S1 S2 S3 S4 S5 S6 S7 Sy
D0 D1 D2 D3 D4 D5 D6 D7 Dy
M0 M1 M2 M3 M4 M5 M6 M7 My
s0 s1 sx S0 S1 S2 S3 Sy
DM0 DM1 DM2 DM3 DM4 DM5 DM6 Dy

FIG. 5

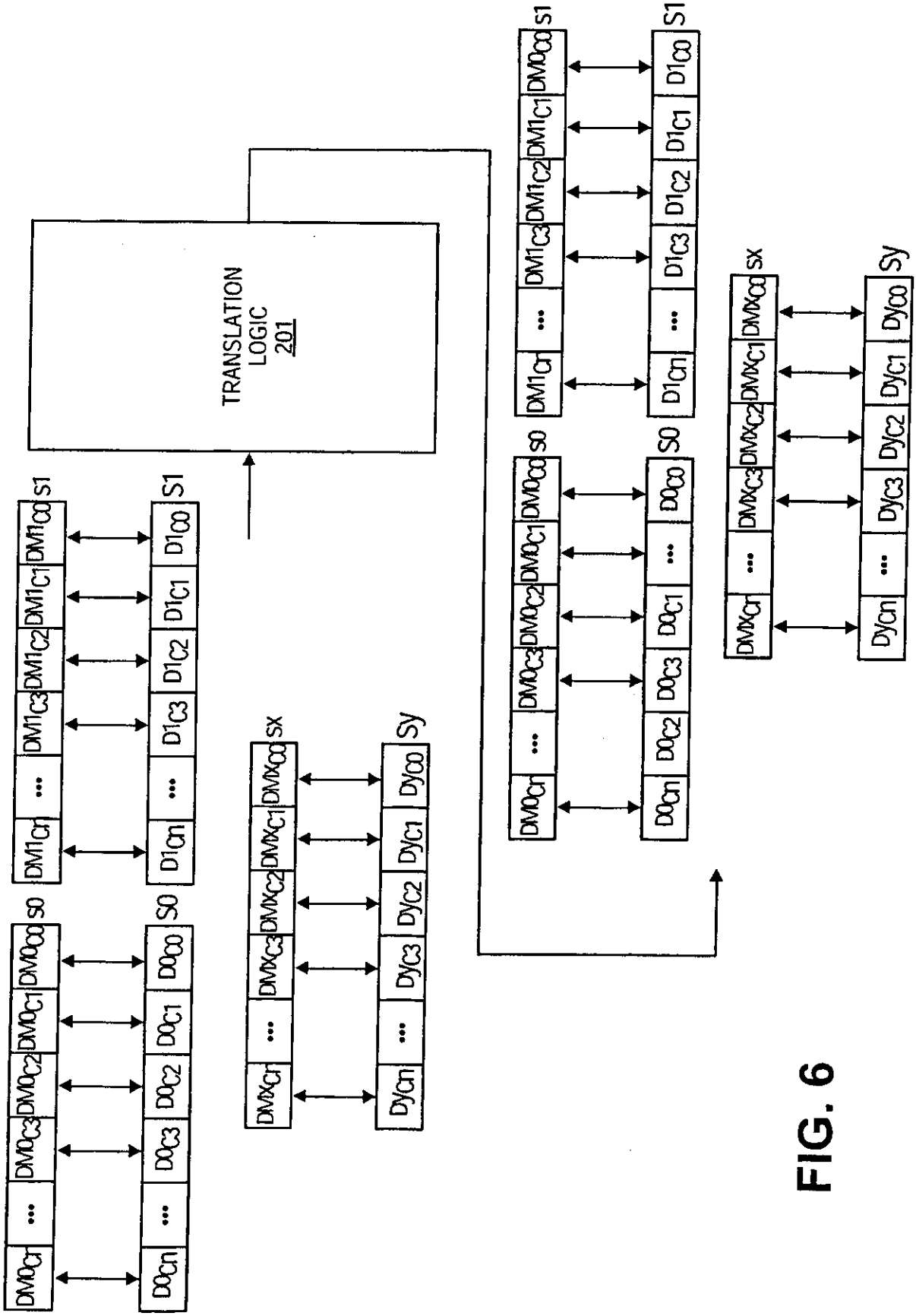

TRANSLATION LOGIC 201
S0
S1
SX
SY
DM0C0
DM0C1
DM0C2
DM0C3
DM0Cn
D0C0
D0C1
D0C2
D0C3
D0Cn
DM1C0
DM1C1
DM1C2
DM1C3
DM1Cn
D1C0
D1C1
D1C2
D1C3
D1Cn
DMXC0
DMXC1
DMXC2
DMXC3
DMXCn
DyC0
DyC1
DyC2
DyC3
DyCn

FIG. 6

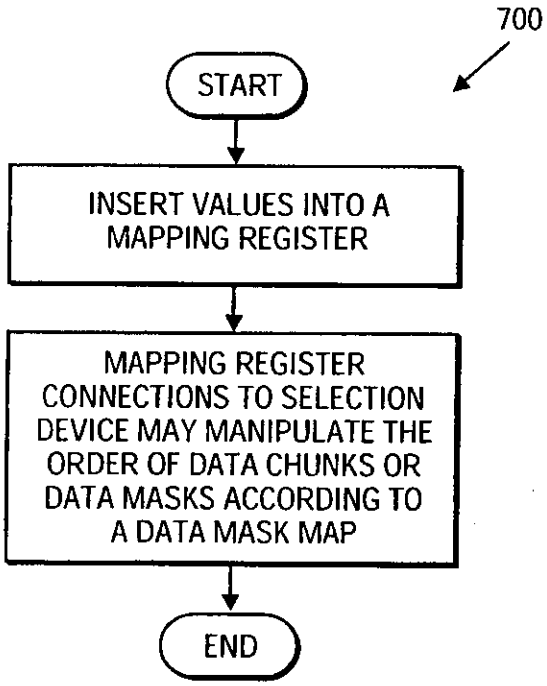

700
START
INSERT VALUES INTO A MAPPING REGISTER
MAPPING REGISTER CONNECTIONS TO SELECTION DEVICE MAY MANIPULATE THE ORDER OF DATA CHUNKS OR DATA MASKS ACCORDING TO A DATA MASK MAP
END

FIG. 7

	column 802	column 804
row 806	Data	Data masks
row 808	DEADBEEF	A dm[3:0]
row 810	FEEDFACE	1 dm[7:4]
row 812	01234567	3 dm[11:8]
row 814	89ABCDEF	2 dm[15:12]
row 816	02468ACE	6 dm[19:16]
row 818	13579BDF	F dm[23:20]
row 820	777777777	0 dm[27:24]
row 822	AAAAAAAA	4 dm[31:28]

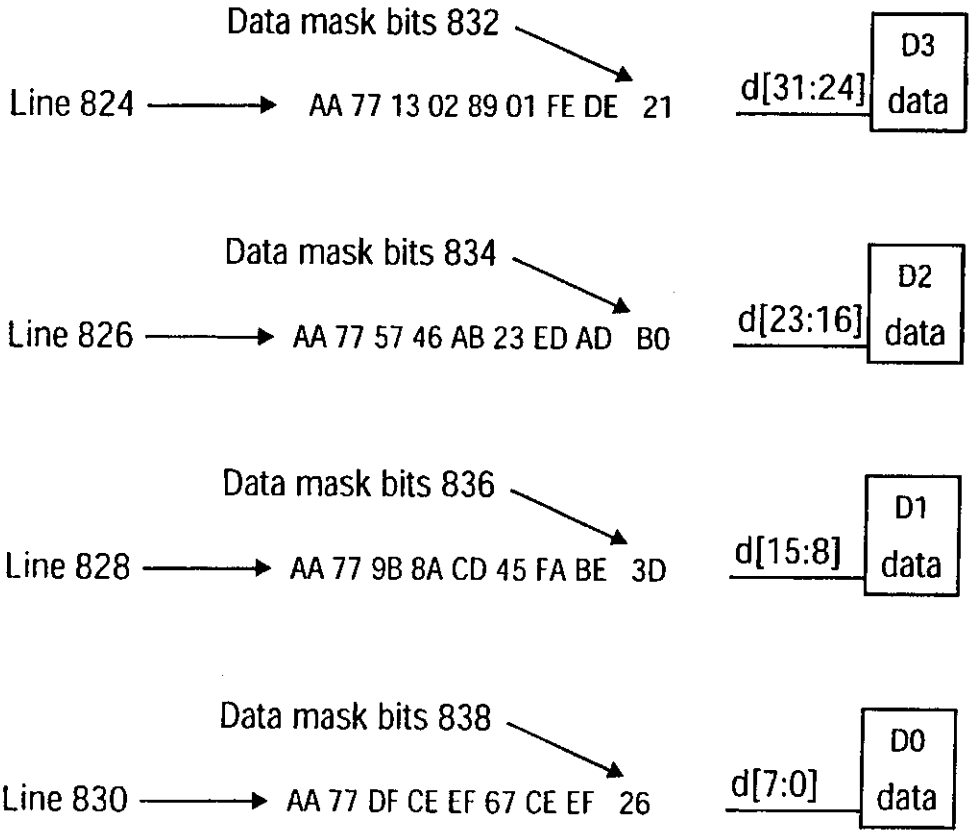


FIG. 8

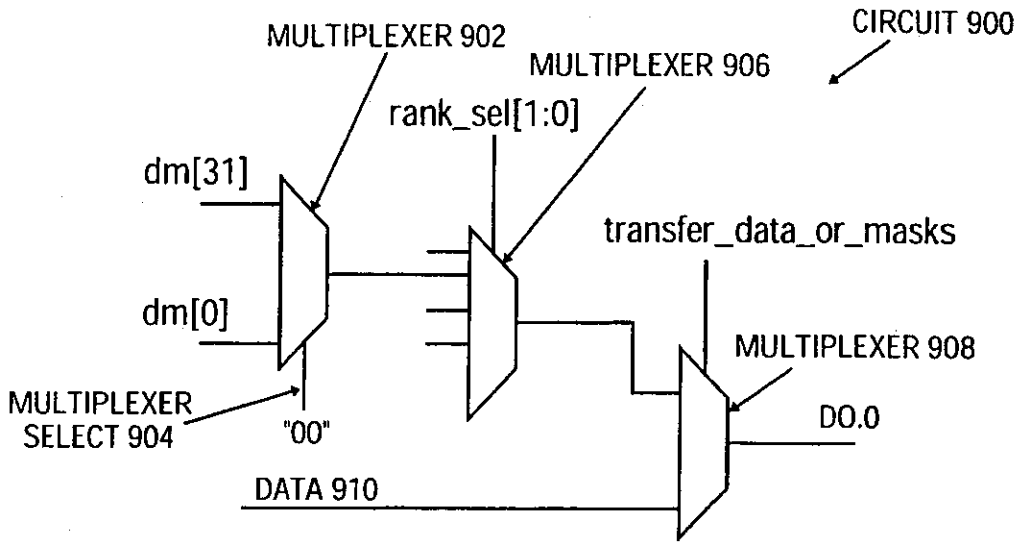

CIRCUIT 900
MULTIPLEXER 902
MULTIPLEXER 906
rank_sel[1:0]
dm[31]
transfer_data_or_masks
dm[0]
MULTIPLEXER 908
MULTIPLEXER
SELECT 904
"00"
DO.0
DATA 910

FIG. 9A

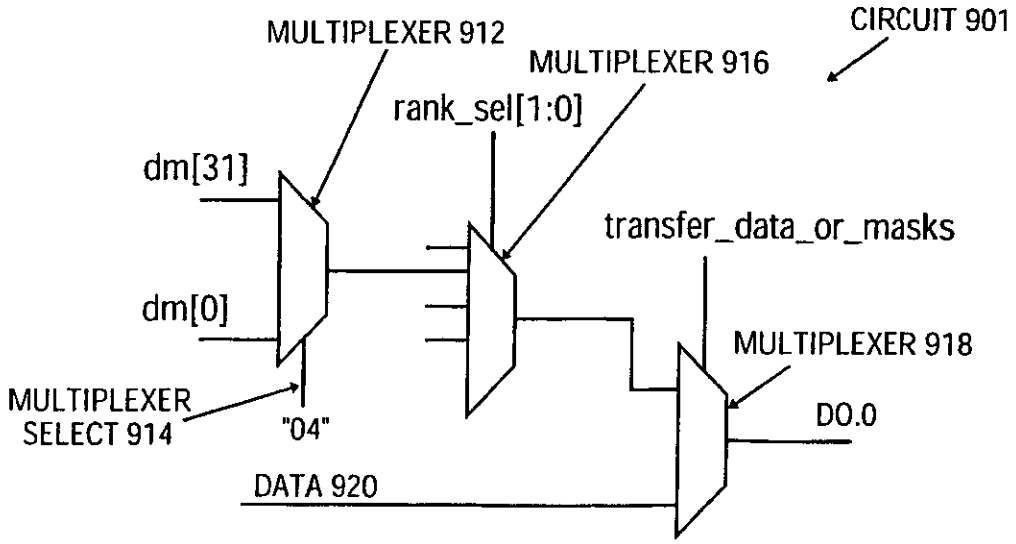

CIRCUIT 901
MULTIPLEXER 912
MULTIPLEXER 916
rank_sel[1:0]
dm[31]
transfer_data_or_masks
dm[0]
MULTIPLEXER 918
MULTIPLEXER
SELECT 914
"04"
DO.0
DATA 920

FIG. 9B

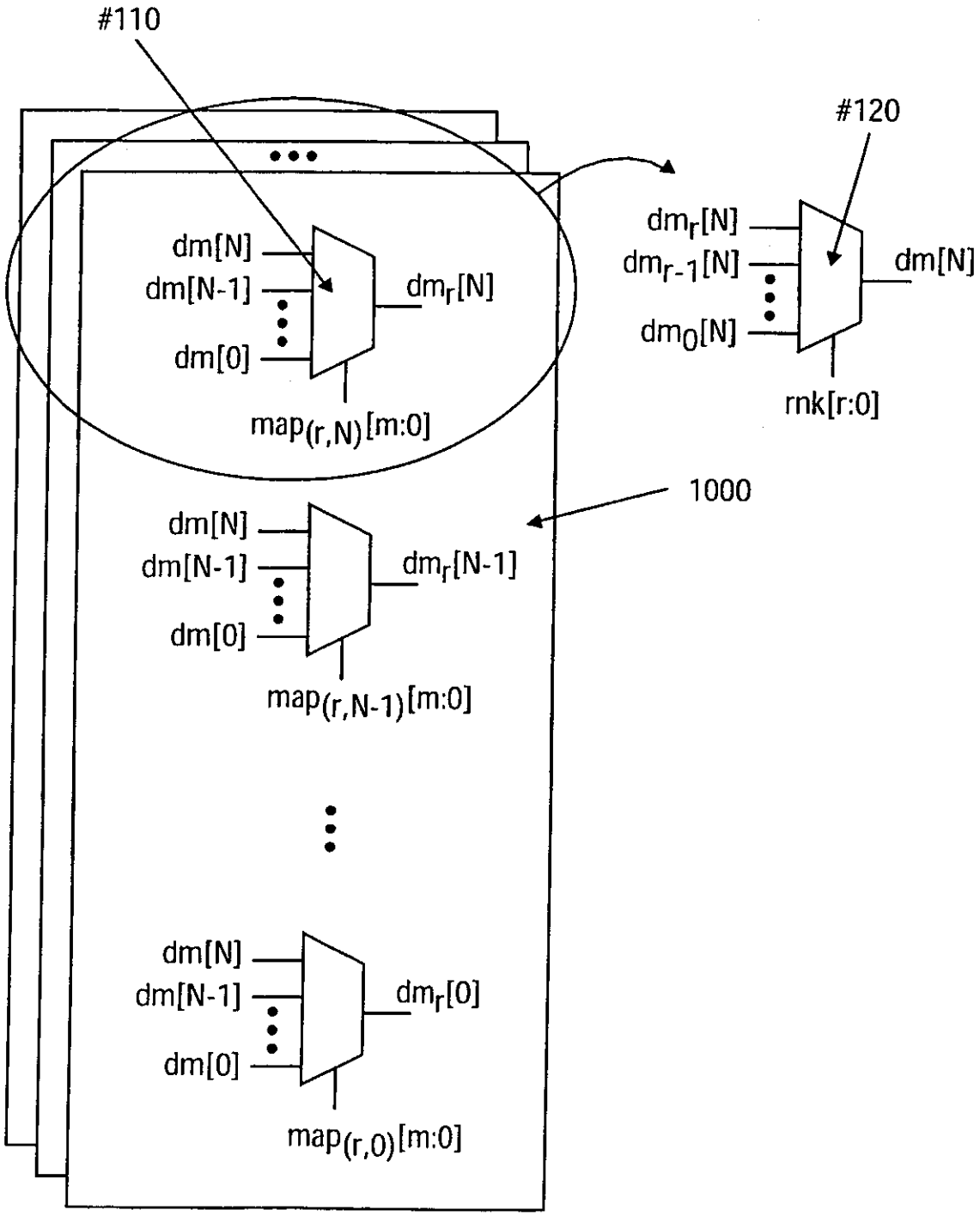

#110
#120
dm[N]
dm[N-1]
dm[0]
dm_r[N]
map_(r,N)[m:0]
dm_r[N]
dm_r-1[N]
dm_0[N]
dm[N]
rnk[r:0]
1000
dm[N]
dm[N-1]
dm[0]
dm_r[N-1]
map_(r,N-1)[m:0]
dm[N]
dm[N-1]
dm[0]
dm_r[0]
map_(r,0)[m:0]

FIG. 10

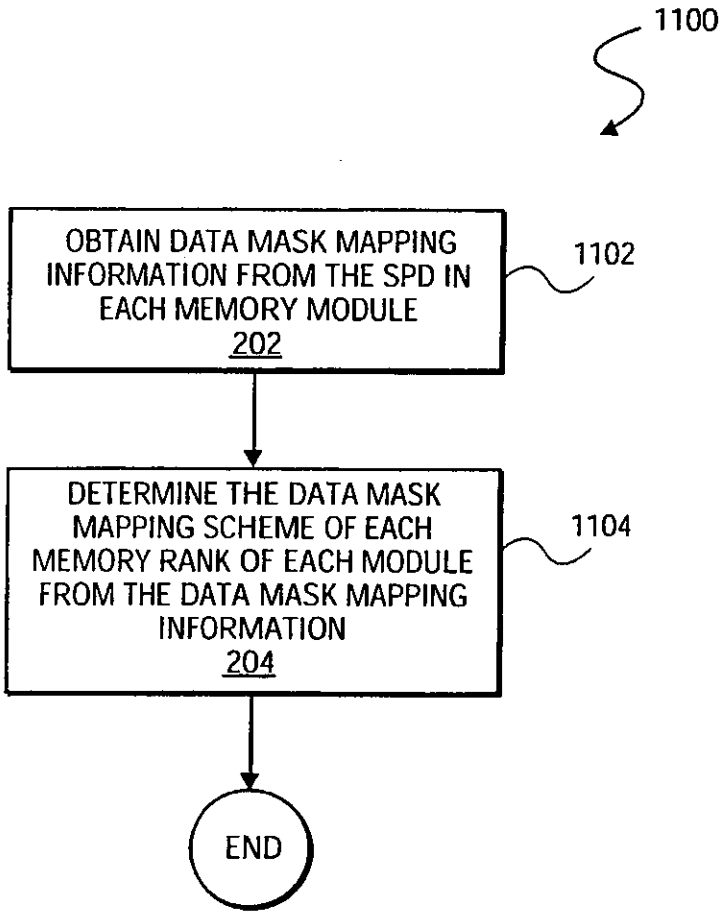

1100
OBTAIN DATA MASK MAPPING INFORMATION FROM THE SPD IN EACH MEMORY MODULE
202
1102
DETERMINE THE DATA MASK MAPPING SCHEME OF EACH MEMORY RANK OF EACH MODULE FROM THE DATA MASK MAPPING INFORMATION
204
1104
END

FIG. 11

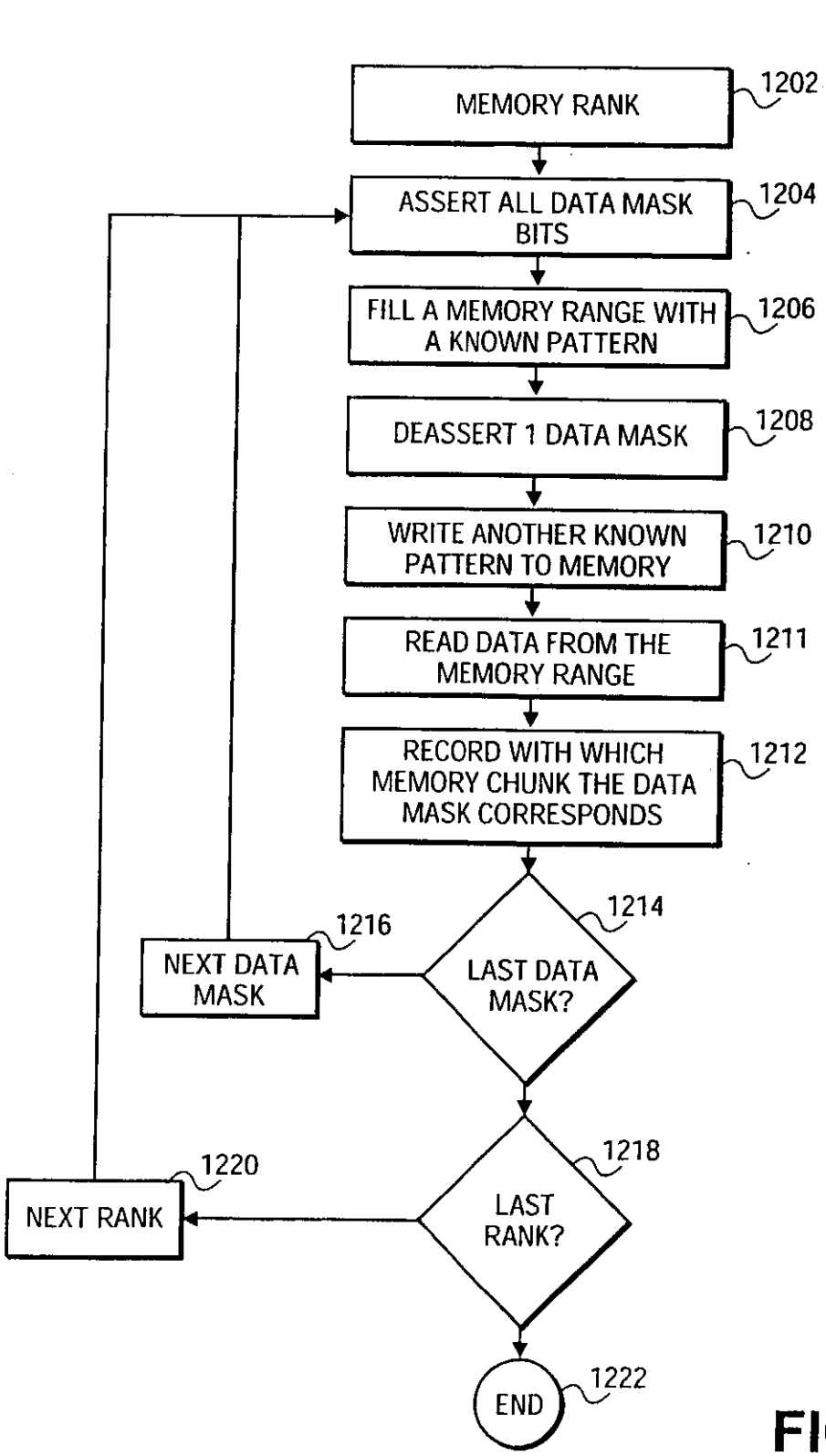

1200
MEMORY RANK
1202
ASSERT ALL DATA MASK BITS
1204
FILL A MEMORY RANGE WITH A KNOWN PATTERN
1206
DEASSERT 1 DATA MASK
1208
WRITE ANOTHER KNOWN PATTERN TO MEMORY
1210
READ DATA FROM THE MEMORY RANGE
1211
RECORD WITH WHICH MEMORY CHUNK THE DATA MASK CORRESPONDS
1212
LAST DATA MASK?
1214
NEXT DATA MASK
1216
LAST RANK?
1218
NEXT RANK
1220
END
1222

FIG. 12