

ABSTRACT

HIGH PERFORMANCE SYMMETRIC ARBITRATION PROTOCOL
SUPPORT FOR I/O REQUIREMENTS

A multiprocessor computer system comprising:

- a main memory;
- a plurality of processors coupled to said memory via a first bus, each processor including an arbitration unit;
- a plurality of digital signal processors coupled to a second bus;
- a digital signal processor arbitration unit coupled between said first bus and said second bus;
- each arbitration unit is capable of arbitrating for ownership of said first bus by asserting a request signal over said first bus, said arbitration units further receiving said request signals from another arbitration units, said arbitration units capable of asserting a lock signal during ownership of said first bus during a locked transaction; and
- said arbitration units further including a priority agent detection logic for detecting a first bus ownership request from a priority agent, wherein an arbitration unit releases ownership of said first bus when a priority agent request is detected, unless said bus transaction is a locked transaction.

Figure 1