



DESCRIPTION

FIELD EMISSION DEVICE, ITS MANUFACTURING METHOD
AND DISPLAY DEVICE USING THE SAME

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FIELD OF THE INVENTION

The present invention relates to the field of field emission devices (FEDs) employed in devices using electron beams, including flat panel display devices, sensors, high frequency oscillators, ultra high speed devices, electron
10 microscopes, and electron beam exposure devices, and their manufacturing methods. More particularly, the present invention relates to FEDs with an emitter which stabilizes emission current by integrating field effect transistors (FET); FEDs having high current density, uniformity, and satisfactory power efficiency; and their manufacturing methods.

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BACKGROUND OF THE INVENTION

The most well-known basic configuration of a conventional field emission device (FED) has a cone-type Spindt structure as disclosed C.A. Spindt
20 et al in the Journal of Applied Physics, vol. 47, p. 5238, 1976. The FED with this Spindt structure, however, has a problem with stable emission current. In particular, unstable emission current leads to a major problem when it is used in a flat display device as proposed in the Japanese Patent Examined Publication No. H6-14263 because unstable current directly affects display picture quality.

25 The Japanese Patent Examined Publication No. H7-118259 discloses a FED with stable emission using the negative feedback effect of resistance by connecting a high resistance resistor in series to an emitter emitting electrons.

However, the use of a high resistance resistor of between 10 and 100 M ohms connected in series to the emitter decreases the response of the FED, and consumes significant power. In addition to the insertion of a high resistance resistor, to solve this problem, more than 1000 emitters, for example, are
5 integrated to form an emitter array for one FED in order to counteract emitter instability by averaging the output of many emitters. However, an increase in the number of emitters adds complexity and increases the manufacturing cost of the FED.

To solve these problems, the Japanese Laid-open Patent Publication No.
10 H9-259744 discloses an approach of controlling the current flowing in the emitter by directly bonding an active element such as a transistor to the emitter of the FED. This enables the stabilization of current at low power consumption. Furthermore, it eliminates the need to form large numbers of emitters. This prior art, however, use single crystal silicon as the substrate, resulting in inability
15 to manufacture a flat display element of large size, as well as increasing costs.

Recently, the Japanese Laid-open Patent Publication No. H9-129123; H. Gamo et al, Applied Physics Letters, vol. 73, p. 1301, 1998; and Y.H. Song et al, SID 98 DIGEST, p. 189, 1998, disclose the use of a glass substrate instead of single crystal silicon to allow a larger size and reducing costs, for the purpose of
20 application to a flat panel display device. In this structure, an emitter, field effect transistor (FET), and its thin film transistor (TFT) are formed on the glass substrate using amorphous silicon and polycrystalline silicon.

Figs. 10 (a) and 10 (b) show the configuration of a conventional FED comprising an emitter array 7 and TFT 23. Fig. 10 (a) is a perspective view

illustrating an entire FED corresponding to one pixel. Fig. 10 (b) is a magnified sectional view of one emitter and TFT in the emitter array 7.

As shown in Fig. 10 (a), more than 1000 emitters 10 are formed in the emitter array 7 of the FED for each pixel controlled by one TFT 23. The current
5 emitted from the emitter array 7 is controlled by one TFT 23 connected to a corner of the emitter array 7 through a cathode electrode.

As shown in Fig. 10 (b), the FED comprises the above TFT 23 and emitter unit connected through the drain electrode 19. The TFT 23 comprises a chrome source electrode 9 on a glass substrate, n+ amorphous silicon contact
10 layer and channel i amorphous silicon layer 20, a silicon dioxide gate insulation layer 3, and a chrome gate electrode 4. The emitter unit comprises the above TFT 23, chrome drain metal 19, amorphous silicon emitter 10, silicon dioxide insulation layer 24, and niobium extraction electrode 11.

Fig. 11 shows a method for manufacturing the conventional FED. As
15 shown in Fig. 11 (a), each material is sequentially layered. Then, the portion which will become the TFT 7 is covered with a photoresist 21. Areas other than TFT are then removed by etching to expose the lower drain electrode 19 (Fig. 11 (b)). Next, an amorphous silicon layer 20 for forming the emitter is formed again (Fig. 11 (c)). The shape of the emitter is then created (Fig. 11 (d)), the
20 insulation layer 24 and extraction electrode 11 are formed on its top, and an emitter hole is created to expose the tip of the emitter (Fig. 11(e)).

In the description, a part such as a cone shape which emits cold electrons is hereafter called an emitter, and the entire device made by connecting this emitter with a transistor is called the FED.

25 The conventional FED has the following disadvantages.

When a thin amorphous or polycrystal silicon layer of 200 nm or less in thickness is formed on a glass substrate, it is not possible to obtain a silicon layer with high electron mobility and good crystallinity. If a TFT or channel layer of FET is formed on such silicon layer, a TFT or FET with uniform and good characteristics is not obtained.

In addition, an excimer laser is used for annealing the amorphous silicon on the glass substrate for crystallization. This complicates the process. Laser annealing is also disadvantageous in mass production, increasing the manufacturing cost.

Still more, the prior art requires the formation of a thin amorphous silicon layer, insulating layer, and metal layer for making a TFT or FET. These layers on the emitter are etched, and a thicker amorphous silicon layer for forming the emitter is formed again, thus complicating the process. Before forming the amorphous silicon layer again to create the emitter, its formation surface is exposed to the air. This contaminates the growing surface, and may degrade the crystallinity of the amorphous silicon layer.

Also as shown in Fig. 10 (a), numerous emitter arrays are controlled by one FET connected to one end of the array region. This makes the distance between the FET drain and each emitter chip different, causing a difference in resistance between the FET and the emitter. As a result, the emission characteristics of each emitter vary.

Furthermore, a gate and source of FET are disposed asymmetrically to the emitter array. This causes asymmetry in the space potential distribution between the emitter array and the anode substrate, which is the phosphor side,

when this FED is used in a flat panel display device. The travelling direction of the electron thus becomes anisotropic.

5 Still more, since the gate metal of the FET is covered only with the insulation layer, any small degree of external noise may affect the gate metal and erroneously trigger the FET, greatly changing the emission current of the emitter.

 As described above, the prior art FED still has a number of disadvantages, and the use of such FED in a flat panel display devices rules out high picture
10 quality, which depends on uniformity and high luminance. It also increases power consumption and cost.

SUMMARY OF THE INVENTION

15 A FED of the present invention comprises
a semiconductor layer grown on a substrate;

 a field effect transistor (FET) comprising a gate electrode, an insulation layer, a source region and a drain region; and

 at least one cone emitter formed on one of said drain region of said FET
20 and a portion of said semiconductor layer contacting said drain region, said cone emitter being formed by etching the semiconductor layer; characterised in that said FET is formed on a surface of said semiconductor layer and said semiconductor layer has a thickness not less than the height of said cone emitter.

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The semiconductor layer may be formed using the chemical vapour
5 deposition method (CVD method) utilizing a catalytic effect caused by the contact
of semiconductor material gas with a metal having high melting point heated to a
high temperature.

An emitter or an array comprising more than one emitter may be formed
in a circular or polygonal FET drain region. The emitter array is surrounded by
10 ring or polygonal gate electrode and source electrode. The entire FET is then
covered with an insulation layer and metal layer.

The above configuration provides the following effects.

A thick polysilicon layer of 500 nm or above may be directly formed at the
rate of 0.2 nm/s or faster, which is a relatively high speed. This enables
15 elimination of the polycrystallization process using laser annealing after the
formation of the polysilicon layer. In addition, the thick layer improves
crystallinity near the surface, and achieves high mobility, enabling manufacture of
an FET with uniform and good characteristics.

The creation of an FET and emitter by growing the semiconductor layer in
20 a single step also simplifies the process. The elimination of the second step to
obtain a thick semiconductor layer avoids exposure of the growing surface to the
air, preventing the possibility of contaminating the surface.

The formation of the emitter array in the circular or polygonal FET drain
region equalizes a distance between the FET drain and each emitter, enabling
25 averaging of the resistance to each emitter, and thus enabling unifying emission
characteristics of each emitter chip. Furthermore, space potential distribution
between the emitter array and anode substrate becomes symmetrical within the
substrate, enabling the emission of electrons uniformly to all directions. The ratio
of FET (gate width/gate length) also becomes large, enabling manufacture of the
30 FET with a high current level even though the mobility of the FET is low.

The metal layer is provided to the FET to shield noise. This prevents erratic operation of FET by being affected by a faint external noise and greatly fluctuating emission current of the emitter.

The above characteristics of FED applied to a flat panel display device
5 enables to offer a high picture quality, including uniformity and high luminance, low power consumption, and low cost.

BRIEF DESCRIPTION OF THE DRAWINGS

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Fig. 1 is a sectional view of a FED in accordance with a first exemplary embodiment of the present invention.

Fig. 2 is a sectional view of a cone-type FED in accordance with the first exemplary embodiment of the present invention..

15 Fig. 3 is a sectional view illustrating a manufacturing process of a FED in accordance with the first exemplary embodiment of the present invention.

Fig. 4 is a sectional view of a FED in accordance with a second exemplary embodiment of the present invention.

20 Fig. 5 is a sectional view of a FED in a third exemplary embodiment of the present invention.

Fig. 6 is a sectional view of a FED in accordance with a fourth exemplary embodiment of the present invention.

Fig. 7 (a) is a plan view of a FED in accordance with a fifth exemplary embodiment of the present invention.

Fig. 7 (b) is a sectional view of the FED in accordance with the fifth exemplary embodiment of the present invention.

Fig. 8 is sectional view of the FED with convergence electrode in accordance with the fifth exemplary embodiment of the present invention.

5 Fig. 9 is a sectional view of a FED in accordance with a sixth exemplary embodiment of the present invention.

Fig. 10 (a) is a perspective of a conventional FED.

Fig. 10 (b) is a magnified sectional view of a part concerned of an element of the conventional FED.

10 Fig. 11 is a sectional view illustrating a manufacturing method of the conventional FED.

DESCRIPTION OF THE PREFERRED EMBODIMENT

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First exemplary embodiment

A first exemplary embodiment of the present invention is described below with reference to Figs. 1, 2, and 3.

As shown in Fig. 1, a FED of the present invention comprises a substrate
20 1, semiconductor layer 2, FET gate insulation layer 3, FET gate metal 4, FET source region 5, FET drain region 6, and emitter array 7.

In the first exemplary embodiment, the emitter array 7 is formed by etching the semiconductor layer 2 on the FET drain region after forming the FET. In other words, the first exemplary embodiment enables the formation of both
25 FET and emitter by a single growth of the semiconductor layer 2. Prevention of

exposure of the surface to the air, which is a problem with the growth of the semiconductor layer 2 in two stages, enables the simplification of the process and prevents degradation of crystallinity.

Fig. 2 shows a sectional view of the FED after a cone emitter 10 and
5 extraction electrode 11 are added to the emitter unit shown in Fig. 1. In addition to Fig. 1, Fig. 2 shows an impurity diffusion preventing layer 8, FET source electrode 9, one cone emitter 10 in the emitter array 7, extraction electrode 11, insulation layer under the extraction electrode 12, and FET passivation layer 13.

Since the cone emitter is located at the center of a cylindrical hole, the
10 electric field is uniformly concentrated at its tip, emitting cold electrons uniformly and at relatively low voltage. Accordingly, the use of a cone emitter and extraction electrode in the FET configuration shown in Fig. 1 enables satisfactory cold electron emission characteristics to be achieved.

The substrate 1 is a single crystal or polycrystalline substrate made of
15 semiconductors such as silicon. In particular, the use of an amorphous glass substrate enables enlargement of its size, and allows reduced cost and larger screen size when applied to display elements.

In general, satisfactory crystallinity is not achievable with a thin layer thinner than 200 nm at the initial stage of layer formation because the lattice
20 constants of crystals differ when the polycrystalline semiconductor layer 2 is formed on the glass substrate 1. The crystallinity then improves gradually after the layer thickness exceeds 500 nm. Accordingly, formation of the FET on the crystal surface of a layer above 500 nm thick facilitates the formation of the semiconductor layer 2 with an electron mobility in excess of $10 \text{ cm}^2/\text{V}\cdot\text{s}$. One
25 method of forming the semiconductor layer 2 is the CVD method which utilizes

the catalytic effect caused by the contact of semiconductor material gas with a metal having high melting point heated to a high temperature. If micro grain silicon or polycrystalline silicon is grown using this CVD method, the semiconductor layer 2 with electron mobility above $10 \text{ cm}^2/\text{V}\cdot\text{s}$ is obtained, and
5 this is suitable for controlling emission current from the emitter.

The impurity diffusion preventing layer 8 is provided to prevent any detrimental effects created by elements in the substrate thermally diffusing to the semiconductor layer as impurities when the substrate and the semiconductor layer on top have different compositions. In particular, a closely packed layer of
10 silicon oxide and silicon nitride which are used in general processes can effectively suppress any diffusion of impurities and also can be easily manufactured.

As for the semiconductor 2, Group IV semiconductors such as silicon and Group III-V semiconductors such as gallium and arsenic may be used. In
15 particular, semiconductors with a wide band gap such as diamond, boron nitride, and gallium nitride themselves have small electron affinity. These types emit electrons in a vacuum at low voltage, and are thus suitable for use as the emitter. Extensive studies have also been done on the use of silicon in integrated circuits, and silicon also has a stable oxide layer. Accordingly, the use of silicon is
20 advantageous for controlling the emitter using an integrated circuit. Since the above semiconductors may also be used as the emitter, an emitter combined with an FET is easily manufactured.

For manufacturing an n-channel FET that is able to respond rapidly and is able to flow large current, p-type semiconductor may be used as the material
25 for the semiconductor layer 2. The p-type semiconductor can be made by

doping boron or aluminum or to Group IV semiconductors, or by doping magnesium and zinc to Group III-V semiconductors. On the other hand, for manufacturing a n-channel FET, n-type semiconductor may be used. The n-type semiconductor can be made by doping phosphorus or arsenic to Group IV semiconductor, and by doping silicon or sulfur to Group III-V semiconductors. For integrating an electronic circuit to control the operation of the emitter, a c-MOS circuit is appropriate. In this case, both n-channel and p-channel FETs are necessary.

The semiconductor layer 2 may have an amorphous, a polycrystalline or a single crystal structure. When using a single crystal for the semiconductor layer 2, the materials for substrate 1 may be limited. For large glass substrates, it may be necessary to use amorphous or polycrystalline semiconductor layer 2. In this case, hydrogen treatment is effective for improving crystallinity by terminating dangling bonds inside the semiconductor.

The FET gate insulation layer 3 may be made of silicon dioxide, silicon nitride, or their composites which have high electrical insulation ability and a very dense structure. To reduce distortion in the insulation layer 3, single layers of these materials are combined to create multiple layers. If the CVD method is used for manufacturing the insulation layer 3, layers from the semiconductor layer to silicon nitride layer may be consecutively formed without causing any damage to the semiconductor layer. An FET with good characteristics may thus be manufactured. The above insulation layer 3 may also be used as an etching mask for processing the emitter, or a mask for doping ions in the drain region of the FET.

For processing the shape of emitter, the above insulation layer 3 may be used as a mask. The insulation layer 3 may also be used as a mask for doping ions in the FET drain region.

For metal wiring including the FET gate metal 4, FET source electrode 9, and extraction electrode 11; aluminum, which is inexpensive, has low electrical resistance, and can be used to form good quality anode oxide layer; may be used. Alternatively, copper, which is inexpensive and has an even lower electrical resistance; titanium, which improves adhesion to the glass substrate; or tantalum, which can form good quality anode oxide layer may be used. Other elements such as neodymium may be added, for example to aluminum, for suppressing hillocks, and to create an alloy containing the major constituent at 95 weight percent or more.

When forming a metal layer on the glass substrate, a thin titanium layer of 100 nm or less may be formed first followed by aluminum layer formation to improve adhesion and electrical conductivity. Accordingly, these metal elements may be used as a single layer or combined to form multiple layers to exploit the best characteristics of each metal.

Figs 3 (a) to 3 (f) show sectional views of an example of the manufacturing process of the FED in the first exemplary embodiment.

As shown in Fig. 3 (a), the impurity diffusion preventing layer 8, semiconductor layer 2 and FET gate insulation layer 3 are formed consecutively using the plasma assisted CVD method, followed by a FET gate metal 4 deposition by vacuum deposition. Next, as shown in Fig. 3 (b), the gate metal 4 and gate insulation layer 3 are patterned by etching such as reactive ion etching to determine the position of the FET and emitter.

Then, as shown in Fig. 3 (c), the cone emitter is formed using the gate insulation layer 3 as the mask for an etching such as reactive ion etching.

Next, as shown in Fig. 3 (d), the FET source region 5 and FET drain region 6 are formed using doping technology such as ion implantation. The
5 emitter is doped at the same time.

As shown in Fig. 3 (e), the insulation layer 12 under the extraction electrode 11 is formed typically using the plasma assisted CVD method, after which a contact hole is etched in the source region 5, and the FET source electrode 9 is formed typically using sputtering.

10 As shown in Fig. 3 (f), the FET passivation insulation layer 13 and extraction electrode 11 are consecutively formed, typically using the plasma assisted CVD method.

Lastly, as shown in Fig. 3 (g), the extraction electrode 11 and insulation layer under extraction electrode 12 are etched to expose the cone emitter.

15 The insulation layer 13 is made to be etched more slowly than that of the insulation layer 12. For example, silicon dioxide may be used for the insulation layer 12 and silicon nitride may be used for the insulation layer 13, or the insulation layer 13 is made to be thicker than that of the insulation layer 12. This is because if the insulation layer 12 and insulation layer 13 are made of the
20 same material and same thickness, the FET itself may be destroyed by dissolving in etching agent while the extraction electrode 11 and insulation layer 12 are being etched to expose the emitter.

The semiconductor layer 2 or gate insulation layer 3 shown in Fig. 3 (a) is preferably formed using one or more of mono-silane, di-silane, hydrogen,
25 nitrogen, ammonia, methane, ethane, propane, butane, trimethyl gallium, triethyl

gallium, trimethyl aluminum, arsine, phosphine, and di-borane as material gas for the CVD utilizing the catalytic effect of metals having high melting point such as tungsten, tantalum, and molybdenum (the so-called hot wire method). This enables the formation of a polysilicon layer of 500 nm thick or more with
5 electron mobility above $10 \text{ cm}^2 \cdot \text{V} \cdot \text{s}$ at a relatively fast rate of around 0.2 to 0.5 nm/s even at relatively low temperatures of below 500°C or below, compared to the ordinary plasma assisted CVD using RF discharge. Consequently, no post-annealing process for polycrystallization such as using excimer laser annealing is necessary.

10 Furthermore, as shown in Fig. 3 (c), the use of part of the gate insulation layer 3 as an etching mask for etching the cone emitter simplifies the process.

As shown in Fig. 3 (d), the electrical resistance among the FET source region 5, FET drain region 6, cone emitter 10, FET drain, and emitter is adjustable using ion implantation, also simplifying the process. If ions are
15 implanted between the FET drain and emitter, leaving a part of the FET gate insulation layer 3, this remaining part will not be doped or less doped, enabling fine adjustment of the electrical resistance of the entire channel between the FET drain and emitter.

Ion doping amount is also adjustable according to the thickness of the
20 FET gate insulation layer 3, and thus resistance is also adjustable. Since the resistance between each emitter and drain is adjustable, the electron emission from each emitter can be made uniform. In addition, if high electrical resistance is provided between the emitter and drain, changes in electron emission from the emitter over time may be stabilized by negative feedback of resistance.

In the process shown in Fig. 3 (g), the crystallinity of the semiconductor layer 2 may be improved by thermal treatment, and thus the characteristics of the FET and in-plane uniformity may be improved. In particular, in the case of amorphous silicon and polycrystalline silicon, thermal treatment may be implemented in a simple nitrogen or inert gas if a silicon nitride passivation layer containing a large amount of hydrogen is formed. In general, however, FET characteristics are effectively improved by thermal treatment in an atmosphere containing hydrogen or water vapor.

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Second exemplary embodiment

A second exemplary embodiment of the present invention is described with reference to Fig. 4. The surface of the emitter 10 is covered with a carbon protective layer 14 such as diamond or diamond-like carbon which is chemically inactive and does not degrade electron emission characteristics, so as to make the surface of the emitter chemically inactive. As a result, satisfactory electron emission characteristics may be maintained even in a relatively low vacuum without being damaged by impact or adsorption of remaining gas in the vacuum system. The protective layer 14 is formed after the step shown in Fig. 3 (f) at areas other than an electrode pad, typically using the microwave excitation plasma assisted CVD.

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Third exemplary embodiment

A third exemplary embodiment of the present invention is described next with reference to Fig. 5.

As shown in Fig. 5, a FED of present exemplary embodiment include a high resistance region 15 between the gate and source and between the gate and drain of FET. The high resistance region 15 can be created by reducing doping amount between the gate and source and between the gate and drain. The
5 structure of the third exemplary embodiment enables the prevention of drifting of emission current due to impact ion effect generated by high electric field around the drain electrode, and thus reduces the OFF current and the impact ion effect.

Fourth exemplary embodiment

10 A fourth exemplary embodiment of the present invention is described next with reference to Fig. 6.

When the glass substrate 1 or impurity diffusion preventing layer 8 is amorphous, or they have different lattice constant from the semiconductor layer 2, crystallization of the semiconductor layer formed on the glass substrate 1 or
15 impurity diffusion preventing layer 8 is difficult. Even the semiconductor layer is crystallized, distortion or defect density may increase. In order to reduce such distortion or defect density, the FED of the fifth exemplary embodiment inserts an amorphous layer 16 of 100 nm thick or less between the substrate and semiconductor layer or between the impurity diffusion preventing layer and
20 semiconductor layer.

For example, if polycrystalline silicon is formed on the glass substrate, the strained super lattice of silicon and germanium or amorphous silicon layer of 100 nm thick or less may be inserted using the plasma assisted CVD method so as to prevent propagation of defective crystal growth generated at the interface.
25 Distortion caused by a difference in lattice constant or in thermal expansion

coefficient may further be reduced to assist crystallization of the semiconductor layer 2. The amorphous silicon layer may also be formed before the formation of the polycrystalline silicon layer using the same process at lower temperature than that for polysilicon. This type of amorphous silicon layer is particularly
5 effective for uniform crystallization of the polycrystalline silicon layer within the entire substrate at a later process.

Fifth exemplary embodiment

A fifth exemplary embodiment of the present invention is described
10 below with reference to Figs. 7 and 8.

The manufacturing process of an FED in this exemplary embodiment is the same as that illustrated in Fig. 3. The difference is that, as shown in Fig. 7, a ring gate structure is adopted for the FET, and the emitter is formed in a circular drain region at the center of the FET.

15 The emitters 10 are disposed in concentric or rotational symmetry in the circular drain region 6 so that the distance between the FET gate and each emitter remains equal. Equal resistance to each emitter makes it possible to equalize the emission current from each emitter as well as preventing leak current from the FET.

20 Moreover, the electric field created by the extraction electrode 11, gate metal 4, and source electrode 3 has an equal effect on electrons emitted from the emitters, and thus electrons are emitted uniformly to all directions. Furthermore, the ring gate structure enables a large gate width / Gate length (W/L) ratio in FET to be secured, allowing FETs acceptable with a high current to be

manufactured even though the electron mobility of the semiconductor layer 2 is low.

If an FET with the same current level as the prior art as shown in Fig. 10 (a) is created, the gate area ($W \times L$) can be made larger than in the prior art ,
5 enabling to reduce the deviation of W/L ratio within the substrate that occurs due to the deviation in manufacturing dimensions of FETs.

In case of the n-channel FET, however, the gate voltage is generally controlled by the positive electric field. This attracts electrons emitted from the emitter, and makes electrons spread somewhat in the substrate. A convergence
10 electrode 17 in the negative electric field is thus formed on the ring FET, as shown in Fig. 8, in order to adjust the spreading angle of emission electrons. The extraction electrode 11 shown in Fig. 3 (f) may also be patterned to act as the convergence electrode 17.

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Sixth exemplary embodiment

A sixth exemplary embodiment of the present invention is described with reference to Fig. 9.

In the sixth exemplary embodiment, the entire FET is covered with a
20 metal layer 18 to create a noise shield for the FET. This eliminates a large fluctuation in emission current from the emitter formed in the FET drain due to a small external noise generated by an inductive noise to the gate metal. The extraction electrode 11 shown in Fig. 3 (f) may be patterned to act as this metal layer 18. The metal layer 18 may also be maintained to a ground potential to
25 achieve sufficient noise shielding effect.

Industrial applicability

As described above, the FED of the present invention enables the manufacturing of an emitter array with FETs with uniform and satisfactory characteristics using the simple process of forming the semiconductor layer on a large glass substrate in a single step, without the need for a post-annealing process.

In addition, the use of a metal layer shielded type FET having ring gate confers strong resistance to external noise, enables to control relatively large current emission characteristics uniformly, and obtains emitter characteristics with uniform electron emissions to all directions. Accordingly, factors crucial to high picture quality, including uniformity and high luminance, low power consumption, and low cost are realizable when the FED of the present invention is applied to a flat panel display device.

CLAIMS

1. A field emission device comprising:
 - 5 a semiconductor layer grown on a substrate;
 - a field effect transistor comprising a gate electrode, an insulation layer, a source region and a drain region; and
 - at least one cone emitter formed on one of said drain region of said field effect transistor and a portion of said semiconductor layer contacting said drain
 - 10 region, said cone emitter being formed by etching said semiconductor layer;
 - characterised in that said field effect transistor is formed on a surface of said semiconductor layer and said semiconductor layer has a thickness not less than the height of said cone emitter.
- 15 2. The field emission device as defined in Claim 1, wherein the thickness of the semiconductor layer is not less than 500nm.
3. The field emission device as defined in Claim 1, wherein an extraction electrode for emitting electron is formed, said extraction electrode being formed in
- 20 a way not to contact said emitter and said drain region.
4. The field emission device as defined in Claim 1, wherein said substrate is an amorphous substrate.
- 25 5. The field emission device as defined in Claim 1 further comprising an impurity diffusion preventing layer between said substrate and said semiconductor layer.

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6. The field emission device as defined in Claim 5, wherein said impurity
5 diffusion preventing layer is made of one of a single layer of one of silicon dioxide
and silicon nitride, multiple layers of their combination and their composite layer.

7. The field emission device as defined in Claim 1, wherein said semiconductor layer is mainly made of one of a IV group element in a periodic table and composite semiconductor of the combination of the IV group elements.

5 8. The field emission device as defined in Claim 1, wherein said semiconductor layer is made of a composite semiconductor of the combination of III group elements and V group elements in a periodic table.

 9. The field emission device as defined in Claim 1, wherein said
10 semiconductor layer is one of a doped p-type semiconductor and n-type semiconductor.

 10. The field emission device as defined in one of Claims 1 and 9,
wherein said semiconductor layer is one of a p-type semiconductor doped with
15 one of boron, aluminum, magnesium, and zinc; and a n-type semiconductor doped with one of phosphorous, arsenic, antimony, silicon, and sulfur.

 11. The field emission device as defined in Claim 1, wherein said
semiconductor layer has a structure one of amorphous, hydrogen treated
20 amorphous, polycrystalline, and hydrogen treated polycrystalline.

 12. The field emission device as defined in Claim 1, wherein said
insulation layer of the field effect transistor is made of one of a single layer of
one of silicon dioxide and silicon nitride, multiple layers of their combination,
25 and their composite layers.

13. The field emission device as defined in Claim 1, wherein a metal layer of said field effect transistor and all metal wirings are made of one of a single layer containing at least 95 weight percent of one of aluminum, copper,
5 titanium, and tantalum, and multiple layers of their combination.

14. The field emission device as defined in Claim 3, wherein an insulation layer having lower etching speed than the etching speed of an insulation layer under said extraction electrode is used as a passivation insulation
10 layer of said field effect transistor.

15. The field emission device as defined in Claim 14, wherein silicon dioxide is used for the insulation layer under said extraction electrode, and silicon nitride is used for the passivation layer of said field effect transistor.

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16. The field emission device as defined in Claim 3, wherein the gate insulation layer of said field effect transistor is thicker than an insulation layer under said extraction electrode.

20 17. The field emission device as defined in Claim 1, wherein a surface of said emitter is covered with a chemically inactive protective layer which does not degrade electron emission characteristics.

18. The field emission device as defined in Claim 17, wherein said
25 protective layer is made of carbon .

19. The field emission device as defined in Claim 1, wherein a layer having
5 higher electric resistance than source and drain is inserted between one of i) source
and drain, and ii) drain and gate of said field effect transistor.
20. The field emission device as defined in Claim 1, wherein said
semiconductor layer is one of polycrystalline and single crystal layers containing
10 one of a strained super lattice layer and an amorphous layer not thicker than 100
nm.
21. The field emission device as defined in claim 1, wherein said field effect
transistor comprises:
15 one of a circular and polygonal drain region, having an emitter array
formed therein;
one of a ring and polygonal gate electrode around said drain region; and
a source electrode around said gate electrode.
- 20 22. The field emission device as defined in Claim 21, wherein an emitter is
disposed in said drain region at one of concentric and rotational symmetric
position.
23. The field emission device as defined in Claim 21, wherein said emitter
25 array has one of ring and polygonal ring convergence electrode, said convergence
electrode surrounding said emitter array in rotational symmetry.
24. The field emission device as defined in Claim 23, wherein said convergence
electrode also acts as an extraction electrode for electron emission.

25. The field emission device as defined in claim 21, wherein an upper
5 part of said field effect transistor is covered with an insulation layer and metal
layer.
26. The field emission device as defined in Claim 25, wherein said metal layer
also act as a extraction electrode for electron emission.
- 10 27. The field emission device as defined in Claim 25, wherein said metal layer
is maintained to a ground potential.
28. A method of manufacturing the field emission device as defined in claim 1,
15 comprising:
growing said semiconductor layer on one of the substrate and an impurity
diffusion protection layer formed on a substrate;
forming a gate insulation layer and a gate metal layer on said
semiconductor layer;
20 forming a gate and the gate electrode of the field effect transistor by
patterning said gate metal layer and said gate insulation layer;
forming said at least one cone emitter by etching a portion of the drain
region of said field effect transistor;
doping an impurity on a surface of at least one of a source, a drain and an
25 emitter of said field effect transistor;

forming said source electrode via said gate insulation layer of said field
5 effect transistor;
forming a passivation layer on said field effect transistor;
forming an extraction electrode via one of said insulation layer and air
against said cone emitter; and
heat treating one of said field effect transistor and an emitter region of said
10 field effect transistor.

29. The method of manufacturing a field emission device as defined in Claim
28, wherein said emitter and said semiconductor layer of said field effect transistor
are made of the same material, and formed simultaneously.

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30. The method of manufacturing a field emission device as defined in Claim
28, further comprising the step of forming an impurity diffusion preventing layer
between said substrate and said semiconductor layer.

20 31. The method of manufacturing a field emission device as defined in Claim
28, wherein one of said semiconductor layer and said insulation layer is formed
using a chemical vapour deposition method utilizing a catalytic effect caused by
the contact of material gas with a metal having high melting point heated to a high
temperature.

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32. The method of manufacturing a field emission device as defined in Claim
31, wherein said material gas is at least one of monosilane, di-silane, hydrogen,
nitrogen, ammonia, methane, ethane, propane, butane, trimethyl gallium, triethyl
gallium, trimethyl aluminium, arsine, phosphine, and di-borane.

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33. The method of manufacturing a field emission device as defined in Claim
5 31, wherein said metal having high melting point is at least one of tungsten,
tantalum, and molybdenum.

34. The method of manufacturing a field emission device as defined in Claim
28, wherein said insulation layer is used as an etching mask for processing a shape
10 of said emitter.

35. The method of manufacturing a field emission device as defined in Claim
28, wherein electric resistance in said drain region in which said emitter is formed
is adjusted by ion implantation.

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36. The method of manufacturing a field emission device as defined in Claim
35, wherein ions are implanted in said drain region, while said insulation layer is
remained.

20 37. The method of manufacturing a field emission device as defined in Claim
28, wherein said semiconductor layer is thermally treated in one of nitrogen and
inert gas atmosphere at not higher than 500 °C and an atmosphere containing one
of hydrogen and water vapour.

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