METHOD FOR FORMING SEMICONDUCTOR STRUCTURE, PLASMA GENERATOR, AND SEMICONDUCTOR PROCESS APPARATUS

TECHNICAL FIELD

[0001] The present disclosure belongs to the technical field of semiconductors, and particularly relates to a method for forming a semiconductor structure, a plasma generator, and a semiconductor process apparatus.

BACKGROUND

[0002] Plasma plays an important role in the etching process. Active substances in the plasma, such as uncharged free radicals and charged ions, react with semiconductor film layers to obtain desired patterns.

[0003] When the wafer is processed, different types of etching processes are required, such as isotropic etching in some process steps and anisotropic etching in other process steps. In the related art, different reaction chambers are required for isotropic etching and anisotropic etching. When the wafer needs to undergo anisotropic etching after undergoing isotropic etching in one reaction chamber, the reaction chamber needs to be purged and evacuated. Then, the wafer is taken out of the reaction chamber by a manipulator and transferred to another reaction chamber, to undergo anisotropic etching. In the process, since the wafer needs to be transferred between chambers, the etching throughput is low.

SUMMARY

[0004] The present disclosure discloses a method for forming a semiconductor structure, a plasma generator, and a semiconductor process apparatus, to solve the problem of low etching throughput caused by transfer between chambers when a semiconductor process apparatus involved in the related art performs different etching processes.

[0005] To solve the technical problem, the present disclosure provides a technical solution as follows:

[0006] In a first aspect, embodiments of the present disclosure disclose a method for forming a semiconductor structure. The method is applied to a semiconductor process apparatus, where the semiconductor process apparatus includes a plasma generation chamber and a reaction chamber communicating with each other, and the method includes:

[0007] performing a first etching process on a stacked semiconductor structure, to form a plurality of fin structures spaced apart from one another, where the stacked semiconductor structure includes at least one first semiconductor layer and at least one second semiconductor layer that are alternately stacked; and separating the plasma generation chamber from the reaction chamber by a first distance when the first etching process is performed; and

[0008] performing a second etching process on the fin structures, to selectively etch at least a portion of one of the first semiconductor layer and the second semiconductor layer, and separating the plasma generation chamber from the reaction chamber by a second distance when the second etching process is performed, where the second distance is greater than the first distance.

[0009] In a second aspect, the embodiments of the present disclosure disclose a plasma generator, the plasma generator is configured to cooperate with a reaction chamber, and the plasma generator includes:

[0010] a plasma generation chamber configured to generate plasma; and

[0011] a plasma delivery tube, where the one end of the plasma delivery tube communicates with the plasma generation chamber, the other end of the plasma delivery tube is configured to communicate with the reaction chamber, and the plasma delivery tube is adjustable in length, to move the plasma generation chamber close to or away from the reaction chamber.

[0012] In a third aspect, the embodiments of the present disclosure disclose a semiconductor process apparatus. The semiconductor process apparatus disclosed includes:

[0013] a reaction chamber; and

[0014] the plasma generator in the second aspect, where a plasma generation chamber communicates with the reaction chamber through a plasma delivery tube.

[0015] The technical solution provided by the present disclosure can achieve the following beneficial effects:

[0016] According to the method for forming a semiconductor structure disclosed in the embodiments of the present disclosure, a distance between the plasma generation chamber and the reaction chamber is adjusted, a delivery distance of the plasma is adjusted, and finally a concentration of free radicals in the plasma is adjusted. Different concentrations of the free radicals can adapt to different etching processes, and achieve different etching effects. In this case, when the plasma etching processes requiring different concentrations of free radicals are performed on the stacked semiconductor structure, merely the distance between the plasma generation chamber and the reaction chamber needs to be adjusted, and different types of etching processes do not

need transfer between different process chambers, such that the problem of low etching throughput is avoided.

BRIEF DESCRIPTION OF DRAWINGS

[0017] FIG. 1 is a schematic flowchart of a method for forming a semiconductor structure according to an embodiment of the present disclosure;

[0018] FIG. 2 is a schematic diagram of a substrate and a stacked semiconductor structure on the substrate after a first etching process is completed by a method for forming a semiconductor structure according to an embodiment of the present disclosure;

[0019] FIG. 3 is a schematic diagram of a substrate and a stacked semiconductor structure on the substrate after a second etching process is completed by a method for forming a semiconductor structure according to an embodiment of the present disclosure;

[0020] FIG. 4 is a scanning electron micrograph obtained by etching a stacked semiconductor structure by using process gas containing no nitrogen;

[0021] FIG. 5 is a scanning electron micrograph obtained by etching a stacked semiconductor structure by using process gas to which nitrogen is added;

[0022] FIG. 6 is a schematic structural diagram of a semiconductor process apparatus according to an embodiment of the present disclosure.

[0023] FIG. 7 is another schematic structural diagram of a semiconductor process apparatus according to an embodiment of the present disclosure;

[0024] FIG. 8 is a first schematic structural diagram of a plasma delivery tube according to an embodiment of the present disclosure;

[0025] FIG. 9 is a second schematic structural diagram of a plasma delivery tube according to an embodiment of the present disclosure;

[0026] FIG. 10 is a third schematic structural diagram of a plasma delivery tube according to an embodiment of the present disclosure;

[0027] FIG. 11 is a fourth schematic structural diagram of a plasma delivery tube according to an embodiment of the present disclosure;

[0028] FIG. 12 is a fifth schematic structural diagram of a plasma delivery tube according to an embodiment of the present disclosure;

[0029] FIG. 13 is a schematic structural diagram of another semiconductor process apparatus with a filter partition plate in a reaction chamber according to an embodiment of the present disclosure;

[0030] FIG. 14 is a schematic structural diagram of yet another semiconductor process apparatus with a filter partition plate in a partition plate storage chamber according to an embodiment of the present disclosure; and

[0031] FIG. 15 is a schematic structural diagram of another filter partition plate according to an embodiment of the present disclosure.

[0032] Description of reference numerals:

[0033] 10-reaction chamber, 11-inner chamber, 101-first subspace, 102-second subspace,

[0034] 20-plasma generator, 21-plasma generation chamber, 22-plasma delivery tube, 23-first driving mechanism, 24-magnetic isolation cover, 25-sealing cover,

[0035] 30-bearing seat, 40-filter partition plate, 41-through hole, 50-second driving mechanism, 60-partition plate storage chamber,

[0036] 01-delivery tube section, 02-annular gap, 03-sealing ring, 031-first magnetic ring, 032-second magnetic ring, 033-magnetic fluid, 034-inner sealing lip, 035-outer sealing lip, 036-base,

[0037] 001-substrate, 002-stacked semiconductor structure, 021-first semiconductor layer, 022-second semiconductor layer, and 023-fin structure.

DETAILED DESCRIPTION

[0038] In order to make objectives, technical solutions and advantages of the present disclosure clearer, the technical solutions of the present disclosure will be clearly and completely described below in conjunction with the specific embodiments and corresponding accompanying drawings of the present disclosure. Apparently, the embodiments described are merely some embodiments rather than all embodiments of the present disclosure. All other embodiments derived by those of ordinary skill in the art from the embodiments of the present disclosure without creative efforts should fall within the protection scope of the present disclosure.

[0039] With reference to FIG. 1 to FIG. 15, the technical solutions according to various embodiments of the present disclosure will be described in detail below.

[0040] The embodiments of the present disclosure disclose a method for forming a semiconductor structure. The semiconductor structure may be configured to form a gate-all-around field effect transistor (GAA-FET) or a memory cell of a three-dimension NAND (3D NAND), for example. The

method is applied to a semiconductor process apparatus. The semiconductor process apparatus involved in the embodiment of the present disclosure includes a reaction chamber 10 and a plasma generation chamber 21. The reaction chamber 10 and the plasma generation chamber 21 communicate with each other. The plasma generation chamber 21 is configured to generate plasma. After being generated, the plasma may be delivered to the reaction chamber 10 to participate in the etching process.

[0041] With reference to FIG. 1, the method for forming a semiconductor structure according to the embodiment of the present disclosure includes:

[0042] S101, a first etching process is performed on a stacked semiconductor structure 002, to form a plurality of fin structures 023 spaced apart from one another.

[0043] For example, the stacked semiconductor structure 002 may be formed on a substrate 001 in a chemical vapor deposition chamber through a deposition process. The stacked semiconductor structure 002 includes at least one first semiconductor layer 021 and at least one second semiconductor layer 022 that are alternately stacked. A structure formed after step S101 is completed is shown in FIG. 2. Each fin structure 023 is formed by alternately stacking a portion of one first semiconductor layer 021 and a portion of one second semiconductor layer 022. That is, the fin structure 023 includes the portion of the first semiconductor layer 021 and the portion of the second semiconductor layer 022. When the first etching process is performed, the plasma generation chamber 21 and the reaction chamber 10 are separated by a first distance. In some embodiments, the plurality of fin structures 023 may be spaced apart from one another in an extending direction of the substrate 001. The first etching process may be, for example, an anisotropic etching process. By applying a radio frequency bias to a lower electrode of the reaction chamber 10, charged ions in the plasma are attracted, to etch the stacked semiconductor structure 002 in a vertical direction, to form the fin structure 023 having high verticality and flat side walls.

[0044] S102, a second etching process is performed on the fin structures 023, to selectively etch at least a portion of one of the first semiconductor layer 021 and the second semiconductor layer 022.

[0045] A structure formed after step S102 is completed is shown in FIG. 3. In step S102, etching is further performed based on step S101. When the second etching process is performed, the plasma generation chamber 21 and the reaction chamber 10 are separated by a second distance. In the embodiment of the present disclosure, the second distance is greater than the first

distance. This second etching process may be, for example, an isotropic etching process without applying the radio frequency bias to the lower electrode. In an example of FIG. 3, the second semiconductor layer 022 has a high etching selectivity relative to the first semiconductor layer 021, such that the second semiconductor layer 022 is laterally etched. In the example of FIG. 3, merely the portion of the second semiconductor layer 022 is selectively etched. It should be understood by those of ordinary skill in the art that the second semiconductor layer 022 may alternatively be etched wholly.

[0046] As described above, there is a distance between the plasma generation chamber 21 and the reaction chamber 10. After the plasma is generated in the plasma generation chamber 21, the plasma needs to be delivered over a distance before entering the reaction chamber 10. The plasma includes active substances such as high-energy electrons, charged ions, and free radicals (free radicals are neutral and not charged). A lifetime (on the order of microseconds) of the charged ions is shorter than a lifetime (on the order of milliseconds) of the free radicals. Thus, when the plasma moves towards the reaction chamber 10, the longer the moving distance of the plasma towards the reaction chamber is, the more charged ions disappear due to recombination. A higher concentration of free radicals is caused. Correspondingly, the shorter the moving distance of the plasma is, the fewer charged ions disappear due to recombination. A lower concentration of free radicals is caused.

[0047] Thus, according to the method for forming a semiconductor structure disclosed in the embodiments of the present disclosure, a distance between the plasma generation chamber 21 and the reaction chamber 10 is adjusted, a delivery distance of the plasma is adjusted, and finally the concentration of free radicals in the plasma is adjusted. Different concentrations of the free radicals can adapt to different etching processes, and achieve different etching effects. In this case, when the plasma etching processes requiring different concentrations of free radicals are performed on the stacked semiconductor structure 002, merely the distance between the plasma generation chamber 21 and the reaction chamber 10 needs to be adjusted, and different etching processes do not need transfer between different process chambers, such that the problem of low etching throughput is avoided.

[0048] In the embodiments of the present disclosure, the first etching process and the second etching process have different requirements for the concentration of free radicals due to different etching purposes. The first etching process and the second etching process are different etching

processes. For example, the first etching process may be the anisotropic etching process, and the second etching process may be the isotropic etching process.

[0049] The stacked semiconductor structure 002 includes the first semiconductor layer 021 and the second semiconductor layer 022 that are alternately stacked. The first semiconductor layer 021 and the second semiconductor layer 022 may have various types, and may be formed of different materials. For example, the first semiconductor layer 021 may be formed of silicon oxide, and the second semiconductor layer 022 may be formed of silicon nitride. Alternatively, the first semiconductor layer 021 may be formed of Si, and the second semiconductor layer 022 may be formed of SiGe. The second etching process may selectively etch at least the portion of one of the first semiconductor layer 021 and the second semiconductor layer 022. For example, SiGe is selectively removed from the stacked structure of Si and SiGe, to form the GAA-FET. Alternatively, the silicon nitride is selectively removed from the stacked structure of the silicon nitride and the silicon oxide, to form a 3D NAND memory unit.

[0050] In some implementations, the first semiconductor layer 021 is a silicon oxide layer, and the second semiconductor layer 022 is a silicon nitride layer. Process gas used in the second etching process may include fluorine-containing gas and oxygen-containing gas. In some embodiments, a content ratio of fluorine element in the process gas to oxygen element in the process gas may range from 0.1 to 2, and the oxygen-containing gas may be nitrogen oxide, carbon oxide, oxygen gas, etc. The fluorine-containing gas may be at least one of CF_4, C_3F_6, C_4F_8, NF_3, and SF_6. In the process gas, the fluorine-containing gas is main etching gas, and the fluorine element reacts with silicon element, to generate volatile product SiF_4 and implement etching. The oxygen-containing gas is used as auxiliary etching gas, and the oxygen element may inhibit reaction between the fluorine element and the silicon oxide layer, to improve the etching selectivity of the silicon nitride relative to the silicon oxide. In some implementations, the process gas used in the second etching process may not contain hydrogen element. The inventor of the present disclosure has found that during an etching process, presence of the hydrogen element in the process gas results in deposition of nonvolatile polymers on a surface of the silicon oxide layer and a surface of the silicon nitride layer. As a result, further etching is hindered, an etching rate is reduced, and the etching selectivity of the silicon nitride relative to the silicon oxide is reduced to some extent.

[0051] Specific types of the process gas required to perform the first etching process and the second etching process are not limited by the embodiments of the present disclosure. More specifically,

when the second etching process is performed, a pressure of the reaction chamber 10 may range from 0 Torr to 2 Torr, a radio frequency power of an upper electrode of the reaction chamber 10 may range from 50 W to 3000 W, and no radio frequency power of a lower electrode is applied. In a specific embodiment, the process gas used in the second etching process includes CF_4 and O_2. A ratio of CF_4 to O_2 ranges from 0.1 to 1. A scanning electron micrograph obtained after the second etching process is shown in FIG. 4, and the silicon nitride layer is selectively etched relative to the silicon oxide layer.

[0052] As can be seen from FIG. 4, while the silicon nitride is etched, the silicon oxide at an outer side also has a loss, and is cambered-shaped. To further improve the etching selectivity of the silicon nitride layer relative to the silicon oxide layer, in some implementations, the process gas used in the second etching process may also include nitrogen-containing gas. A content ratio of the fluorine element in the process gas to nitrogen element in the process gas may be greater than 1. The inventor of the present disclosure has found that when the auxiliary etching gas includes nitrogen element and oxygen element, the oxygen element and the nitrogen element combine and generate N_xO_y. The substrate can further promote the etching of the silicon nitride layer. Further, the content ratio of the fluorine element to the nitrogen element may be greater than 2 and less than 10.

[0053] In a specific embodiment, the process gases used in the second etching process may include CF_4, O_2, and N_2. A flow rate ratio of CF_4 to O_2 may range from 0.1 to 1, and a flow rate ratio of CF_4 to N_2 may be greater than 0.5. More preferably, a flow rate ratio of CF_4 to N_2 may range from 0.1 to 1. A scanning electron microscope diagram obtained after the second etching process is shown in FIG. 5. It can be clearly seen that a side wall of the etched sunken silicon nitride layer is smooth with desirable etching uniformity. An outline of the silicon oxide layer at an outer side is flat. In a case that the nitrogen-containing gas is added in the process gas used in the second etching process, the etching selectivity of the silicon nitride layer relative to the silicon oxide layer is significantly improved, and an extremely low loss of the silicon oxide layer is ensured while the silicon nitride layer is etched. It should be noted that the ratio between gases in the present disclosure refers to a volume ratio or the flow rate ratio.

[0054] Further, in some implementations, as shown in FIG. 7, the semiconductor process apparatus according to the embodiment of the present disclosure may further include a filter partition plate 40. The method according to the embodiment of the present disclosure may further include:

[0055] the filter partition plate 40 is moved out of the reaction chamber 10 when the first etching process is performed.

[0056] In this case, various ions of the plasma input into the reaction chamber 10 may participate in etching.

[0057] When the second etching process is performed, the filter partition plate 40 is moved into the reaction chamber 10. The filter partition plate 40 is configured to block the charged ions in the generated plasma from passing therethrough. That is, the charged ions are blocked from reaching a surface of the stacked semiconductor structure 002.

[0058] In this case, since the filter partition plate 40 filters the charged ions out of the plasma, uncharged free radicals in the plasma pass through the filter partition plate 40, to participate in the second etching process. Thus, a better isotropic etching effect is achieved. Specifically, the filter partition plate 40 is provided with a through hole 41. Since a lifetime of the charged ions is shorter than a lifetime of the free radicals, the charged ions extend a path when passing through the through hole 41. Thus, the charged ions are annihilated. Since the lifetime of the free radicals is long, the free radicals that collide with a non-through hole area of the filter partition plate 40 may also move continuously to pass through the through hole 41 and participate in the second etching process.

[0059] In the embodiment of the present disclosure, the filter partition plate 40 may alternatively be grounded or a voltage may be applied to the filter partition plate. In this way, the charged ions in the plasma are absorbed to the filter partition plate 40 and recombined, and may not pass through the filter partition plate 40 when the plasma passes through the filter partition plate 40. Thus, the charged ions are better filtered.

[0060] With reference to FIG. 6, the embodiment of the present disclosure discloses a plasma generator 20. The plasma generator 20 disclosed is configured to cooperate with a reaction chamber 10. The plasma generator 20 includes a plasma generation chamber 21 and a plasma delivery tube 22. The plasma generation chamber 21 is configured to generate plasma. One end of the plasma delivery tube 22 communicates with the plasma generation chamber 21, the other end of the plasma delivery tube 22 is configured to communicate with the reaction chamber 10. In a specific operating process, the plasma generation chamber 21 can generate the plasma, and the plasma can be delivered into the reaction chamber 10 through the plasma delivery tube 22 to perform a corresponding etching process.

[0061] In this embodiment of the present disclosure, the plasma delivery tube 22 is adjustable in length, to move the plasma generation chamber 21 close to or away from the reaction chamber 10. In this case, the plasma delivery tube 22 can be adjusted in length. Thus, a distance (for example, the first distance and the second distance) between the plasma generation chamber 21 and the reaction chamber 10 may be changed, and finally a concentration of free radicals delivered into the reaction chamber 10 can be adjusted to adapt to different types of etching processes. It can be seen that the plasma generator 20 disclosed in the embodiment of the present disclosure can adjust the concentration of free radicals, and the reaction chamber 10 can perform different types of etching processes without changing different reaction chambers 10 during the process. Thus, etching throughput is undoubtedly improved advantageously.

[0062] There are various structures adjusting the length of the plasma delivery tube 22, and the specific structure of the plasma delivery tube 22 is not limited by the embodiment of the present disclosure. In some embodiments, the plasma delivery tube 22 may include a bellows and a protective layer such as a quartz coating or an alumina layer coated on an inner wall of the bellows. The bellows may extend or retract to change the length of the plasma delivery tube 22. A first port of the bellows may be hermetically connected to the plasma generation chamber 21, and a second port of the bellows is configured to communicate with the reaction chamber 10. The protective layer is configured to protect the bellows from plasma etching.

[0063] In other embodiments, as shown in FIG. 8, the plasma delivery tube 22 may include at least two delivery tube sections 01, and one of two adjacent delivery tube sections 01 is sleeved around the other delivery tube section and is movable relative to the other delivery tube section. The delivery tube section 01 at the one end of the plasma delivery tube 22 may communicate with the plasma generation chamber 21, and the delivery tube section 01 at the other end of the plasma delivery tube 22 is configured to communicate with the reaction chamber 10. The plasma delivery tube 22 is capable of adaptively extending or retracting through relative sliding between two adjacent tube sections 01. In a specific use process, two adjacent delivery tube sections 01 slide relatively, to change the length of the whole plasma delivery tube 22. When the length of the plasma delivery tube 22 changes, the delivery distance of the plasma is changed, and the concentration of free radicals in the plasma is adjusted.

[0064] In the embodiment where the plasma delivery tube 22 includes at least two delivery tube sections 01, an annular gap 02 may be formed between nested portions of two adjacent delivery tube sections 01, as shown in FIG. 8. During the process, the plasma may escape through the

annular gap 02. Based on this, a length of the annular gap 02 (that is, in a length direction of the plasma delivery tube 22) and a width of the annular gap 02 may be designed. In this way, once the plasma enters the annular gap 02, the plasma can be annihilated in the process of escaping along the annular gap 02, and the plasma can be prevented from escaping out of the plasma delivery tube 22 through the annular gap 02. Those of ordinary skill in the art may design the dimensions (that is, the length and the width) of the annular gap 02 clearly. In this way, the annular gap 02 can be an annihilation gap that enables the plasma to be annihilated although the annular gap 02 enables communication of an internal environment with an external environment of the plasma delivery tube 22. Thus, occurrence of plasma escape can be avoided.

[0065] In a case that the annular gap 02 implements communication of the internal environment with the external environment of the plasma delivery tube 22, the process gas may leak out through the annular gap 02. To avoid adverse effects on the external environment, in some implementations, as shown in FIG. 9, the plasma generator 20 disclosed in the embodiment of the present disclosure may further include a sealing cover 25. The sealing cover 25 hermetically covers an exterior of the plasma delivery tube 22, and the plasma delivery tube 22 passes through the sealing cover 25 and is slidably sealed with the sealing cover 25. It is clear that the sealing cover 25 and the plasma delivery tube 22 can be in sliding fitting, to avoid impact on the extending or retracting of the plasma delivery tube 22.

[0066] The seal member may be not arranged in the annular gap 02. It is clear that to better prevent the plasma and the process gas from escaping, in a further technical solution, as shown in FIG. 10 to FIG. 12, the plasma generator 20 disclosed in the embodiment of the present disclosure may further include a sealing ring 03, and the sealing ring 03 is arranged between two adjacent delivery tube sections 01. Specifically, the sealing ring 03 is arranged in the annular gap 02 formed by two adjacent delivery tube sections 01. Specifically, among a plurality of delivery tube sections 01 constituting the plasma delivery tube 22, the sealing ring 03 may be arranged in each of the annular gaps 02 formed by nesting all two adjacent delivery tube sections 01. The sealing ring 03 can block the annular gap 02, thus better preventing the plasma and the process gas from passing therethrough. The sealing ring 03 may slide along with one of the two adjacent delivery tube sections 01 relative to the other delivery tube section. Thus, the annular gap 02 can be sealed, and adapting to the relative movement between the two adjacent delivery tube sections 01 during the extending or retracting of the plasma delivery tube 22 can be implemented.

[0067] There are many types of sealing rings 03, and the specific types of the sealing ring 03 are not limited by the embodiments of the present disclosure. In some embodiments, the sealing ring 03 may be a magnetic fluid sealing ring. As shown in FIG. 10, the magnetic fluid sealing ring may include a first magnetic ring 031, a second magnetic ring 032, and a magnetic fluid 033, and the first magnetic ring 031 and the second magnetic ring 032 are sleeved around the delivery tube section 01 at the inner side and spaced apart. Magnetic poles of opposite ends of the first magnetic ring 031 and the second magnetic ring 032 are opposite. The magnetic fluid 033 is confined in a space defined by the first magnetic ring 031, the second magnetic ring 032, an outer wall of the delivery tube section 01 at an inner side, and an inner wall of the delivery tube section 01 at an outer side, and is in sealing fit with the inner wall of the delivery tube section 01 at the outer side and the outer wall of the delivery tube section 01 at the inner side, to seal the annular gap 02. In this embodiment, the magnetic fluid sealing ring can play a sealing function, and can further avoid friction with the delivery tube section 01. Thus, particles generated by friction can be prevented from falling into the plasma delivery tube 22, the phenomenon that the particles enter the reaction chamber 10 and pollute the reaction chamber 10 after falling into the plasma delivery tube 22 can be further avoided, and a process effect can be better ensured.

[0068] To prevent the magnetic fluid sealing ring from being interfered by a magnetic field of the external environment or prevent a magnetic field of the magnetic fluid sealing ring from affecting the external environment, further, in some implementations, as shown in FIG. 11, the plasma generator 20 disclosed in the embodiment of the present disclosure may further include a magnetic isolation cover 24. The plasma delivery tube 22 passes through the magnetic isolation cover 24, and the magnetic isolation cover 24 covers a corresponding area of the magnetic fluid sealing ring. In this case, the magnetic isolation cover 24 can isolate the magnetic field, such that magnetic field interference can be avoided. In this case, the magnetic isolation cover 24 may be in sliding fitting with the plasma delivery tube 22, such that the extending or retracting of the plasma delivery tube 22 cannot be affected.

[0069] As described above, there are multiple types of sealing rings 03. Specifically, the sealing ring 03 may alternatively be a common sealing ring. For example, the sealing ring 03 may be an O-ring, a V-ring, etc. With reference to FIG. 12, in some embodiments, the sealing ring may be a Y-ring, the Y-ring has an integrated structure and includes an inner sealing lip 034, an outer sealing lip 035, and a base 036. A first end of the inner sealing lip 034 and a first end of the outer sealing lip

035 are fixed to the base 036, and a second end of the inner sealing lip 034 and a second end of the outer sealing lip 035 may extend in a direction away from the base 036 and away from each other. The outer sealing lip 035 is in sealing fit with the inner wall of the delivery tube section 01 located at the outer side. The inner sealing lip 034 is in sealing fit with the outer wall of the delivery tube section 01 at the inner side. In this case, the inner sealing lip 034 and the outer sealing lip 035 are in sealing fit with two adjacent delivery tube sections 01, to implement sealing. In addition, a recess is formed between the inner sealing lip 034 and the outer sealing lip 035. Thus, the particles generated by friction during the relative sliding between the sealing ring 03 and the delivery tube section 01 can be collected, and the phenomenon that particles may fall into the plasma delivery tube 22 can be avoided.

[0070] In the embodiment of the present disclosure, of two adjacent delivery tube sections 01, the delivery tube section 01 at a higher position may be sleeved outside the delivery tube section 01 at a lower position. In this case, the annular gap 02 formed by two adjacent delivery tube sections 01 is located outside the delivery tube section 01 at the lower position. In this case, even if there are particles generated by friction, the particles easily fall into the annular gap 02 under the action of gravity, instead of easily falling into the delivery tube section 01 at the lower position, and then are delivered to the reaction chamber 10.

[0071] The plasma delivery tube 22 is a tube for delivering the plasma, and then may be made of materials suitable for delivering the plasma. In some embodiments, the plasma delivery tube 22 may be made of a quartz material. In a case where the plasma delivery tube 22 includes a plurality of delivery tube sections 01, the delivery tube sections 01 may be quartz tubes. Alternatively, the delivery tube section 01 may be a metal tube, and an inner wall of the metal tube may be coated with the protective layer such as the alumina layer or the quartz material layer. The protective layer is configured to protect the delivery tube section 01 from being etched by the plasma. The specific material of the delivery tube section 01 is not limited by the embodiments of the present disclosure.

[0072] To make the apparatus more automatic, the plasma generator 20 disclosed in the embodiment of the present disclosure may further include a first driving mechanism 23. A driving end of the first driving mechanism 23 may be connected to the plasma generation chamber 21, a body of the first driving mechanism 23 is configured to be mounted in the reaction chamber 10 or another mounting base component, and the first driving mechanism 23 is configured to drive the plasma generation chamber 21 to move close to or away from the reaction chamber 10. In

this case, the first driving mechanism 23 can drive the plasma generation chamber 21 to move relative to the reaction chamber 10, to move close to or away from the reaction chamber 10. In this process, the plasma delivery tube 22 may extend or retract accordingly, such that the length is adjustable. The first driving mechanism 23 may be a hydraulic telescopic member, a pneumatic telescopic member, a linear motor, etc. The specific type of the first driving mechanism 23 is not limited by the embodiments of the present disclosure.

[0073] Based on the plasma generator according to the embodiment of the present disclosure, as shown in FIG. 6, the embodiments of the present disclosure further disclose a semiconductor process apparatus. The semiconductor process apparatus includes a reaction chamber 10 and the plasma generator 20 in any embodiment described above. A plasma generation chamber 21 communicates with the reaction chamber 10 through a plasma delivery tube 22.

[0074] To ensure etching quality, further isolate the charged ions in the plasma, and improve the effect of isotropic etching, with reference to FIG. 7, the semiconductor process apparatus disclosed in the embodiment of the present disclosure may further include a filter partition plate 40. The reaction chamber 10 has an inner chamber 11, and the filter partition plate 40 is arranged in the inner chamber 11. The filter partition plate 40 may alternatively be grounded or a voltage may be applied to the filter partition plate. The filter partition plate 40 is arranged in the inner chamber 11. The inner chamber 11 is divided into a first subspace 101 and a second subspace 102, and the first subspace 101 is located above the second subspace 102. A bearing seat 30 is arranged in the second subspace 102. A substrate 001 provided with the stacked semiconductor structure 002 shown in FIG. 2 and FIG. 3 is placed on the bearing seat 30, and is located within the second subspace 102.

[0075] The first subspace 101 communicates with the plasma delivery tube 22. The plasma delivered by the plasma delivery tube 22 enters the first subspace 101, and the plasma passes through the filter partition plate 40. Charged ions in the plasma are filtered out by the filter partition plate 40 and do not enter the second subspace 102. Free radicals may pass through the filter partition plate 40 since the free radicals are not charged, and enter the second subspace 102, to participate in etching. In this case, a concentration of free radicals can be ensured as high as possible, to improve the effect of isotropic etching.

[0076] In some embodiments, the filter partition plates 40 are provided with a plurality of through holes 41 spaced apart from one another, to allow the free radicals to pass through. The plurality of through holes 41 may be uniformly or non-uniformly distributed, which is not limited in the

embodiment of the present disclosure. It is clear that the plurality of through holes 41 may be distributed in rows and columns or in a plurality of circles, and the specific distribution mode of the through holes is not limited by the embodiments of the present disclosure. It is clear that the through hole 41 may be a straight hole or a curved hole, which is not limited by the embodiment of the present disclosure. It is clear that in a case that the through hole 41 is a curved hole, the charged ions need a longer path to pass through the curved hole, and can be better filtered, as shown in FIG. 15.

[0077] In the embodiment of the present disclosure, the filter partition plate 40 may be fixed in the inner chamber 11 or may be movably arranged in the inner chamber 11. It is clear that in other etching scenarios, such as an anisotropic etching scenario, the charged ions are needed to etch the stacked semiconductor structure 002 shown in FIG. 2 and FIG. 3. Based on this, as shown in FIG. 13, the semiconductor process apparatus according to the embodiment of the present disclosure may further include a partition plate storage chamber 60 and a second driving mechanism 50. The partition plate storage chamber 60 is located in a side surface of the reaction chamber 10, and communicates with the reaction chamber 10. Specifically, the partition plate storage chamber 60 and the reaction chamber 10 are sequentially distributed in a horizontal plane. The filter partition plate 40 is arranged on a bearing arm of the second driving mechanism 50, and the second driving mechanism 50 is configured to convey the filter partition plate 40 between the partition plate storage chamber 60 and the reaction chamber 10. In the etching scenario where charged ions are needed, the second driving mechanism 50 places the filter partition plate 40 in the partition plate storage chamber 60. In the etching scenario where charged ions are not needed, the second driving mechanism 50 places the filter partition plate 40 in the reaction chamber 10.

[0078] When the filter partition plate 40 is in the reaction chamber 10, as shown in FIG. 13, the filter partition plate 40 divides the inner chamber 11 into the first subspace 101 and the second subspace 102, to block charged ions in the generated plasma from passing therethrough. When the filter partition plate 40 is in the partition plate storage chamber 60, as shown in FIG. 14, the filter partition plate 40 does not divide the inner chamber 11. In this case, the charged ions in the plasma entering the inner chamber 11 from the plasma delivery tube 22 are no longer filtered by the filter partition plate 40.

[0079] The second driving mechanism 50 is arranged on the reaction chamber 10 or the partition plate storage chamber 60. The second driving mechanism 50 can drive the filter partition plate 40 to

be transferred between the reaction chamber 10 and the partition plate storage chamber 60. Such structural design can improve automation of the semiconductor process apparatus. It is clear that the filter partition plate 40 may be movably arranged in the reaction chamber 10 or the partition plate storage chamber 60, and a position may be transferred manually by an operator.

[0080] In the embodiment of the present disclosure, the through hole 41 may be a straight hole or a curved hole, and the specific shape of the through hole 41 is not limited by the embodiments of the present disclosure.

[0081] To improve a filtering effect, at least two filter partition plates 40 in the embodiment of the present disclosure may be provided, and at least two second driving mechanisms 50 may be provided correspondingly. Each filter partition plate 40 is connected to a corresponding second driving mechanism 50, and may be transferred between the partition plate storage chamber 60 and the reaction chamber 10 when driven by the corresponding second driving mechanism 50. In this case, at least two filter partition plates 40 are overlapped or spaced apart. Thus, the plasma input from the first subspace 101 can be filtered several times, and the charged ions in the plasma can be filtered out better. Thus, in a case of the plurality of filter partition plates 40, the charged ions can be further filtered by adjusting the number of filter partition plates 40 in the reaction chamber 10.

[0082] In the embodiment of the present disclosure, each filter partition plate 40 is provided with a plurality of the through holes 41, and the at least two second driving mechanisms 50 adjust positions of corresponding filter partition plates 40 in the reaction chamber 10, to adjust an overlapping area of the through holes 41 of the at least two filter partition plates 40. For example, in a specific adjustment process, each filter partition plate 40 may be driven by the corresponding second driving mechanism 50. In this case, the second driving mechanism 50 enables the through holes 41 of the filter partition plate 40 to be completely overlapped, partially overlapped, or non-overlapped. It is clear that in a case that the through holes are non-overlapped, the plasma enters a gap between one filter partition plate 40 and another adjacent filter partition plate 40 from the through hole 41 of the filter partition plate, and then enters the through hole 41 of another filter partition plate 40. In this embodiment, the second driving mechanism 50 can adjust the positions of the respective corresponding filter partition plates 40, and adjust the overlapping areas of the through holes 41 in the filter partition plates 40. For example, the second driving mechanisms 50 may be rotated by corresponding angles, to adjust

the overlapping degree of the through holes. Alternatively, the second driving mechanism 50 may be rotated by the same angle. For example, each tray bearing the filter partition plate 40 is arranged on the same rotating shaft, and one or more trays extend or retract by a distance in a radial direction, to adjust an overlapping degree of the through holes.

[0083] In this case, when the plasma passes through the filter partition plate 40 and charged ions are absorbed by the filter partition plate 40 and filtered out, free radicals collide with the filter partition plate 40 in different degrees due to the different overlapping areas between the filter partition plates 40. Thus, activity of the free radicals is different. When the free radicals pass through the filter partition plate 40, the more times the free radicals collide, the lower the activity gradually becomes. Too frequent collision leads to the end of lifetimes of some free radicals and annihilation, thus affecting the number of the free radicals passing through the filter partition plate 40. The reactivity and the number of the radicals lead to different etching rates. Specifically, the lower the activity of free radicals is, the less the number is, and the lower the etching rate is. Conversely, the higher the activity of free radicals is, the greater the number is, and the higher the etching rate. The smaller the overlapping area of the through holes 41 is, the more frequently the free radicals collide in the process of passing through the filter partition plate 40. The lower the activity of the free radicals is, the less the number the free radicals is. On the contrary, the less frequently the free radicals collide in the process of passing through the filter partition plate 40, the higher the activity of the free radicals is, and the greater the number of the free radicals is.

[0084] Thus, in this embodiment of the present disclosure, by adjusting the relative position of the filter partition plates 40, the overlapping area of the through holes 41 of the filter partition plate 40 can be adjusted. Further, the activity and the number of the free radicals can be adjusted, and the etching rate can be adjusted.

[0085] Further, the semiconductor process apparatus according to the embodiment of the present disclosure may further include a controller. The controller includes at least one memory and at least one processor. The memory stores a computer program, and the computer program implements the method according to the embodiment when executed by the processor.

[0086] In other embodiments, the semiconductor process apparatus may further include a controller. The controller is configured to adjust a length of the plasma delivery tube 22 according to a process step to be performed by the semiconductor process apparatus. Specifically, the controller may control the first driving mechanism 23, the first driving mechanism 23 drives the

plasma generation chamber 21 to move, and the plasma generation chamber 21 moves close to or away from the reaction chamber 10. In this process, the plasma delivery tube 22 extends or retracts adaptively, to indirectly adjust the length of the plasma delivery tube 22.

[0087] In the embodiment of the present disclosure, the semiconductor process apparatus may further include a controller. The controller is configured to separate the plasma generation chamber 21 from the reaction chamber 10 by a first distance when the semiconductor process apparatus performs an anisotropic etching process, the controller is further configured to separate the plasma generation chamber 21 from the reaction chamber 10 by a second distance when the semiconductor process apparatus performs an isotropic etching process, and the second distance is greater than the first distance. A change in the distance between the plasma generation chamber 21 and the reaction chamber 10 essentially changes the length of the plasma delivery tube 22, and finally changes the delivery distance of the plasma.

[0088] In other embodiments, the semiconductor process apparatus may further includes a controller. The controller is configured to control the second driving mechanism 50 to place the filter partition plate 40 in the partition plate storage chamber 60 when the semiconductor process apparatus performs an anisotropic etching process, and the controller is further configured to control the second driving mechanism 50 to place the filter partition plate 40 in the reaction chamber 10 when the semiconductor process apparatus performs an isotropic etching process.

[0089] The foregoing embodiments of the present disclosure focus on differences among the embodiments, and different optimization features of the embodiments can be combined to form a preferred embodiment as long as they are not contradictory, which is not repeated herein for the sake of conciseness.

[0090] The embodiments of the present disclosure have been described above with reference to the accompanying drawings, but the present disclosure is not limited to the above particular implementations, which are merely illustrative rather than restrictive. Under the teachings of the present disclosure, those of ordinary skill in the art can devise numerous variations without departing from the spirit of the present disclosure and the protection scope of the claims, which should fall within protection scope of the present disclosure.

Claims

1. A method for forming a semiconductor structure, applied to a semiconductor process apparatus, wherein the semiconductor process apparatus comprises a plasma generation chamber and a reaction chamber communicating with each other, and the method comprises:

performing a first etching process on a stacked semiconductor structure, to form a plurality of fin structures spaced apart from one another, wherein the stacked semiconductor structure comprises at least one first semiconductor layer and at least one second semiconductor layer that are alternately stacked; and separating the plasma generation chamber from the reaction chamber by a first distance when the first etching process is performed; and

performing a second etching process on the fin structures, to selectively etch at least a portion of one of the first semiconductor layer and the second semiconductor layer, and separating the plasma generation chamber from the reaction chamber by a second distance when the second etching process is performed, wherein the second distance is greater than the first distance.

2. The method according to claim 1, wherein the semiconductor process apparatus further comprises a filter partition plate, and the method further comprises:

moving the filter partition plate out of the reaction chamber when the first etching process is performed; and

moving the filter partition plate into the reaction chamber when the second etching process is performed, wherein the filter partition plate is configured to block a charged ion in generated plasma from passing therethrough.

3. The method according to claim 1, wherein the first etching process is an anisotropic etching process, and the second etching process is an isotropic etching process.

4. The method according to claim 1, wherein the first semiconductor layer is a silicon oxide layer, the second semiconductor layer is a silicon nitride layer, and the second etching process selectively etches at least a portion of the silicon nitride layer.

5. The method according to claim 4, wherein process gas used in the second etching process comprises fluorine-containing gas and oxygen-containing gas, and a content ratio of fluorine element in the process gas to oxygen element in the process gas ranges from 0.1 to 2.

6. The method according to claim 5, wherein the process gas used in the second etching process further comprises nitrogen-containing gas, and a content ratio of the fluorine element in the process gas to nitrogen element in the process gas is greater than 1.

7. The method according to claim 6, wherein the content ratio of the fluorine element to the nitrogen element is greater than 2 and less than 10.

8. The method according to any one of claims 5 to 7, wherein the process gas used in the second etching process does not comprise hydrogen element; or

when the second etching process is performed, a pressure in the reaction chamber ranges from 0 Torr to 2 Torr; or

when the second etching process is performed, a radio frequency power of an upper electrode of the reaction chamber ranges from 50 W to 3000 W; or

the fluorine-containing gas comprises at least one of CF_4, C_3F_6, C_4F_8, NF_3, and SF_6, the oxygen-containing gas comprises O_2, the process gas further comprises the nitrogen-containing gas, and the nitrogen-containing gas comprises N_2.

9. A plasma generator, configured to cooperate with a reaction chamber, comprising:

a plasma generation chamber configured to generate plasma; and

a plasma delivery tube, wherein the one end of the plasma delivery tube communicates with the plasma generation chamber, the other end of the plasma delivery tube is configured to communicate with the reaction chamber, and the plasma delivery tube is adjustable in length, to move the plasma generation chamber close to or away from the reaction chamber.

10. The plasma generator according to claim 9, wherein the plasma delivery tube comprises at least two delivery tube sections; one of two adjacent delivery tube sections is sleeved around the other delivery tube section and is movable relative to the other delivery tube section, the delivery tube section at the one end of the plasma delivery tube communicates with the plasma generation chamber, and the delivery tube section at the other end of the plasma delivery tube is configured to communicate with the reaction chamber; and the plasma delivery tube is capable of adaptively extending or retracting through relative sliding between two adjacent tube sections.

11. The plasma generator according to claim 10, wherein of two adjacent delivery tube sections, the delivery tube section at a higher position is sleeved around the delivery tube section at a lower position.

12. The plasma generator according to claim 10, further comprising:

a sealing ring, wherein the sealing ring is arranged between two adjacent delivery tube sections, and the sealing ring is slidable along with one of the two adjacent delivery tube sections relative to the other delivery tube section; and/or

a sealing cover, wherein the sealing cover hermetically covers an exterior of the plasma delivery tube, and the plasma delivery tube passes through the sealing cover and is slidably sealed with the sealing cover.

13. The plasma generator according to any one of claims 9 to 12, further comprising a first driving mechanism, a driving end of the first driving mechanism is connected to the plasma generation chamber, and the first driving mechanism is configured to drive the plasma generation chamber to move close to or away from the reaction chamber.

14. A semiconductor process apparatus, comprising:

a reaction chamber; and

the plasma generator according to any one of claims 9 to 13, wherein a plasma generation chamber communicates with the reaction chamber through a plasma delivery tube.

15. The semiconductor process apparatus according to claim 14, further comprising:

a filter partition plate configured to block charged ions in generated plasma from passing therethrough, wherein the filter partition plate is provided with through holes for free radicals in the plasma to pass therethrough;

a partition plate storage chamber located in a side surface of the reaction chamber and communicating with the reaction chamber; and

second driving mechanisms, wherein the filter partition plate is connected to the second driving mechanism, and the second driving mechanism is configured to convey the filter partition plate between the partition plate storage chamber and the reaction chamber.

16. The semiconductor process apparatus according to claim 15, wherein at least two filter partition plates are provided, at least two second driving mechanisms are provided, and the filter partition plate is connected to the corresponding second driving mechanism, and is capable of being transferred between the partition plate storage chamber and the reaction chamber when driven by the corresponding second driving mechanism.

17. The semiconductor process apparatus according to claim 16, wherein the filter partition plates are provided with the plurality of through holes, and the at least two second driving mechanisms adjust positions of the corresponding filter partition plates in the reaction chamber, to adjust an overlapping area of the through holes of the at least two filter partition plates.

18. The semiconductor process apparatus according to claim 15, wherein the through hole is a curved hole or a straight hole.

19. The semiconductor process apparatus according to any one of claims 14 to 18, further comprising a controller, wherein the controller comprises at least one memory and at least one processor, a computer program is stored in the memory, and the computer program implements the method according to any one of claims 1 to 8 when executed by the processor.

20. The semiconductor process apparatus according to any one of claims 14 to 18, further comprising a controller, wherein the controller is configured to adjust a length of the plasma delivery tube according to a process step to be performed by the semiconductor process apparatus.

21. The semiconductor process apparatus according to claim 20, wherein the controller is configured to separate the plasma generation chamber from the reaction chamber by a first distance when the semiconductor process apparatus performs an anisotropic etching process, the controller is further configured to separate the plasma generation chamber from the reaction chamber by a second distance when the semiconductor process apparatus performs an isotropic etching process, and the second distance is greater than the first distance.

22. The semiconductor process apparatus according to any one of claims 15 to 18, further comprising a controller, wherein the controller is configured to control the second driving mechanism to place the filter partition plate in the partition plate storage chamber when the semiconductor process apparatus performs an anisotropic etching process, and the controller is further configured to control the second driving mechanism to place the filter partition plate in the reaction chamber when the semiconductor process apparatus performs an isotropic etching process.