Method of Generating Defects in a Lattice Structure Of a Semiconductor Material

The present invention relates to a method of generating defects in a lattice structure of a semiconductor material during thermal treatment of the material.

During the treatment of semiconductor materials, it is known to thermally treat the semiconductor materials in order to influence the implanting or doping profile of foreign atoms within the semiconductor material.

In this connection, it is known, for example, from W. Lerch et al.; Mat. Res. Soc. Symp. Proc. (1998), volume 525, pages 237-255, and D. F. Downey et al.; Mat. Res. Soc. Symp. Proc. (1998), volume 525, pages 263-271, that the doping profile of boron within a semiconductor material can be influenced by means of an oxygen-containing process gas at constant thermal load. The oxygen-containing process gas effects an oxidation of the Si semiconductor material, which leads to a super saturation of inherent intermediate lattice atoms (Si atoms on intermediate lattice locations), the concentration of which influences the diffusion characteristic of the boron and hence the doping profile.

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In general, with the above-described method it is possible to influence essentially only those doping profiles the foreign atoms of which essentially reach a lattice position via the so-called kick-out mechanism. With this mechanism, the foreign atom that was previously located in an interstitial lattice position reaches a lattice position, whereby a silicon (or in general lattice) atom is displaced from its lattice position in the interstitial lattice position.

It is furthermore known that the doping profile of foreign atoms, which form lattice defects within a semiconductor material, can be changed during a thermal treatment by varying the temperature behavior, whereby high thermal stresses are frequently generated within the semiconductor material in order to achieve desired profiles. However, this inherently contains the risk of damage to the semiconductor due to the thermal treatment. Furthermore, the energy consumption for the thermal treatment is very high.

Furthermore, from the conference report of D.F. Downey, et al.: "Rapid thermal process requirements for the annealing of ultra-shallow junctions" of the Materials Research Society Symposium Proceedings, volume 470, pages 299 to 311 (1 April 1997) XP002101565, there is disclosed a method for the thermal treatment of semiconductor materials in which a process gas atmosphere that is used demonstrates an influence upon the diffusion characteristic of foreign atoms. In particular, the injection of vacancies or interstitials by the annealing in NH_3 or O_2 is mentioned, which influences the diffusion characteristic of boron.

Proceeding from this aforementioned state of the art, it is an object of the present invention to provide a new method which in a simple and economical manner enables a precise control of lattice defects in a semiconductor material.

This object is inventively realized by a method of generating defects in a lattice structure of a semiconductor material during thermal treatment of the material, according to which the defect concentration and/or distribution is controlled as a function of a process gas atmosphere. The above method enables a control of the defect concentration and/or distribution in a lattice structure of a semiconductor material during the thermal treatment thereof at an essentially constant budget (integral of the temperature-time curve). Thus, at a minimal thermal stress, the defect concentration and/or distribution can be controlled as a function of the process gas atmosphere. The defect concentration and/or distribution in turn influences the concentration as well as the diffusion characteristic of foreign atoms within the semiconductor material.

Pursuant to one preferred specific embodiment of the invention, the defects that are generated are vacancies (empty lattice positions). Due to the generation of vacancies, foreign atoms can pass to the lattice positions independently of the above mentioned kick-out mechanism. This is particularly advantageous with large foreign atoms such as arsenic or antimony, which essentially pass to lattice positions of the semiconductor only by filling of vacancies (empty lattice positions).

Pursuant to a further embodiment of the invention, the defects are semiconductor atoms on interstitial or intermediate lattice positions that in turn require another mechanism via which the foreign atoms reach lattice positions.

The defects are advantageously generated in the region of the semiconductor surface with a depth of 0 to approximately 1000 angstroms. The defects are thus also disposed in the region of implanted foreign atoms, as a result of which the distribution and concentration of the foreign atoms are considerably influenced.

Pursuant to a particularly preferred embodiment of the present invention, the composition of the process gas is controlled. By means of the composition of the process gas, which can comprise a mixture of several gases, the defect concentration and/or distribution can be controlled in a particularly straightforward, precise and effective manner. The concentration of the process gas or the process gas component is preferably controlled within an inert gas, which functions as a carrier gas.

The partial pressure of the process gas is preferably controlled.

Pursuant to a particularly preferred embodiment of the invention, the process gas is a nitrogen-containing gas that preferably generates vacancies (empty lattice positions) that considerably influence the doping profile of foreign atoms. In this connection, the process gas is preferably formed of NH_3 or N_2. The nitrogen-containing gas leads to an injection of vacancies via the equilibrium concentration.

The process gas is advantageously provided with no oxygen, especially no free oxygen, which would lead to an oxidation of the semiconductor material and could adversely affect the generation of vacancies (empty lattice positions). O_2 leads to a self interstitial injection via the equilibrium concentration at the process temperature.

Pursuant to an alternative embodiment, in contrast, the process gas is provided with an oxygen-containing component that can lead to an increase of the defect concentration (self interstitials). In this connection, the oxygen-containing component preferably comprises N_2O. Pursuant to a further preferred embodiment of the invention, the temperature behavior of the thermal treatment is controlled in terms of time, and the thermal loading of the semiconductor material is preferably reduced to a minimum.

Furthermore, via the control of the temperature behavior of the thermal treatment in terms of time, the diffusion characteristic of the defects as well as of implanted foreign atoms can be controlled. In this regard, in particular the depth of penetration of the lattice defects, vacancies and/or self-interstitials as well as of the foreign atoms, and thus the spatial distribution thereof within the semiconductor material, can be influenced.

The process gas atmosphere preferably contains argon, which functions as an inert carrier gas.

Pursuant to a preferred embodiment of the invention, an $Si_xO_yN_z$ layer is generated upon the surface of the semiconductor. The thickness of the layer is preferably between 0 and 20 angstroms.

Pursuant to an alternative specific embodiment of the invention, a natural Si_2O layer is preferably removed from the semiconductor surface prior to the thermal treatment in order to be able to generate an oxide-free surface layer. During the thermal treatment an Si_3N_4 layer having a thickness between 0 and approximately 40 angstroms is then preferably generated upon the semiconductor wafer.

Pursuant to a particularly preferred embodiment of the invention, the NH_3 concentration is between approximately 500 to 10,000ppm. The NH_3 concentration is preferably between 2500 to 5,000ppm.

To avoid damage to the wafer, the thermal stress of the semiconductor wafer during the thermal treatment is preferably reduced to a minimum. At this low thermal stress the defects can advantageously be controlled via the process gas atmosphere.

Pursuant to a particularly preferred embodiment of the invention, a concentration and/or distribution of foreign atoms within the semiconductor material is controlled via the concentration and/or distribution of the defects.

The foreign atoms are preferably selected from the following group: boron, phosphorus, As, Sb and In, whereby combinations are also possible.

Pursuant to one embodiment of the invention, the above method is preferably carried out on a doped semiconductor, as a result of which during the thermal treatment at the time the

concentration and/or distribution of the foreign atoms is controlled by the defect concentration and/or distribution, i.e. vacancies and/or self-interstitials.

Pursuant to an alternative embodiment of the present invention, the method is carried out on a non-doped semiconductor. In this way, the semiconductor material can be prepared for a subsequent, selected as targeted doping of the semiconductor material, which has a direct influence upon the following treatment processes of the semiconductor.

The invention will be subsequently explained in greater detail with the aid of preferred specific embodiments of the invention in conjunction with the drawings; the drawings show:

Figure 1 the thickness of an oxy-nitride layer as a function of the NH_3 concentration in an argon atmosphere for an Si wafer that is coated with natural oxide;

Figure 2 schematically the percent of retained dose of foreign atoms in an implanted silicon semiconductor as a function of the NH_3 concentration for a prescribed temperature-time process control in an RTP system, as well as the

correlation of the sheet resistance of the semiconductor as a function of the NH_3 concentration;

Figure 3 the arsenic distribution in a silicon semiconductor material implanted with arsenic for various NH_3 concentrations in an inert gas, as a function of the depth of penetration thereof from the wafer surface, for a prescribed course of the temperature-time control of the thermal treatment;

Figure 4 the sheet resistance of a semiconductor after a thermal treatment with prescribed temperature-time controls, as a function of a NH_3 concentration in argon;

Figure 5 the concentration of arsenic atoms in a silicon semiconductor wafer as a function of the depth of penetration from the substrate surface for various process gas compositions, at the same temperature-time control.

Figure 1 shows the thickness of an oxy-nitride layer as a function of the NH_3 concentration in an argon atmosphere for a silicon semiconductor wafer that is coated with a natural oxide and that is subjected to a thermal treatment of, for example, 1000 °C for 10 seconds. With the thermal treatment that is the basis of Figure 1, argon was used as the

inert carrier gas for the NH_3 component. The thermal treatment includes heating the semiconductor wafer to, for example, 1100 °C for 10 seconds. In so doing, the oxy-nitride layer is built up during the thermal treatment. A nitride layer is formed at lesser or also greater temperatures, and the process time is also not fixed.

As can be seen from Figure 1, after the thermal treatment and at very low NH_3 concentrations (in the range of 0 to 1ppm) or under vacuum conditions (e.g. 10^{-6} torr), the $Si_xO_yN_z$ layer is less than the original, natural oxide layer thickness which, as can be seen from Figure 1, is approximately 13 angstroms. This is attributable to the fact that at these NH_3 concentrations, and as a function of the temperature and possible gas impurities (e.g. O_2), an "etching" of the Si wafer takes place. This need, however, not necessarily occur.

As the NH_3 concentration increases (with the thermal treatment, however, remaining the same), the $Si_xO_yN_z$ layer increases and reaches a maximum of approximately 20 angstroms in pure NH_3. In this connection, it should be noted that the maximum layer thickness is essentially a function of the process control, i.e. of the temperature-time behavior of the process.

For thermal treatments with temperatures below approximately 1000 °C, instead of argon, N_2 can be used as the inert gas since due to the high bonding energy of N_2 below 1000 °C, no or only very little nitriding occurs. At temperatures above 1000 °C, N_2 can also be used as a nitriding component in a process gas, for example together with argon or also NH_3.

With the method that forms the basis of Figure 1, a semiconductor wafer having a natural silicon layer was treated. Alternatively, prior to the treatment, however, the natural silicon oxide can also be removed from the wafer, for example by wet etching, VPC (Vapor Phase Cleaning) or some other known method, so that during the subsequent thermal treatment essentially an Si_3N_4 layer is formed. The Si_3N_4 layer thicknesses that can hereby be achieved are in a range of approximately 0 to 40 angstroms, whereby the layer thickness is a function not only of the concentration and the composition of the nitrogen-containing process gas but also of the temperature-time control of the thermal treatment.

Figure 2 schematically shows the retained dose R_D of foreign atoms in a doped or implanted silicon semiconductor, as well as the sheet resistance R_S as a function of the NH_3 concentration

after a thermal treatment having a prescribed temperature-time process control.

Figure 2 schematically shows the retained dose of foreign atoms R_D (Retained Dose) in the semiconductor (silicon) as a function of the NH_3 concentration (or in general the concentration of a nitrogen-containing process gas component) for a specific temperature-time process control in an RTP system. It is clearly shown that in pure inert gas, a large proportion of the foreign atoms leave the semiconductor by diffusion. This results in a reduction of foreign atoms in the semiconductor. A drawback of this reduction is, an increase of the sheet resistance R_S and under certain circumstances to an unuseability of the overall semiconductor (wafer). By adding one or more nitrogen-containing process gas components, a nitriding occurs on the semiconductor surface that acts as a diffusion barrier for the foreign atoms. As the nitrogen-containing process gas component (or components) increases, the "out diffusion" of the foreign atoms is suppressed.

At higher NH_3 concentrations, the retained dose of foreign atoms increases within the semiconductor wafer and at a concentration of approximately 2500ppm nearly achieves a maximum. This is attributable to the fact that the nitrogen-containing process gas

component effects a nitriding on the semiconductor surface that acts as a diffusion barrier for the foreign atoms.

For example, at a concentration of approximately 2500 to 10,000ppm NH_3 in an inert gas, such as argon, at a temperature-time process of 900 °C to 1150 °C at a duration of, for example, 10 seconds, the "out diffusion" of foreign atoms in an implanted semiconductor wafer (such as with arsenic or antimony) in silicon is nearly entirely suppressed. This is achieved by an $Si_xO_yN_z$ or Si_3N_4 layer having a thickness of 10 to 16 angstroms (see Figure 1). This is a great advantage, especially with very thin pn junctions, since here a "out diffusion" of foreign atoms would lead to undefined pn junctions having undefined high sheet resistances.

Figure 3 shows by way of example the arsenic distribution of silicon semiconductors implanted with arsenic after a prescribed thermal treatment with a constant thermal budget for different NH_3 concentrations in argon, as a function of the depth of penetration from the wafer surface. In this connection, the same starting conditions were present.

The distribution for 0ppm NH_3, i.e. in the case of conducting the process in pure argon or inert gas, exhibits a considerable reduction of foreign atoms in comparison to the other distributions. This is due to the "out diffusion" of the arsenic (foreign) atoms described above in conjunction with Figure 2. Such a reduction of foreign atoms leads to a considerable increase of the sheet resistance, as illustrated in Figure 4, which shows the sheet resistance of the semiconductor as a function of the NH_3 concentration for various temperatures at a process time of 10 seconds. As can be seen from this diagram, the sheet resistance demonstrates a tendency toward small resistances at approximately 10,000ppm NH_3, whereby its absolute value is essentially codetermined from the temperature-time process control. The higher the selected temperature, the smaller the sheet resistance. In this connection, the thermal budget is advantageously minimized, i.e. the wafers are preferably processed at a high temperature in order to keep the process duration as short as possible. Typical process temperatures are between 800 °C and 1200 °C, and typical times are between approximately 0.5s and 360s.

Figure 3 shows that during a treatment of the doped silicon semiconductor in pure argon, the concentration, as well as the depth of penetration of the arsenic, are at their lowest, resulting in a higher R_S

value. As the NH_3 concentration increases, not only does the arsenic concentration increase but the depth of penetration of the arsenic atoms in the semiconductor wafer also increases.

Figure 3 shows that merely by the selection of the concentration of at least one nitrogen-containing process gas component, at a prescribed temperature-time process, the distribution of the foreign atoms and the depth of penetration of the foreign atoms can be adjusted or established. This provides the possibility, at a minimum still tolerable thermal stress of the semiconductor, to set the foreign atom distribution in wide ranges merely via the process gas composition. In this way, the sheet resistance can be varied up to a factor of approximately 10, and in the same way the depth of penetration of the foreign atoms can be varied approximately by a factor of 2.

Figure 4 shows the sheet resistance of a silicon semiconductor wafer implanted with arsenic as a function of the NH_3 in an argon carrier gas for various temperatures of the thermal treatment at a respective process time of 10 seconds. It can be recognized that at higher NH_3 concentrations the sheet resistance is reduced. In this connection, at a concentration greater than approximately 2500 – 5000ppm NH_3 a saturation or lower threshold value of the sheet resistance to small

sheet resistances occurs that cannot be further reduced even if the NH_3 concentrations rise further. The value of the sheet resistance is similarly essentially codetermined from the temperature-time process control. In this connection, one can recognize that at higher temperatures the sheet resistance becomes less. Typical process temperatures are between 800 °C and 1200 °C, and typical steady state times are between 0.5s to 360s. However, to prevent damage to the semiconductor material, the thermal budget should be minimized, in which connection the process times should preferably be under 60 seconds and the temperatures should be between 950 °C and 1150 °C. With very thin pn junctions, so-called flash processes are utilized that are defined by very high temperature increase rates, between 100 °C per second and 500 °C per second, as well as a rapid cooling, between approximately 25 °C per second to 150 °C per second. With these processes, the maximum temperature is frequently maintained for less than five seconds. Often there is even a direct transition from the heating phase into the cooling phase, as a result of which very small thermal budgets can be achieved. However, very high temperatures must be achieved in a very short period of time. At the moment, this can be achieved only with the most modern units, such as the AST 3000 from RTP Systems GmbH, since only with such equipment the power for such high ramp rates is available in a

controlled manner, so that a homogeneous heating of the semiconductor substrate is still possible.

Figure 5 again shows the concentration of arsenic atoms in a doped Si semiconductor wafer as a function of the depth of penetration from the substrate surface for various process gas compositions, with the temperature-time processes remaining constant. With the method that forms the basis of Figure 5, in addition to NH_3 in an argon atmosphere an oxygen-containing component, namely N_2O, was also used.

Figure 5 shows that the addition of N_2O increases the arsenic concentration. This also allows the sheet resistance to be further reduced. Furthermore, Figure 5 shows that the addition of an adequate quantity of N_2O reduces the depth of penetration of the arsenic atoms, which is particularly expedient for thin pn junctions. By adding oxygen-containing gas, the arsenic concentration can be increased by up to approximately twenty times as a function of the concentration of the nitrogen containing gas, whereby the depth of penetration of the foreign atoms is increased only insignificantly, and can if necessary be reduced. In this way, the arsenic distribution can approximate a desired box profile having steeply dropping sides. By

the generation of self-defects (vacancies, self-interstitials) on the surface, prescribed dopant profiles (electrically inactive) can be converted into electrically active dopant profiles accompanied by a minimalization of the depth of penetration and a maximum concentration (so-called box profile).

In general one can say that by means of oxygen and/or nitrogen containing gases, independently of whether the wafer is extrinsically doped (implantation, GPD, diffusion by out diffusion of a layer disposed on a semiconductor into the semiconductor) or is not doped, the defect concentration (self-interstitials/vacancies) can be set as desired, also under the influence of the thermal treatment.

The present invention has been described with the aid of specific exemplary embodiments, without thereby being limited to these special examples. In particular, for carrying out the method it is not necessary that the process gas atmosphere contain an inert carrier gas. Rather, the method could be carried out under low pressure or partial vacuum conditions, whereby the process gas concentration can be regulated via the pressure. Furthermore, the present invention is not limited to the use of NH_3 or N_2O as process gas components. Further examples

for process gas combinations are, for example, NO, H_2O (water vapor). If H_2O is used, the thermal budget can be reduced still further, and there occurs a lower OED (Oxygen Enhanced Diffusion). The method can also be used for non-doped semiconductors in order to prepare them for a subsequent treatment, such as an implantation or a doping step.

A further exemplary application for the inventive method is also the use upon boron and/or phosphorus and/or antimony and/or indium (or universal acceptors/donators) in order to influence the diffusion characteristic (profile) with oxygen-containing and/or nitrogen-containing gases, and to establish, for example, box profiles.

CLAIMS

1. Method of generating defects in a lattice structure of a semiconductor material during thermal treatment of the material, in which the concentration and/or distribution of defects vacancies is controlled as a function of a process gas atmosphere, and an $Si_xO_yN_z$ oxy-nitride layer having a thickness of up to 2nm (20 angstroms) is produced on the surface of the semiconductor.

2. Method of generating defects in a lattice structure of a semiconductor material during thermal treatment of the material, according to which the concentration and/or distribution of defects or vacancies is controlled as a function of a process gas temperature, whereby prior to the thermal treatment a natural SiO_2 layer is removed from the semiconductor surface and an Si_3N_4 layer having a thickness of up to 4nm (40 angstroms) is produced on the semiconductor wafer.

3. Method according to claim 1 or 2, characterized in that the defects are vacancies (empty lattice positions).

4. Method according to one of the preceding claims, characterized in that the defects are semiconductor-

substrate atoms on interstitials (self-interstitials).

5. Method according to one of the preceding claims, characterized in that the composition of the process gas is controlled.

6. Method according to one of the preceding claims, characterized in that the concentration of the process gas or of the process gas components is controlled.

7. Method according to one of the preceding claims, characterized in that the partial pressure of the process gas is controlled.

8. Method according to one of the preceding claims, characterized in that the process gas includes a nitrogen-containing gas.

9. Method according to claim 8, characterized in that the process gas includes NH_3.

10. Method according to claim 8 or 9, characterized in that the process gas includes N_2.

11. Method according to one of the preceding claims, characterized in that the process gas contains no oxygen.

12. Method according to one of the claims 1 to 10, characterized in that the process gas includes an oxygen-containing

component.

13. Method according to claim 12, characterized in that the oxygen-containing component includes N_2O, NO and/or H_2O.

14. Method according to one of the preceding claims, characterized in that the temperature behavior of the thermal treatment is controlled in terms of time.

15. Method according to one of the preceding claims, characterized in that the process gas atmosphere contains argon.

16. Method according to one of the preceding claims, characterized in that prior to the thermal treatment a natural SiO_2 layer is removed from the semiconductor surface.

17. Method according to claim 9, characterized in that the NH_3 concentration is 0 to 10,000ppm.

18. Method according to claim 17, characterized in that the NH_3 concentration is 2500 to 5,000ppm.

19. Method according to one of the preceding claims, characterized in that a distribution of foreign atoms within the semiconductor material is controlled via the distribution of the defects.

20. Method according to claim 19, characterized in that the foreign atoms have at least one element of the following group of boron, phosphorus, As, Sb and In.

21. Method according to one of the preceding claims, characterized in that the method is carried out on a semiconductor doped with foreign atoms.

22. Method according to one of the claims 1 to 19, characterized in that the method is carried out on a semiconductor that is to be doped.

23. Method according to claim 22, characterized in that the semiconductor is doped.

24. Method according to one of the preceding claims, characterized in that the semiconductor is doped by means of gas phase doping implantation, and/or diffusion by out-diffusion into the semiconductor from a layer that contacts the semiconductor.