

1. A system comprising:
a computer bus;
a host computer to execute test flows; and
instrument modules, an instrument module comprising:
5 resources; and
a processing device;

wherein resources operated on by a test flow define a domain;

wherein the host computer is configured to output commands including a sync
command in the test flow to the instrument modules, the sync command for causing the
10 instrument module to provide a status to the computer bus and to pause the processing
device;

wherein statuses from the instrument modules in the domain are aggregated on
the computer bus, and wherein information is distributed to the instrument modules
based on the statuses aggregated; and

15 wherein the processing device is configured to resume executing commands
based on the information.

2. The system of claim 1, wherein the information is distributed after all
instrument modules in the domain have encountered a sync command.

3. The system of claim 1, wherein the host computer is programmed to send the
commands to the instrument modules via a communication bus that is different from the
computer bus.

25 4. The system of claim 1, wherein aggregating the status and distributing the
information are performed independent of the host computer.

5. The system of claim 1, wherein at least some of the commands instruct
resources in the domain to perform operations.

6. The system of claim 1, wherein the instrument module comprises an endpoint device to provide status to the computer bus;

wherein the endpoint device comprises a contributing endpoint device; and

wherein the contributing endpoint device is configured to receive the information
5 from the computer bus and to generate a signal based on the information to trigger operation of one or more of the resources.

7. The system of claim 1, wherein the instrument module comprises an endpoint device; and

10 wherein the endpoint device comprises a non-contributing endpoint device to receive the information from the computer bus and to generate a signal based on the information to trigger operation of one or more of the resources.

8. The system of claim 1, wherein the host computer is programmed to execute
15 a test program that includes multiple, separate instruction flows, the multiple, separate instruction flows including the test flow.

9. The system of claim 8, wherein the instrument module comprises an endpoint device; and

20 wherein the endpoint device is configured to subscribe to one or more of the multiple, separate flows.

10. The system of claim 1, wherein the instrument module comprises an endpoint device; and

25 wherein the endpoint device is configured to generate a signal to provide to resources in the domain.

11. The system of claim 10, wherein the signal is to trigger the resource to perform an action for which the resource has been previously armed.

12. The system of claim 10, wherein an offset may be added to the signal to control signal timing relative to receipt of the information.

13. The system of claim 1, wherein the instrument module comprises an endpoint device; and
5 wherein the endpoint device comprises a transmitter to implement output to the computer bus, and a receiver to implement receiving from the computer bus.

14. The system of claim 1, wherein the status comprises a pass or fail status of
10 a test performed by the processor.

15. The system of claim 1, wherein the status comprises bits that are encoded in time-division-multiple-access fashion onto the computer bus using a periodic frame comprised of multiple bits.
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16. The system of claim 15, wherein the periodic frame is characterized by one or more of headers, trailers, cyclic redundancy checks, or 8b/10b encoding.

17. The system of claim 1, wherein at least some of the bits of the information
20 represent a system time alignment signal to set system clock counters on the instruments to at least one of a specified value or a specified time that is in a payload on the bus.

18. The system of claim 1, wherein the computer bus comprises at least one of a
25 wired-OR bus; point-to-point connections and logic gates; non-contact, wireless or optical signaling; or a combination of one or more of: a wired-OR bus; point-to-point connections and logic gates; non-contact, and wireless or optical signaling.

19. The system of claim 1, wherein the information is received over the
30 computer bus.

20. The system of claim 1, wherein the information is received over a communication bus that is different than the computer bus.

21. The system of claim 1, wherein the sync command in the test flow immediately precedes, in the test flow, a command requiring action or measurement vis-à-vis a device under test by the test flow.

22. The system of claim 1, wherein at least part of the test flow is controllable not to be synchronized.

23. A system comprising:
a computer bus;
instrument modules, an instrument module comprising:
resources; and
a processing device to execute commands from a queue;
wherein the processing device is configured, in response to encountering at least one sync command in the queue, to cause the instrument module to provide a status to the computer bus and to pause the processing device;
wherein statuses from the instrument modules are aggregated on the computer bus, and wherein information is distributed to the instrument modules based on the statuses aggregated; and
wherein the processing device is configured to resume executing commands based on the information.

24. The test system of claim 23, further comprising:
a host computer; and
a communication bus;
wherein the host computer is configured to output the commands to the instrument module via the communication bus.

25. A test system comprising:

instruments for controlling testing, each instrument being controlled by a processing unit, each processing unit being configured to operate on portions of a test program relevant to an instrument that the processing unit controls; and

5 a synchronization mechanism operating with at least some processing units to produce a synchronized sequence of actions, measurements, or measurements and actions at a test instrument interface absent intervention from a centralized controller.

26. The test system of claim 25, wherein the synchronization mechanism is configured to:

10 enable each processing unit to transmit status data indicating whether the processing unit has completed a portion of the test program;
to receive and to aggregate status data across all processing units; and
to transmit one or more aggregated status bits back to all processing units.

15 27. The test system of claim 26, wherein the processing unit is configured to perform operations comprising: when the processing unit has completed a portion of the test program, the processing unit indicates, on a synchronization bus, that the processing unit has completed the portion of the test program and, before proceeding to a next portion of the test program, the processing unit receives the one or more
20 aggregated status bits indicating that all other processing units in the test system have completed portions of the test program.

28. The test system of claim 26, wherein the synchronization mechanism has a defined timing relative to system clocks so that multiple instruments can receive the one
25 or more aggregated status bits and be triggered to perform an action, a measurement, or both an action and a measurement with predictable and repeatable timing alignment among multiple instruments.

29. The test system of claim 26, wherein the synchronization mechanism is
30 configured to support status data comprising multiple status bits that are transmittable by each processing unit, and that can be aggregated to produce the one or more

aggregated status bits, the one or more aggregated status bits being transmitted to all of the processing units.

30. The test system of claim 26, wherein the one or more aggregated status bits
5 are usable to synchronize all instruments in the test system to synchronize a sequence of actions, a sequence of measurements, or a sequence of actions and measurements.

31. The test system of claim 26, wherein the status data comprises at least one
10 bit to transmit pass or fail status of a test program.

32. The test system of claim 26, wherein the status data comprises one or more
status bits that are encoded in time-division-multiple-access fashion onto a serial data
bus using a periodic frame.

33. The test system of claim 32, wherein the periodic frame is characterized by
15 one or more of headers, trailers, cyclic redundancy checks, or 8b/10b encoding.

34. The test system of claim 32, wherein the periodic frame is configurable to
20 transmit information other than the one or more status bits.

35. The test system of claim 26, wherein one or more bit transmitted to the
processing units represent a system time alignment signal to set system clock counters
on the instruments to a specified value.

36. The test system of claim 26, wherein the one or more aggregated status bits
25 comprises a single status bit to synchronize all instruments in the test system to
synchronize a sequence of actions, a sequence of measurements, or a sequence of
actions and measurements.

37. The test system of claim 26, wherein the synchronization mechanism
30 comprises at least one of a wired-OR bus; point-to-point connections and logic gates;

non-contact, wireless or optical signaling; or a combination of one or more of: a wired-OR bus; point-to-point connections and logic gates; non-contact, and wireless or optical signaling.

5 38. The test system of claim 26, wherein at least part of the synchronization mechanism is controllable to be disabled either automatically or manually.

 39. The test system of claim 26, wherein at least part of the synchronization mechanism is controllable to operate on only part of the test program.

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