

CAPACITOR, MANUFACTURING METHOD OF CAPACITOR, AND SEMICONDUCTOR EQUIPMENT

TECHNICAL FIELD

The present disclosure belongs to the field of semiconductor manufacturing, and particularly relates to a capacitor, a manufacturing method thereof, and semiconductor equipment.

BACKGROUND

As one of the most basic components in a circuit, a capacitor plays a crucial role in an entire electronic device. With the development of semiconductor technologies, thin film deposition technology enables nano-scale manufacturing processes of electronic components, and has become a main means for miniaturization and integration of capacitors, and the prepared miniaturized capacitors are generally called micro-capacitors.

At present, an existing micro-capacitor generally includes an upper metal electrode, a lower metal electrode, and a dielectric layer located therebetween. The upper metal electrode includes a W film layer and a TiN film layer sequentially stacked in a direction approaching the lower metal electrode; the lower metal electrode includes a TiN film layer, a W film layer and a TiN film layer sequentially stacked in a direction approaching the upper metal electrode; and the dielectric layer is an Al_2O_3 film layer.

However, the above capacitor has the following problems in practical applications:

a manufacturing process flow of the capacitor is complex due to the multiple layers and complex structure of the capacitor, and requires six deposition processes. Moreover, in the six deposition processes, both the TiN film layer and the W film layer are prepared by a Chemical Vapor Deposition (CVD) equipment, and the dielectric layer is prepared by Atomic Layer Deposition (ALD) equipment; and the CVD equipment and the ALD equipment are independent of each other and cannot be integrated into a vacuum transport system, so a substrate needs to be transported to the independent equipment corresponding to the next process after the process in every independent equipment is completed. Since the transport of the substrate between two pieces of independent equipment makes the substrate exposed to air, the substrate will be exposed to air five times in the entire manufacturing process of the capacitor, which inevitably causes contamination to a surface of the deposited film.

SUMMARY

In order to solve the above technical problems in the prior art, the present disclosure

provides a capacitor, a manufacturing method thereof and semiconductor equipment, which have a simple structure and thus have a simplified manufacturing process and can reduce the number of times that the substrate is exposed to air while being transported, thereby reducing the contamination on a film surface to a certain extent.

In order to solve the above technical problems, the present disclosure provides a capacitor, including an upper electrode, a lower electrode, and a dielectric layer disposed between the upper electrode and the lower electrode, each of the upper electrode and the lower electrode includes a metal layer, and the metal layer of the upper electrode and the metal layer of the lower electrode are made of a same material.

Preferably, a material of the metal layers includes Al, Au, Ti, or Cu.

Preferably, both the upper electrode and the lower electrode are prepared by a Physical Vapor Deposition (PVD) process.

Preferably, both a thickness of the upper electrode and a thickness of the lower electrode are in a range of 50nm to 500nm.

Preferably, both the thickness of the upper electrode and the thickness of the lower electrode are in a range of 100nm to 300nm.

Preferably, the dielectric layer includes an Al_2O_3 layer, a TiO_2 layer, or an HfO_4 layer.

Preferably, a thickness of the dielectric layer is in a range of 5nm to 15nm.

Preferably, the capacitor is a high-density capacitor.

As another technical solution, the present disclosure further provides semiconductor equipment configured to manufacture the capacitor provided by the present disclosure, and the semiconductor equipment includes a PVD chamber, an Atomic Layer Deposition (ALD) chamber and a transport platform;

the PVD chamber is configured to prepare the upper electrode and the lower electrode of the capacitor;

the ALD chamber is configured to prepare the dielectric layer of the capacitor; and

the transport platform is respectively connected with the PVD chamber and the ALD chamber and is configured to transport a substrate.

Preferably, the semiconductor equipment further includes a degas chamber configured to degas and anneal the substrate and connected with the transport platform.

Preferably, the semiconductor equipment further includes a pre-clean chamber configured to remove impurities from a surface of the substrate and connected with the transport platform.

Preferably, the semiconductor equipment includes a plurality of PVD chambers configured to respectively deposit films of a plurality of materials.

Preferably, a target-base distance is greater than 90mm in the PVD chamber.

Preferably, the target-base distance is in a range of 200mm to 410mm.

As another technical solution, the present disclosure further provides a manufacturing method of a capacitor, including steps of:

forming a lower electrode on a surface, on which deposition is to be performed, of a substrate by a PVD process;

forming a dielectric layer on a surface of the lower electrode away from the substrate by an ALD process; and

forming an upper electrode on a surface of the dielectric layer away from the lower electrode by a PVD process;

wherein each of the upper electrode and the lower electrode includes a metal layer, and the metal layer of the upper electrode and the metal layer of the lower electrode are made of a same material.

Preferably, a material of the metal layer includes Al, Au, Ti, or Cu.

Preferably, in the step of forming the upper electrode on the surface of the dielectric layer away from the lower electrode by the PVD process, a process pressure is in a range of 0mTorr to 2mTorr, a sputtering power is in a range of 30kW to 38kW, and a bias power is in a range of 400W to 1000W.

Preferably, the dielectric layer includes an Al_2O_3 layer, a TiO_2 layer, or an HfO_4 layer.

Preferably, in the step of forming the dielectric layer on the surface of the lower electrode away from the substrate by the ALD process, a process temperature is in a range of 300°C to 400°C.

Preferably, before the step of forming the lower electrode on the surface, on which deposition is to be performed, of the substrate by the PVD process, the manufacturing method of a capacitor further includes a degassing process for degassing the surface, on which deposition is to be performed, of the substrate.

Preferably, after the step of forming the upper electrode on the surface of the dielectric layer away from the lower electrode by the PVD process, the manufacturing method of a capacitor further includes an annealing process.

The present disclosure has the beneficial effects as follows.

In the technical solutions of the capacitor, the manufacturing method of a capacitor and the semiconductor equipment provided by the present disclosure, the capacitor includes an upper electrode, a lower electrode and a dielectric layer disposed therebetween, each of the upper electrode and the lower electrode includes a metal layer, and the metal layer of the upper electrode and the metal layer of the lower electrode made of the same material. The capacitor has a simple structure, so that the manufacturing process can be simplified, and the number of

times that the substrate is exposed to air while being transported can be reduced, thereby reducing the contamination on the film surface to a certain extent.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic structural diagram of a capacitor according to a first embodiment of the present disclosure;

Fig. 2a is a schematic structural diagram of semiconductor equipment according to a second embodiment of the present disclosure;

Fig. 2b is a schematic structural diagram of semiconductor equipment according to a modified embodiment of the second embodiment of the present disclosure;

Fig. 3 is a schematic structural diagram of a PVD chamber according to the second embodiment of the present disclosure; and

Fig. 4 is a flowchart of a manufacturing method of a capacitor according to a third embodiment of the present disclosure.

Referential numbers:

20-substrate, 201-trench, 21-upper electrode, 22-lower electrode, 23-dielectric layer, 31, 32-PVD chambers, 33-ALD chamber, 34-transport chamber, 41-sputtering target, 42-base

DETAILED DESCRIPTION

In order to enable those skilled in the art to better understand the technical solutions of the present disclosure, a capacitor, a manufacturing method thereof and semiconductor equipment provided by the present disclosure will be described in detail below with reference to the accompanying drawings.

With reference to Fig. 1, a first embodiment of the present disclosure provides a capacitor, including a substrate 20, an upper electrode 21, a lower electrode 22, and a dielectric layer 23 disposed between the upper electrode 21 and the lower electrode 22, each of the upper electrode 21 and the lower electrode 22 includes a metal layer, and the metal layer of the upper electrode 21 and the metal layer of the lower electrode 22 are made of a same material.

The capacitor has a three-layer structure composed of metal layer/dielectric layer/metal layer, which is similar to a sandwich structure. This structure is simple, thus the manufacturing process can be simplified, and the number of times that the substrate is exposed to air while being transported can be reduced, thereby reducing the contamination on film surfaces to a certain extent.

In the embodiment, the capacitor is a trench capacitor including the substrate 20, and the

substrate 20 may be made of SiO₂ or other materials. Furthermore, the substrate 20 has a trench 201. The upper electrode 21, the dielectric layer 23, and the lower electrode 22 are formed on and cover a surface, on which the trench 201 is located, of the substrate 20, the surface herein including both the surface of the substrate 20 on which the trench 201 is located and an inner surface of the trench 201 that can be exposed to air. After the upper electrode 21, the dielectric layer 23 and the lower electrode 22 are formed, the trench 201 is completely filled.

Optionally, the capacitor is a high-density capacitor. A high-density capacitor refers to a capacitor formed by depositing a metal layer and a dielectric layer in a high-density trench.

Optionally, a material of the metal layers includes Al, Au, Ti, Cu, or the like.

In the embodiment, both the upper electrode 21 and the lower electrode 22 are prepared by a Physical Vapor Deposition (PVD) process. In the prior art, the metal layer is usually prepared by a Chemical Vapor Deposition (CVD) process. By preparing the metal layer by the PVD process, the present application may greatly reduce resistivity of the metal layer and improve compactness and surface flatness of the metal layer. For example, the resistivity of an Al layer prepared by the PVD process is nearly 100 times lower than that of a W layer prepared by the CVD process, and a thickness of the Al layer on an inner sidewall of the trench 201 is much thinner than that of the W layer. In a case where a thickness of the dielectric layer 23 is constant, the thinner the thickness of the metal layer is, the larger the area of the metal layer is, and the larger the capacitance of the capacitor is, thereby improving the electrode characteristics of the capacitor.

Optionally, both a thickness of the upper electrode 21 and a thickness of the lower electrode 22 are in the range of 50nm to 500nm, preferably in the range of 100nm to 300nm. With the thickness within such range, the quality of the capacitor can be guaranteed, and the capacitance of the capacitor can be increased.

Optionally, the dielectric layer 23 includes a film layer having a relatively large dielectric constant, such as an Al₂O₃ layer, a TiO₂ layer, or an HfO₄ layer.

Optionally, a thickness of the dielectric layer 23 is in the range of 5nm to 15nm. In practical applications, the thickness of the dielectric layer 23 may be adjusted according to a breakdown voltage of the capacitor. For example, if the breakdown voltage of the capacitor is 2.5V, the thickness of the dielectric layer 23 may be controlled to be in the range of 9nm to 10nm.

A second embodiment of the present disclosure provides semiconductor equipment which can be used to manufacture a capacitor. The semiconductor equipment includes: a PVD chamber, an ALD chamber and a transport platform. The PVD chamber is configured to prepare an upper electrode and a lower electrode of the capacitor; the ALD chamber is configured to prepare a dielectric layer of the capacitor; and the transport platform is respectively connected with the

PVD chamber and the ALD chamber and is configured to transport a substrate. Specifically, the transport platform mainly includes a transport chamber and a loading/unloading platform, and the transport chamber is a vacuum chamber and is provided therein with a manipulator. The PVD chamber and the ALD chamber surround and communicate with the transport chamber, so as to form a cluster device system.

After being loaded onto the loading platform of the transport platform, a substrate is taken out of the loading platform by the manipulator and is transported to the PVD chamber and the ALD chamber in a process order. After the preparation of the capacitor is finished, the processed substrate is transported out to the unloading platform.

With the semiconductor equipment provided by the embodiment of the present disclosure, the upper and lower electrodes of the capacitor are prepared by adopting the PVD chamber, which, as compared with the case of adopting a CVD process, greatly reduces the resistivity of the upper electrode and the resistivity of the lower electrode and improves the compactness and the surface flatness of the upper and lower electrodes, so that metal electrode performance of the upper and lower electrodes can be improved, thereby further improving performance of the capacitor; meanwhile, the PVD chamber and the ALD chamber are integrated with the same transport platform to form a single cluster device system, which not only lowers equipment cost, but also prevents the substrate from being exposed to air while being transported, thereby further avoiding the contamination on the film surface. In addition, control of industrialization cost is facilitated due to low process costs of the PVD chamber and the ALD chamber.

Specific implementation of the semiconductor equipment provided by the embodiment of the present disclosure will be described in detail below. Specifically, with reference to Fig. 2a, the semiconductor equipment includes a PVD chamber 31, an ALD chamber 33, a degas chamber 35, a pre-clean chamber 36, and a transport platform. The transport platform includes a transport chamber 34, which is a vacuum chamber, and a manipulator is provided in the transport chamber 34. The PVD chamber 31, the ALD chamber 33, the degas chamber 35 and the pre-clean chamber 36 surround and communicate with the transport chamber 34, so as to form a cluster device system.

The PVD chamber 31 is used to perform a PVD process to prepare an upper electrode and a lower electrode of a capacitor. Optionally, each of the upper electrode and the lower electrode includes a metal layer, and the metal layer of the upper electrode and the metal layer of the lower electrode are made of a same material. Optionally, a material of the metal layers includes Al, Au, Ti, Cu, or the like.

With reference to Fig. 3, a target 41 is disposed at the top of the PVD chamber 31, and a base 42 for supporting a to-be-processed workpiece is disposed below the target 41. A sputtering

surface of the sputtering target 41 is disposed opposite to a supporting surface of the base 42, and a distance H between the sputtering surface of the sputtering target 41 and the supporting surface of the base 42 is referred to as a target-base distance. Optionally, the target-base distance is greater than 90mm, so that the chamber can meet the requirement for implementing long-range sputtering, thereby facilitating improvement in film uniformity. Preferably, the target-base distance is in the range of 200mm to 410mm, and within this range, the chamber can meet the requirement for implementing long-range sputtering, and also production efficiency can be ensured.

The ALD chamber 33 is used to perform an ALD process to prepare a dielectric layer of a capacitor. Optionally, the dielectric layer includes a film layer having a relatively large dielectric constant, such as an Al_2O_3 layer, a TiO_2 layer, an HfO_4 layer, or the like.

The degas chamber 35 is used to degas and anneal the to-be-processed workpiece.

The pre-clean chamber 36 is used to clean a surface of the to-be processed workpiece to remove impurities from the surface of the workpiece.

It should be noted that one PVD chamber 31 is provided in this embodiment, but the present disclosure is not limited thereto. In practical applications, a plurality of PVD chambers 31 may be disposed around the transport chamber 34 to form a cluster device system together with the other chambers.

As shown in Fig. 2a, in a case where the semiconductor equipment is provided with only one PVD chamber 31, a substrate is transported into the PVD chamber 31 to prepare a lower electrode, then is transported into the ALD chamber 33 to prepare a dielectric layer, and finally is transported into the PVD chamber 31 again to prepare an upper electrode.

As shown in Fig. 2b, in a case where the semiconductor equipment is provided with two PVD chambers (31, 32), a substrate is transported into a first PVD chamber 31 to prepare a lower electrode, then is transported into the ALD chamber 33 to prepare a dielectric layer, and finally is transported into a second PVD chamber 32 to prepare an upper electrode. Compared to the above semiconductor equipment provided with only one PVD chamber 31, the semiconductor equipment provided with two PVD chambers makes it unnecessary to return the substrate to the PVD chamber, which is beneficial to line production, thereby improving processing efficiency of the semiconductor equipment.

A third embodiment of the present disclosure provides a manufacturing method of a capacitor, including steps of:

forming a lower electrode on a surface, on which deposition is to be performed, of a substrate by a PVD process;

forming a dielectric layer on a surface of the lower electrode away from the substrate by an

ALD process; and

forming an upper electrode on a surface of the dielectric layer away from the lower electrode by a PVD process.

By preparing the upper and lower electrodes by the PVD processes, the resistivity of the upper electrode and the resistivity of the lower electrode are greatly reduced, and the compactness and the surface flatness of the upper and lower electrodes are improved, so that the metal electrode performance of the upper and lower electrodes can be improved, thereby further improving the performance of the capacitor.

With reference to Fig. 1 to Fig. 4, the manufacturing method of a capacitor provided by the third embodiment of the present disclosure adopt the semiconductor equipment provided by the second embodiment of the present disclosure to manufacture the capacitor shown in Fig. 1. Specifically, the manufacturing method of a capacitor includes the following steps S1 to S5.

step S1 includes: performing a degassing process, that is, degassing the surface of the substrate 20 on which deposition is to be performed.

In step S1, the substrate 20 is first transported into the degas chamber 35 for degassing so as to remove the impurities from the surface of the substrate 20. During the degassing process, the pressure of the degas chamber 35 is controlled to be 0 Torr-10Torr, and the temperature of the degas chamber 35 is controlled to be 0°C -400°C. Preferably, the pressure of the degas chamber 35 is controlled to be 1Torr-7Torr, and the temperature of the degas chamber 35 is controlled to be 300°C -400°C.

The substrate 20 may be made of SiO₂ or other materials and has the trench 201. The surface of the substrate 20 on which deposition is to be performed includes both the surface of the substrate 20 where the trench 201 is located and the inner surface of the trench 201 that can be exposed to air.

Step S2 includes: forming the lower electrode 22 on the surface of the substrate 20 on which deposition is to be performed by a PVD process.

Step S3 includes: forming the dielectric layer 23 on the surface of the lower electrode 22 away from the substrate 20 by an ALD process.

Step S4 includes: forming the upper electrode 21 on the surface of the dielectric layer 23 away from the lower electrode 22 by a PVD process.

In steps S2 to S4, the upper electrode 21, the dielectric layer 23 and the lower electrode 22 cover the surface of the substrate 20 on which deposition is to be performed, and completely fill the trench 201.

In steps S2 and S4, each of the upper electrode 21 and the lower electrode 22 includes a metal layer, and the metal layer of the upper electrode 21 and the metal layer of the lower

electrode 22 are made of the same material. Thus, the capacitor has a three-layer structure composed of metal layer/dielectric layer/metal layer, which is similar to a sandwich structure. This structure is simple, thus the manufacturing process can be simplified, and the number of times that the substrate is exposed to air while being transported can be reduced, thereby reducing the contamination on the film surfaces to a certain extent.

Optionally, a material of the metal layers includes Al, Au, Ti, Cu, or the like.

Optionally, the dielectric layer 23 includes a film layer having a relatively large dielectric constant, such as an Al_2O_3 layer, a TiO_2 layer, an HfO_4 layer, or the like.

In the embodiment, the target 41 is disposed at the top of the PVD chamber 31 that is used to prepare the upper electrode 21 and the lower electrode 22, and the base 42 for supporting the to-be-processed workpiece is disposed below the target 41. The target-base distance is greater than 90mm, preferably in the range of 200mm to 410mm. During the PVD process, a process gas is introduced into the PVD chamber 31, and the pressure of the chamber ranges from 0mTorr to 5mTorr, preferably from 0mTorr to 2mTorr. The sputtering power applied to the target 41 ranges from 0kW to 40kW, preferably from 30kW to 38kW. The bias power applied to the base ranges from 0W to 2000W, preferably from 400W to 1000W.

Optionally, both the thickness of the upper electrode 21 and the thickness of the lower electrode 22 are in the range of 50nm to 500nm, preferably 100nm to 300nm. With the thickness in such range, the quality of the capacitor can be guaranteed, and the capacitance of the capacitor can be increased.

Optionally, the thickness of the dielectric layer 23 is in the range of 5nm to 15nm. In practical applications, the thickness of the dielectric layer 23 may be adjusted according to a breakdown voltage of the capacitor. For example, if the breakdown voltage of the capacitor is 2.5V, the thickness of the dielectric layer 23 may be controlled to be in the range of 9nm to 10nm.

In step S3, when performing the ALD process, a temperature is controlled to be 150°C - 400°C, preferably 300°C - 400°C, so that an annealing process can be performed on the lower electrode 22 while preparing the dielectric layer 23, thereby optimizing crystallization of the lower electrode 22 and improving performance of the lower electrode 22.

Step S5 includes: performing an annealing process on the upper electrode 21, the dielectric layer 23 and the lower electrode 22.

Since stress is easily generated in the processes of preparing the upper electrode 21, the lower electrode 22 and the dielectric layer 23, an annealing process needs to be performed on the upper electrode 21, the lower electrode 22 and the dielectric layer 23 after the preparing processes are completed. The annealing process may be performed in the degas chamber 35, or in another chamber having an annealing function. When performing the annealing process, the

pressure of the chamber is controlled to be 0-10Torr, preferably 1Torr-7Torr, and the temperature is controlled to be 0°C -400°C, preferably 300°C -400°C

In the embodiment, if the depth-to-width ratio of the trench 201 is 4:1, when preparing the upper electrode 21 and the lower electrode 22, the target-base distance is preferably 290mm, the pressure in the chamber is preferably 0.1mTorr,-1mTorr, the sputtering power applied to the target 41 is preferably 30 kW-35kW, the bias power applied to the base 42 is preferably 500W-800W, and the thickness of the obtained upper electrode 21 and the thickness of the obtained lower electrode 22 are both 100nm-200nm.

It should be understood that the above embodiments are merely exemplary embodiments employed to illustrate the principles of the present disclosure, and the present disclosure is not limited thereto. Various modifications and improvements can be made by those skilled in the art without departing from the spirit and essence of the present disclosure, and are considered to fall within the scope of the present disclosure.

What is claimed is:

1. A capacitor, characterized by comprising an upper electrode, a lower electrode and a dielectric layer disposed between the upper electrode and the lower electrode, characterized in that, each of the upper electrode and the lower electrode comprises a metal layer, and the metal layer of the upper electrode and the metal layer of the lower electrode are made of a same material.

2. The capacitor according to claim 1, characterized in that, a material of the metal layers comprises Al, Au, Ti, or Cu.

3. The capacitor according to claim 1 or 2, characterized in that, both the upper electrode and the lower electrode are prepared by a physical vapor deposition process.

4. The capacitor according to claim 2, characterized in that, both a thickness of the upper electrode and a thickness of the lower electrode is in a range of 50nm to 500nm.

5. The capacitor according to claim 4, characterized in that, both the thickness of the upper electrode and the thickness of the lower electrode are in a range of 100nm to 300nm.

6. The capacitor according to claim 1, characterized in that, the dielectric layer comprises an Al_2O_3 layer, a TiO_2 layer, or an HfO_4 layer.

7. The capacitor according to claim 6, characterized in that, a thickness of the dielectric layer is in a range of 5nm to 15nm.

8. The capacitor according to claim 1, characterized in that, the capacitor is a high-density capacitor.

9. Semiconductor equipment, characterized in that, the semiconductor equipment is configured to manufacture the capacitor according to any one of claims 1 to 8, and comprises: a physical vapor deposition chamber, an atomic layer deposition chamber and a transport platform; the physical vapor deposition chamber is configured to prepare the upper electrode and the lower electrode of the capacitor;

the atomic layer deposition chamber is configured to prepare the dielectric layer of the capacitor; and

the transport platform is respectively connected with the physical vapor deposition chamber and the atomic layer deposition chamber and is configured to transport a substrate.

10. The semiconductor equipment according to claim 9, characterized by further comprising a degas chamber configured to degas and anneal the substrate and connected with the transport platform.

11. The semiconductor equipment according to claim 9, characterized by further comprising a pre-clean chamber configured to remove impurities from a surface of the substrate and connected with the transport platform.

12. The semiconductor equipment according to claim 9, characterized in that, the semiconductor equipment comprises a plurality of physical vapor deposition chambers configured to deposit thin films of a plurality of materials, respectively.

13. The semiconductor equipment according to claim 9, characterized in that, a target-base distance is greater than 90mm in the physical vapor deposition chamber.

14. The semiconductor equipment according to claim 13, characterized in that, the target-base distance is in a range of 200mm to 410mm.

15. A manufacturing method of a capacitor, characterized by comprising:
forming a lower electrode on a surface, on which deposition is to be performed, of a substrate by a physical vapor deposition process;
forming a dielectric layer on a surface of the lower electrode away from the substrate by an atomic layer deposition process; and
forming an upper electrode on a surface of the dielectric layer away from the lower electrode by a physical vapor deposition process;
wherein each of the upper electrode and the lower electrode comprises a metal layer, and the metal layer of the upper electrode and the metal layer of the lower electrode are made of a same material.

16. The manufacturing method of a capacitor according to claim 15, characterized in that, a material of the metal layers comprises Al, Au, Ti, or Cu.

17. The manufacturing method of a capacitor according to claim 15, characterized in that, in the step of forming the upper electrode on the surface of the dielectric layer away from the lower electrode by the physical vapor deposition process, a process pressure is in a range of 0mTorr to 2mTorr, a sputtering power is in a range of 30kW to 38kW, and a bias power is in a range of 400W to 1000W.

18. The manufacturing method of a capacitor according to claim 15, characterized in that, the dielectric layer comprises an Al_2O_3 layer, a TiO_2 layer, or an HfO_4 layer.

19. The manufacturing method of a capacitor according to claim 15, characterized in that, a process temperature is in a range of 300°C to 400°C in the step of forming the dielectric layer on the surface of the lower electrode away from the substrate by the atomic layer deposition process.

20. The manufacturing method of a capacitor according to claim 15, characterized by further comprising a degassing process for degassing the surface, on which deposition is to performed, of the substrate before the step of forming the lower electrode on the surface, on which deposition is to performed, of the substrate by the physical vapor deposition process.

21. The manufacturing method of a capacitor according to claim 15, characterized by further comprising an annealing process after the step of forming the upper electrode on the surface of the dielectric layer away from the lower electrode by the physical vapor deposition process.