

CIRCUIT ARRANGEMENT AND METHOD OF OPERATING THE SAME

Cross-reference to Related Application

[0001] This application claims the benefit of priority of United States patent application No. 61/892,689, filed 18 October 2013, the content of it being hereby incorporated by reference in its entirety for all purposes.

Technical Field

[0002] Various aspects of this disclosure relate to circuit arrangements and methods of operating the same.

Background

[0003] Capacitive sensors play an important role in many industrial and commercial instrumentation applications such as displacement, acceleration, pressure, and humidity measurement. The electronic interface circuit suitable for capacitive sensing plays the most important role in determining the overall system performance such as the power consumption, sensing resolution, system noise level as well as linearity and distortion. A high-quality interface circuit ensures good sensor system performance.

[0004] FIG. 1 is a schematic 100 illustrating a common front-end Switched-Capacitor Capacitance-to-Voltage-Converter (SC-CVC) readout interface including a simple operational amplifier (OA) 102 with appropriate switches 104a, 104b connecting the sensing reference voltage V_{ref} to the dedicated reference capacitor C_R 106a as well as the sensing capacitor C_X 106b. This is under the control of the two-phased non-overlapping clock signals Φ_1 and Φ_2 for charge sampling and charge transfer to the feedback capacitor C_F 110. Switches 108a, 108b are arranged between the capacitors 106a, 106b and ground. The feedback capacitor 110 is coupled between the output and inverting input of the amplifier 102. A reset switch 112 is coupled in parallel with the

feedback capacitor. The output of amplifier 102 is also coupled to a sample and hold (S/H) circuit 114.

[0005] However, this single-ended SC-CVC circuitry suffers from several disadvantages. The fundamental precision and thermal stability of this SC-CVC circuit are affected by the switch errors arising from charge-injection and clock feed-through effects. Several circuit techniques have been proposed to reduce these non-ideal effects. Although using the dummy switch compensation can help reduce some of the channel charge injection, it is not effectively cancelled out. Differential circuit structure provides a good solution. However, the differential method requires a more complex circuit design and it often imposes more stringent requirement on device matching for some critical component pairs, resulting in a higher cost as well as higher power consumption. Another circuit architecture to relax the above direct current (DC) offset problems for the SC-CVC circuit is the well-known Offset-Canceled Cascade Capacitance-to-Voltage Converter (OCC-CVC). Unfortunately, the OCC-CVC scheme cancels only the first stage errors consisting of DC offset, flicker noise and charge injection of switches but not those of the second stage. The relative errors originated in the second stage with respect to the first stage sensor interface can be minimized only if the gain of the first stage is very high and the gain of the second stage should be kept as small as possible in a bid to reduce the amplification of errors that greatly influence the stability of sensor signal in terms of DC offset, thermal drift or aging drift. This imposes significant challenge in the context of design tradeoff among stability, power consumption and resolution when the readout circuit is applied to capacitive sensors which may have very large inherent parasitic capacitances such as the microelectromechanical systems (MEMS)-based capacitive sensing accelerometers.

Summary

[0006] In various embodiments, a circuit arrangement may be provided. The circuit arrangement may include a charge sensing stage. The circuit arrangement may also

include an input stage coupled to the charge sensing stage. The input stage may include an input switching mechanism configured to provide a first charge signal to the charge sensing stage when a first control signal, the first control signal including a first pulse with a rising edge and a falling edge, is applied to the input switching mechanism and to provide a second charge signal to the charge sensing stage when a second control signal, the second control signal including a second pulse with a rising edge and a falling edge, is applied to the input switching mechanism. The circuit arrangement may further include an output stage coupled to the charge sensing stage. The output stage may include a first output node. The output stage may further include a second output node. The output stage may additionally include an output switching mechanism configured to couple the charge sensing stage to the first output node when a third control signal is applied to the output switching mechanism, the third control signal including a third pulse with a rising edge behind the rising edge of the first control signal and a falling edge before the falling edge of the first control signal; and to couple the charge sensing stage to the second output node when a fourth control signal is applied to the output switching mechanism, the fourth control signal including a fourth pulse with a rising edge behind the rising edge of the second control signal and a falling edge before the falling edge of the second control signal.

[0007] In various embodiments, a method of operating a circuit arrangement may be provided. The method may include providing a first control signal, the first control signal including a pulse with a rising edge and a falling edge, to an input switching mechanism of an input stage so that the input switching mechanism provides a first charge signal to a charge sensing stage coupled to the input stage. The method may also include providing a second control signal, the second control signal including a pulse with a rising edge and a falling edge, to the input switching mechanism of the input stage so that the input switching mechanism provides a second charge signal to the charge sensing stage. The method may further include providing a third control signal, the third control signal including a third pulse with a rising edge behind the

rising pulse of the first control signal and a falling edge before the falling edge of the first control signal, to an output switching mechanism of an output stage so that the charge sensing stage is coupled to a first output node of the output stage. The method may additionally include providing a fourth control signal, the fourth control signal including a fourth pulse with a rising edge behind the rising pulse of the second control signal and a falling edge before the falling edge of the second control signal, to the output switching mechanism of the output stage so that the charge sensing stage is coupled to a second output node of the output stage.

Brief description of the drawings

[0008] The invention will be better understood with reference to the detailed description when considered in conjunction with the non-limiting examples and the accompanying drawings, in which:

FIG. 1 is a schematic illustrating a common front-end Switched-Capacitor Capacitance-to-Voltage-Converter (SC-CVC) readout interface including a simple operational amplifier (OA) with appropriate switches connecting the sensing reference voltage V_{ref} to the dedicated reference capacitor C_R as well as the sensing capacitor C_X .

FIG. 2 is a schematic showing a circuit arrangement according to various embodiments.

FIG. 3A is a schematic showing a circuit arrangement according to various embodiments.

FIG. 3B is a graph illustrating the control signals (T_1 , T_2 , T_{1s} , T_{2s}) and reset signal (Φ_1) applied to the circuit arrangement according to various embodiments.

FIG. 3C is a schematic of the circuit arrangement shown in FIG. 3A according to various embodiments with error sources.

FIG. 3D is a schematic of the circuit arrangement shown in FIG. 3A according to various embodiments with parasitic capacitance.

FIG. 4A is a schematic showing a circuit arrangement according to various embodiments.

FIG. 4B is a graph illustrating the control signals (T_1 , T_2 , T_{1s} , T_{2s}) and reset signal (Φ_1) applied to the circuit arrangement according to various embodiments.

FIG. 4C is an illustration showing the operation of a circuit arrangement according to various embodiments.

FIG. 5A is a schematic illustrating a circuit arrangement according to various embodiments.

FIG. 5B is a graph illustrating the control signals (T_1 , T_2 , T_{1s} , T_{2s} , P_1 , P_2 , P_{1s} , P_{2s} , Q_1 , Q_2 , Q_{1s} , Q_{2s}), enable signals (T_{en} , P_{en} , Q_{en}) and reset signal (Φ_1) applied to the circuit arrangement according to various embodiments.

FIG. 5C is an illustration showing the operation of a circuit arrangement according to various embodiments.

FIG. 6A is a schematic illustrating a circuit arrangement according to various embodiments.

FIG. 6B is a graph illustrating the control signals (T_1 , T_2 , T_{1s} , T_{2s} , P_1 , P_2 , P_{1s} , P_{2s} , Q_1 , Q_2 , Q_{1s} , Q_{2s}), enable signals (T_{en} , P_{en} , Q_{en}) and reset signal (Φ_1) applied to the circuit arrangement according to various embodiments.

FIG. 6C is an illustration showing the operation of a circuit arrangement according to various embodiments.

FIG. 7 is a schematic illustrating a method of operating a circuit arrangement.

Detailed description

[0009] The following detailed description refers to the accompanying drawings that show, by way of illustration, specific details and embodiments in which the invention may be practiced.

[0010] The word "exemplary" is used herein to mean "serving as an example, instance, or illustration". Any embodiment or design described herein as "exemplary"

is not necessarily to be construed as preferred or advantageous over other embodiments or designs.

[0011] In various embodiments, a "circuit" may be understood as any kind of a logic implementing entity, which may be special purpose circuitry or a processor executing software stored in a memory, firmware, or any combination thereof. Thus, in various embodiments, a "circuit" may be a hard-wired logic circuit or a programmable logic circuit such as a programmable processor, e.g. a microprocessor (e.g. a Complex Instruction Set Computer (CISC) processor or a Reduced Instruction Set Computer (RISC) processor). A "circuit" may also be a processor executing software, e.g. any kind of computer program, e.g. a computer program using a virtual machine code such as e.g. Java. Any other kind of implementation of the respective functions which will be described in more detail below may also be understood as a "circuit" in accordance with various alternative embodiments.

[0012] FIG. 2 is a schematic 200 showing a circuit arrangement according to various embodiments. The circuit arrangement may include a charge sensing stage 202. The circuit arrangement may also include an input stage 204 coupled to the charge sensing stage 202. The input stage 204 may include an input switching mechanism configured to provide a first charge signal to the charge sensing stage when a first control signal, the first control signal including a first pulse with a rising edge and a falling edge, is applied to the input switching mechanism and to provide a second charge signal to the charge sensing stage when a second control signal, the second control signal including a second pulse with a rising edge and a falling edge, is applied to the input switching mechanism. The circuit arrangement may further include an output stage 206 coupled to the charge sensing stage 204. The output stage 206 may include a first output node. The output stage may further include a second output node. The output stage may additionally include an output switching mechanism configured to couple the charge sensing stage to the first output node when a third control signal is applied to the output switching mechanism, the third control signal including a third pulse with a

rising edge behind the rising edge of the first control signal and a falling edge before the falling edge of the first control signal; and to couple the charge sensing stage to the second output node when a fourth control signal is applied to the output switching mechanism, the fourth control signal including a fourth pulse with a rising edge behind the rising edge of the second control signal and a falling edge before the falling edge of the second control signal.

[0013] In other words, the circuit arrangement may include a charge sensing stage 202 coupled between the input stage 204 and the output stage 206. The input stage 204 may include an input switching mechanism. When a first control signal having a first pulse, the first pulse including a rising edge and a falling edge, is applied to the input switching mechanism, a first charge signal may be provided to the charge sensing stage 202. Correspondingly, when a second control signal having a second pulse, the second pulse including a rising edge and a falling edge, is applied to the input switching mechanism, a second charge signal may be provided to the charge sensing stage 202. The output stage 206 may include a first output node and a second output node. The output stage 206 may also include an output switching mechanism configured to switch between coupling the first output node to the charge sensing stage 202 and coupling the second output node to the charge sensing stage 202. The first output node may be coupled to the charge sensing stage 202 when a third control signal having a third pulse is applied to the output switching mechanism. The second output node may be coupled to the charge sensing stage 202 when a fourth control signal having a fourth pulse is applied to the output switching mechanism. The third pulse may overlap with the first pulse and may be contained within the duration of the first pulse. The duration of the third pulse may be shorter or substantially equal to the duration of the first pulse. The fourth pulse may overlap with the second pulse and may be contained within the duration of the second pulse. The duration of the fourth pulse may be shorter or substantially equal to the duration of the second pulse.

[0014] Coupling a first circuit element to a second circuit element may include electrically connecting the first circuit element to the second circuit element. Activating a switch may include turning on the switch through application of an external voltage or an external current or an external force so that an internal current may flow from a first terminal to a second terminal of the switch or switching mechanism. In the absence of the external voltage or the external current or the external force, no internal current or an insubstantial current may flow between the first terminal and the second terminal.

[0015] The first charge signal may also be referred to as a first amount of charge and the second charge signal may be referred to as a second amount of charge. The first amount of charge may vary over a period of time. The second amount of charge may also vary over a period of time. The first amount of charge may be substantially equal to the negative of the second amount of charge. In other words, the absolute magnitude of the first charge signal may be substantially equal to the absolute magnitude of the second charge signal while the sign is opposite.

[0016] In various embodiments, the third pulse may have the same duration as the first pulse. In various other embodiments, the third pulse may be included or contained within the first pulse. In various embodiments, the fourth pulse may have the same duration as the second pulse. In various other embodiments, the fourth pulse may be included or contained within the second pulse.

[0017] The first pulse may be or may represent a logical high of the first control signal. The second pulse may be or may represent a logical high of the second control signal. Further, the third pulse may be or may represent a logical high of the third control signal. The fourth pulse may be or may represent a logical high of the fourth control signal.

[0018] The rising edge of the third pulse may occur later than the rising edge of the first pulse. The falling edge of the third pulse may occur earlier than the falling edge of the first pulse. The rising edge of the fourth pulse may occur later than the rising

edge of the second pulse. The falling edge of the fourth pulse may occur earlier than the falling edge of the second pulse.

[0019] In other words, the third pulse may occur when there is a first pulse. The third pulse may be at logic high only when the first pulse is at logic high (the third pulse may also be at logic low when the first pulse is at logic high). It may not be possible for the third pulse to be at logic high when the first pulse is at logic low. The fourth pulse may occur when there is a second pulse. The fourth pulse may be at logic high only when the second pulse is at logic high (the fourth pulse may also be at logic low when the second pulse is at logic high). It may not be possible for the fourth pulse to be at logic high when the second pulse is at logic low.

[0020] FIG. 2 shows an exemplary implementation of the charge sensing stage 202 as an illustration. Other implementations of the charge sensing stage 202 may also be possible. In various embodiments, the charge sensing stage 202 may include an amplifier 210 having a first input, a second input and an output. The charge sensing stage 202 may also include a feedback capacitor 212 having a first end coupled to the first input of the amplifier 210 and a second end coupled to the output of the amplifier 210.

[0021] The charge sensing stage 202 may also include a reset switch mechanism 214 coupled in parallel to the feedback capacitor 212. The reset switch mechanism 214 may have a first end coupled to the first input of the amplifier 210 and a second end coupled to the output of the amplifier 210.

[0022] The first input of the amplifier 210 may be coupled to the input stage 204. The second input of the amplifier 210 may be configured to be coupled to a reference voltage such as ground. The output of the amplifier 210 may be coupled to the output stage 206.

[0023] FIG. 2 shows an exemplary implementation of the input stage 204 as an illustration. Other implementations of the input stage 204 may also be possible. The input stage 204 may include a first input capacitor 216a and a second input capacitor

216b connected in series. The first input capacitor 216a may be a sensing capacitor. The second input capacitor 216b may also be a sensing capacitor. In other words, the first input capacitor 216a and the second input capacitor 216b may be configured to detect changes in the external environment. When there are changes in the external environment, the capacitance of the first input capacitor 216a and/or second input capacitor 216b may be varied. A node between the first input capacitor 216a and the second input capacitor 216b may be coupled to the charge sensing stage 202. A total charge proportional to the capacitance change and the reference voltage may be transferred to the feedback capacitor 212 of the charge sensing stage 202. As a result, the variation of the capacitance is converted to an output voltage after the charge sensing stage 202. The circuit arrangement may be able to detect changes in the external environment through the first input capacitor 216a and/or second input capacitor 216b.

[0024] The input switching mechanism configured to provide the first charge signal to the charge sensing stage may include the input switching mechanism configured to apply the first capacitor 216a and the second capacitor 216b with a first potential difference when the first control signal is applied so that the first potential difference charges the first input capacitor and the second input capacitor to provide the first charge signal.

[0025] The input switching mechanism configured to provide the second charge signal to the charge sensing stage 202 may include the input switching mechanism configured to apply the first capacitor 216a and the second capacitor 216b with a second potential difference when the second control signal is applied so that the second potential difference charges the first input capacitor 216a and the second input capacitor 216b to provide the second charge signal. The first potential difference and the second potential difference are in opposing directions. In various embodiments, the first potential difference and the second potential difference may have substantially the same magnitude. When the first potential difference varies in

magnitude as a result of changes in the external environment, the second potential difference may change by the same magnitude.

[0026] In various embodiments, the input stage 204 may include a first reference voltage ($V_{\text{ref+}}$) and a second reference voltage ($V_{\text{ref-}}$) to supply the first potential difference and the second potential difference. The input stage 204 may instead be configured to be coupled to the first reference voltage and the second reference voltage. In various other embodiments, the input stage may include a common reference voltage to supply the first potential difference and the second potential difference. The input stage may alternatively be coupled to the common reference voltage. In other words, the input stage may include or may be configured to be coupled to one or two reference voltages for providing the first potential difference across the capacitors when the first control signal is applied and the second potential difference across the capacitors when the second control signal is applied.

[0027] In various embodiments, the input switching mechanism 204 may include switches 220a, 220b, 220c, 220d, 220e, 220f.

[0028] The circuit arrangement may further include a first coupling circuit coupling the input stage to the output stage, the first coupling circuit configured to generate the third control signal for the output switching mechanism when the first control signal is applied to the first coupling circuit. The circuit arrangement may also include a second coupling circuit coupling the input stage to the output stage, the second coupling circuit configured to generate the fourth control signal for the output switching mechanism when the second control signal is applied to the second coupling circuit. In other words, the circuit arrangement may include a first coupling circuit coupling the input stage to the output stage so that after the working phase in which the first control signal is applied to the first coupling circuit, the third control signal is applied to the output switching mechanism. The circuit arrangement may include a second coupling circuit coupling the input stage to the output stage so that after the working phase in which the second control signal is applied to the second

coupling circuit, the fourth control signal is applied to the output switching mechanism.

[0029] In various embodiments, the output switching mechanism may include a first sample and hold circuit 222a and a second sample and hold circuit 222b. FIG. 2 shows an exemplary implementation of the output stage 206 as an illustration. Other implementations of the output stage 206 may also be possible.

[0030] The input stage 204 may further include a further input switching mechanism configured to provide a further first charge signal to the charge sensing stage 202 when a further first control signal, the further first control signal including a further first pulse with a rising edge and a falling edge, is applied to the further input switching mechanism and to provide a further second charge signal to the charge sensing stage 202 when a further second control signal, the further second control signal including a further second pulse with a rising edge and a falling edge, is applied to the further input switching mechanism. The output stage 206 may further include a further first output node and a further second output node. The output stage 206 may also include a further output switching mechanism configured to couple the charge sensing stage 202 to the further first output node when a further third control signal is applied to the further output switching mechanism, the further third control signal including a further third pulse with a rising edge behind the rising edge of the further first control signal and a falling edge before the falling edge of the further first control signal. The further output switching mechanism may be further configured to couple the charge sensing stage 202 to the second output node when a further fourth control signal is applied to the further output switching mechanism, the further fourth control signal including a further fourth pulse with a rising edge behind the rising edge of the further second control signal and a falling edge before the falling edge of the further second control signal.

[0031] The circuit arrangement may also include an enable switching mechanism coupling the input switching mechanism to the charge sensing stage 202. The circuit

arrangement may additionally include a further enable switching mechanism coupling the further input switching mechanism to the charge sensing stage 202. The input switching mechanism may be coupled to a first end of the enable switching mechanism, while the charge sensing stage 202 may be coupled to a second end of the enable switching mechanism. Likewise, the further input switching mechanism may be coupled to a first end of the further enable switching mechanism, while the charge sensing stage 202 may be coupled to a second end of the further enable switching mechanism. When the enable switching mechanism is switched on, the input switching mechanism may be connected to the charge sensing stage 202 and the first charge signal and/or the second charge signal may be provided to the charge sensing stage 202. Also, when the further enable switching mechanism is switched on, the further input switching mechanism may be connected to the charge sensing stage 202 and the further first charge signal and/or the further second charge signal may be provided to the charge sensing stage 202. When the enable switching mechanism is deactivated, the first charge signal and/or the second charge signal may not be provided to the charge sensing stage 202. The input switching mechanism may be electrically isolated from the charge sensing stage 202 when the enable switching mechanism is deactivated. Similarly, when the further enable switching mechanism is deactivated, the first charge signal and/or the second charge signal may not be provided to the charge sensing stage 202. The further input switching mechanism may be electrically isolated from the charge sensing stage 202 when the further enable switching mechanism is deactivated.

[0032] In general, the input stage 204 may further include one or more subsequent input switching mechanisms to form a plurality of input switching mechanisms. Each of the plurality of switching mechanisms may be configured to provide a respective first charge signal to the charge sensing stage 202 when a respective first control signal, the respective first control signal including a respective first pulse with a rising edge and a falling edge, is applied to the respective input switching mechanism and to

provide a respective second charge signal to the charge sensing stage 202 when a respective second control signal, the respective second control signal including a respective second pulse with a rising edge and a falling edge, is applied to the respective input switching mechanism. The output stage 206 may further include one or more subsequent first output nodes to form a plurality of first output nodes and one or more subsequent second output nodes to form a plurality of second output nodes. Each of the plurality of first output nodes may form one paired circuit with one respective second output node. In other words, the output stage 206 may include a plurality of paired circuits, each paired circuit including one respective first output node and one respective second output node. The output stage 206 may include one or more subsequent output switching mechanisms to form a plurality of output switching mechanisms. Each paired circuit may also include one respective output switching mechanism of the plurality of switching mechanisms, the respective output switching mechanism configured to couple the charge sensing stage 202 to the respective first output node when a respective third control signal is applied to the respective output switching mechanism, the respective third control signal including a respective third pulse with a rising edge behind the rising edge of the respective first control signal and a falling edge before the falling edge of the respective first control signal. The respective output switching mechanism may be further configured to couple the charge sensing stage 202 to the respective second output node when a respective fourth control signal is applied to the respective output switching mechanism, the respective fourth control signal including a respective fourth pulse with a rising edge behind the rising edge of the respective second control signal and a falling edge before the falling edge of the respective second control signal.

[0033] FIG. 3A is a schematic 300a showing a circuit arrangement according to various embodiments. The circuit arrangement may include a charge sensing stage 302. The circuit arrangement may also include an input stage 304 coupled to the charge sensing stage 302. The input stage 304 may include an input switching

mechanism configured to provide a first charge signal to the charge sensing stage 302 when a first control signal (T_1), the first control signal (T_1) including a first pulse with a rising edge and a falling edge, is applied to the input switching mechanism and to provide a second charge signal to the charge sensing stage when a second control signal (T_2), the second control signal (T_2) including a second pulse with a rising edge and a falling edge, is applied to the input switching mechanism. The circuit arrangement may further include an output stage 306 coupled to the charge sensing stage 302. The output stage 306 may include a first output node 308a. The output stage may further include a second output node 308b. The output stage 306 may additionally include an output switching mechanism configured to couple the charge sensing stage 302 to the first output node 308a when a third control signal (T_{1s}) is applied to the output switching mechanism, the third control signal (T_{1s}) including a third pulse with a rising edge behind the rising edge of the first control signal (T_1) and a falling edge before the falling edge of the first control signal (T_1); and to couple the charge sensing stage to the second output node 308b when a fourth control signal (T_{2s}) is applied to the output switching mechanism, the fourth control signal (T_{2s}) including a fourth pulse with a rising edge behind the rising edge of the second control signal (T_2) and a falling edge before the falling edge of the second control signal (T_2).

[0034] The circuit arrangement may be or may include a time-multiplexed differential capacitance-to-voltage converter (TMD-CVC).

[0035] The charge sensing stage 302 may include an amplifier 310 having a first input (e.g. inverting or negative input), a second input (e.g. non-inverting or positive input) and an output. The charge sensing stage 302 may also include a feedback capacitor 312 C_f having a first end coupled to the first input (inverting input) of the amplifier 310 and a second end coupled to the output of the amplifier 310. The charge sensing stage 302 may further include a reset switch mechanism 314 coupled in parallel to the feedback capacitor 312. The reset switch mechanism 314 may include

reset switch SW_1 . A first end of reset switch SW_1 may be coupled to first input of the amplifier 310 and the second end of reset switch SW_1 may be coupled to the output of the amplifier 310. The second input (non-inverting input) of the amplifier 310 may be configured to be coupled to ground. The amplifier 310 may be an operational amplifier or op-amp.

[0036] The first input of the amplifier 310 may be coupled to the input stage 304. The output of the amplifier 310 may be coupled to the output stage 306. The input stage 304 may include a first input capacitor C_{1s} 316a and a second input capacitor C_{2s} 316b connected in series. A node, i.e. input node 318, between the first input capacitor 316a and the second input capacitor 316b may be coupled to the charge sensing stage 302.

[0037] In various embodiments, a switch may refer to a three-way switch such as a transistor. The transistor may include a metal oxide field effect transistor (MOSFET) or a bipolar junction transistor (BJT). The transistor may include a control electrode, a first controlled electrode and a second controlled electrode. In various embodiments, when a voltage or signal of logic “high” is applied to the control electrode, the transistor may be activated and current may flow between the first controlled electrode and the second controlled electrode. Conversely, when a voltage or signal of logic “low” is applied to the control electrode, no current or an insubstantial current (such as leakage current) may flow between the first controlled electrode and the second controlled electrode. In various alternate embodiments, when a voltage or signal of logic “low” is applied to the control electrode, the transistor may be activated and current may flow between the first controlled electrode and the second controlled electrode. Conversely, when a voltage or signal of logic “high” is applied to the control electrode, no current or an insubstantial current (such as leakage current) may flow between the first controlled electrode and the second controlled electrode.

[0038] The input switching mechanism configured to provide the first charge signal to the charge sensing stage 302 may include the input switching mechanism

configured to apply the first capacitor 316a and the second capacitor 316b with a first potential difference when the first control signal (T_1) is applied so that the first potential difference charges the first input capacitor 316a and the second input capacitor 316b to provide the first charge signal. The node 318 may provide the first charge signal to the charge sensing stage 302.

[0039] The input switching mechanism configured to provide the second charge signal to the charge sensing stage 302 may include the input switching mechanism configured to apply the first capacitor 316a and the second capacitor 316b with a second potential difference when the second control signal (T_2) is applied so that the second potential difference charges the first input capacitor 316a and the second input capacitor 316b and to provide the second charge signal. The node 318 may provide the second charge signal to the charge sensing stage 302.

[0040] The first potential difference and the second potential difference may be in opposing directions. The first potential difference and the second potential difference may have the same magnitude but may have different polarities. The input stage may include a first reference voltage (V_{ref+}) and a second reference voltage (V_{ref-}) to supply the first potential difference and the second potential difference.

[0041] The input switching mechanism may include a first input switch 320a (denoted by SW_2), a second input switch 320b (denoted by SW_3), a third input switch 320c (denoted by SW_4), a fourth input switch 320d (denoted by SW_5), a fifth input switch 320e (denoted by SW_6) and a sixth input switch 320f (denoted by SW_7). The first input switch 320a may include a first end coupled to the first capacitor 316a and a second end coupled or configured to be coupled to ground. The second input switch 320b may include a first end coupled to the second capacitor 316b and a second end coupled or configured to be coupled to ground. The third input switch 320c may include a first end coupled or configured to be coupled to the first reference voltage (V_{ref+}) and a second end coupled to the first capacitor 316a. The fourth input switch 320d may include a first end coupled or configured to be coupled to the second

reference voltage ($V_{\text{ref-}}$) and a second end coupled to the second capacitor 316b. The fifth input switch 320e may include a first end coupled or configured to be coupled to the first reference voltage ($V_{\text{ref+}}$) and a second end coupled to the second capacitor 316b. The sixth input switch 320f may include a first end coupled or configured to be coupled to the second reference voltage ($V_{\text{ref-}}$) and a second end coupled to the first capacitor 316a.

[0042] The reset switch 314, the first input switch 320a and the second input switch 320b may be controlled by the reset signal Φ_1 . The third and fourth input switches 320c, 320d may be controlled by the first control signal T_1 while the fifth and sixth input switches 320e, 320f may be controlled by the second control signal T_2 .

[0043] The output switching mechanism may include a first output switch 322a (denoted by SW_8) and a second output switch 322b (denoted by SW_9). The first output switch 322a may include a first end coupled to the output of the amplifier 310 and a second end coupled to the first output node 308a. The second output switch 322b may include a first end coupled to the output of the amplifier 310 and a second end coupled to the second output node 308b. The first output switch 322a may be controlled by the third control signal T_{1s} while the second output switch 322b may be controlled by the fourth control signal T_{2s} .

[0044] The output switching mechanism may also include a first output capacitor 324a (C_{h1}) and a second output capacitor 324b (C_{h2}). The first end of the first output capacitor 324a may be coupled to the first output node 308a and the second end may be coupled or configured to be coupled to ground. The first end of the second output capacitor 324b may be coupled to the second output node 308b and the second end may be coupled or configured to be coupled to ground.

[0045] FIG. 3B is a graph 300b illustrating the control signals (T_1 , T_2 , T_{1s} , T_{2s}) and reset signal (Φ_1) applied to the circuit arrangement according to various embodiments. The control signals (T_1 , T_2 , T_{1s} , T_{2s}) and reset signal (Φ_1) may also be referred to as clock signals. 350a indicates the reset signal (Φ_1), which may include a plurality of

pulses, which may be referred to as reset pulses. The reset pulses may be separated by troughs, which may be referred to as reset troughs. In other words, reset signal 350a may include a plurality of logical highs and a plurality of logical lows, one logical high separated from a successive logical high by a logical low. The period of one logical high may be equal to the period of another logical high. The period of one logical low may be equal to the period of another logical low. The period of one logical high may be equal to the period of one logical low. A period may also be referred to as a duration. Each pulse may be or may include one logical high. Each pulse may include a rising edge, a flat portion, and a falling edge. The rising edge may go from a preceding logical low to a start of the flat portion. The voltage of the flat portion may be substantially equal throughout the flat portion (from start to end of the flat portion). The fall edge may go from an end of the flat portion to a subsequent logical low.

[0046] 350b indicates the first control signal (T_1), 350c indicates the second control signal (T_2), 350d indicates the third control signal (T_{1s}), and 350e indicates the fourth control signal (T_{2s}). The control signals indicated by 350b, 350c, 350d, 350e may also include a series of pulses. In other words, the control signals 350b, 350c, 350d, 350e may include a plurality of logical highs and a plurality of logical lows, one logical high separated from a successive logical high by a logical low.

[0047] The frequency of the reset signal 350a may be about twice that of the control signals 350b, 350c, 350d, 350e. A pulse of the reset signal 350a may be separated from a further pulse of the reset signal 350a by a pulse of the first control signal 350b. The further pulse of the reset signal 350a may be separated from another pulse of the reset signal 350a by a pulse of the second control signal 350c. The portion of the second control signal 350c between the pulse and the further pulse of the reset signal 350a may be at logical low and the portion of the first control signal 350b between the further pulse and the other pulse of the reset signal 350a may be at logical low.

[0048] The third control signal 350d may be based on the first control signal 350b. A duration of a pulse of the third control signal 350d may be contained within a duration of a pulse of the first control signal 350b. The pulse of the third control signal 350d (herein also referred to as selected pulse) contained within a pulse of the first control signal 350b (herein also referred to as corresponding pulse) may have a rising edge that is behind the rising edge of the corresponding pulse and a falling edge that is before the falling edge of the corresponding pulse. An edge of a pulse coinciding with an edge of another pulse may mean that the edges of the two pulses occur at the same time. The flat portion of the selected pulse of the third control signal 350d may be of a shorter duration than the flat portion of the corresponding pulse of the first control signal 350b.

[0049] Similarly, the fourth control signal 350e may be based on the second control signal 350c. A duration of a pulse of the fourth control signal 350e may be contained within a duration of a pulse of the second control signal 350c. The pulse of the fourth control signal 350e (herein also referred to as selected pulse) contained within a pulse of the second control signal 350c (herein also referred to as corresponding pulse) may have a rising edge that is behind the rising edge of the corresponding pulse and a falling edge that is before the falling edge of the corresponding pulse. The flat portion of the selected pulse of the fourth control signal 350e may be of a shorter duration than the flat portion of the corresponding pulse of the second control signal 350c.

[0050] A pulse of the first control signal may also be referred to as a first pulse of the first control signal, a pulse of the second control signal may also be referred to as a second pulse of the second control signal, a pulse of the third control signal may also be referred to as a third pulse of the third control signal, a pulse of the fourth control signal may also be referred to as a fourth pulse of the fourth control signal, and a pulse of the reset signal may be referred to as a reset pulse of the reset signal.

[0051] Various embodiments may relate to a multi-rate switched-capacitor design. Various embodiments may involve the storage of two time-multiplexed output results

arising from two transfer phases of TMD-CVC. This arrangement may permit conversion of capacitive sensor signal from a single-ended CVC output to the time-multiplexed output signal in differential format. The fundamental clock frequency (Φ_1) of the readout circuit may be m times faster than that of the multiplexed clock rate. As shown in FIG. 3B, m may be set equal to 2. As far as the time multiplexing rate is much larger than the sensor signal frequency, the latency contributed by the switching duration of time-multiplex clock may be kept to minimum so as to reduce the sampled signal error due to latency. Therefore, the opposite cycle of converted electrical signal in the time-multiplexed based cross-coupling switching network may be very close to the magnitude of positive cycle generated by the single-ended CVC in the earlier time-multiplexing action.

[0052] Unlike in the classical fully differential structure, the matching requirement for the feedback capacitor 312 C_f , the reset switch 314 SW_1 , and the symmetry requirement of op-amp implementation may be eliminated because the differential signal is generated by the same set of circuit components.

[0053] This may lead to smaller circuit error and simpler op-amp circuit architecture whilst without encountering the common-mode feedback circuit in differential readout circuit design. Besides, the common mode components such as $1/f$ noise, DC offset and/or switch errors contributed by charge injection and clock feed-through and thermal drift may be simultaneously reduced by the use of time-multiplexed differential output of the TMD-CVC.

[0054] With reference to FIG. 3A, the differential capacitive sensor pair formed by C_{1s} and C_{2s} may be controlled by seven switches 314, 320a - 320f (SW_1 - SW_7) for time-multiplexing operation. Three switches 314, 320a, 320b (SW_1 - SW_3) may be controlled by the reset clock Φ_1 . Switches 320c, 320d (SW_4 - SW_5) may be controlled by the clock signal T_1 whereas switches 320e, 320f (SW_6 - SW_7) may be controlled by the clock signal T_2 . The feedback capacitor 314 (C_f) and the op-amp 310 OA_1 serve the charge-to-voltage conversion. The single-ended output of the op-amp 310 OA_1

may be sampled by two sample-and-hold networks formed by the holding capacitors 324a (C_{h1}) and 324b (C_{h2}) together with respective switches 322a (SW_8) and 322b (SW_9) under the control of the corresponding sub clock signals, T_{1s} and T_{2s} respectively.

[0055] The non-overlapping clock periods between the switch pairs, 320c, 320d (SW_4 – SW_5) and 320e, 320f (SW_6 – SW_7), may be controlled by T_1 and Φ_1 , T_2 and Φ_1 respectively. The reset clock Φ_1 may be designed to have twice the frequency of that of T_1 and T_2 . When Φ_1 is off and T_1 goes high, the capacitive sensor signal may be converted at the output of op-amp 310 (OA_1) which is sampled by the holding capacitor 324a (C_{h1}) to yield V_{o1} . The same goes for T_2 period with the corresponding holding capacitor 324b (C_{h2}) to yield V_{o2} . Due to the swapping action across the voltage references, V_{ref+} and V_{ref-} , during T_2 on-period, the generated output V_{o2} may be opposite with respect to V_{o1} . In other words, the output voltage at the first output node 308a and the output voltage at the second output node 308b may have substantially the same magnitude but may have opposite polarity. Therefore, a time-multiplexed differential signal may be established between V_{o1} and V_{o2} .

[0056] For capacitive sensor with large parasitic capacitance, the charging and discharging action in CVC may cause spikes because the voltages on the capacitors cannot change instantly. It may need time to charge or discharge to settle to the final values. The magnitude and duration of spikes may depend upon the size of parasitic capacitances. It may be significant in bulk micro-machined capacitive sensors whereas it may be negligible in surface micro-machined capacitive sensors. The spikes may contribute DC offset of the sensing interface. It may occur when the reset signal Φ_1 is turned on or when T_1 or T_2 signals are turned on during the charge transfer phase. In order to reduce the impact of spikes, two special sample-and-hold sub clocks, T_{1s} and T_{2s} , may be generated with the guard band, which rise up later and fall down earlier than the corresponding charge transfer clocks T_1 and T_2 .

[0057] The overall on-period for T_{1s} and T_{2s} may be less than the respective period, T_1 and T_2 . This arrangement may ensure that the corresponding output signal being sampled to the associated holding capacitors 324a, 324b are isolated first prior to the arrival of big spikes for the stated switching transitions. Ultimately, this may help provide a glitch-free SC design with the dedicated sample-and-hold process.

[0058] The functioning steps may be summarized as follows: (a) When Φ_1 turns on, both the sensing capacitors 316a, 316b and the op-amp 310 may be reset. (b) Φ_1 turns off, T_1 turns on, the reference voltages V_{ref+} , V_{ref-} may charge up the sensing capacitors 316a, 316b and the output voltage V_{o1} starts to develop at the feedback capacitor 312. (c) After a certain delay, T_{1s} may turn on and the output voltage V_{o1} may be sampled and stored on capacitor 324a C_{h1} . (d) This may be then followed by the turn-on of Φ_1 again to reset the sensing elements 316a, 316b and the op-amp 310 prior to the second charge transfer phase. (e) After Φ_1 turns off, T_2 may turn on, the reference voltages V_{ref+} , V_{ref-} may be interchanged to generate a time-multiplexed differential sensing charge signal across capacitor 312 (C_f). (f) T_{2s} may turn on and the output voltage V_{o2} may be sampled and stored on capacitor 324b C_{h2} . (g) The process may be repeated again.

[0059] The input switching mechanism may be configured to apply the first capacitor 316a and the second capacitor 316b with a first potential difference when the first control signal is applied and may be configured to apply the first capacitor and the second capacitor with a second potential difference opposite the first potential difference when the second control signal is applied. The circuit arrangement may be further configured to apply the reset signal between applying the first control signal and the second control signal and/or applying the second control signal and the first control signal. The reset signal may discharge the charges in capacitors 316a, 316b. The reset signal may further reset the op-amp 310.

[0060] FIG. 3C is a schematic 300c of the circuit arrangement shown in FIG. 3A according to various embodiments with error sources. The errors may be represented

as voltage sources 326a, 326b connected to the non-inverting (positive) input of the op-amp 310. 326a may represent offset error (denoted as V_{os}) and 326b may represent flicker noise (V_{no}). Assume that the gain of the op-amp 310 is high enough and the sensing capacitances can be fully charged and discharged with adequate time constant in half a clock period. When Φ_1 is on, the sensing capacitors 316a (C_{1s}), 316b (C_{2s}) and the integration capacitor 312 (C_f) as well as the op-amp 310 may be in reset mode. The DC offset voltage and the low-frequency flicker noise may charge up the sensing capacitors 316a (C_{1s}) and 316b (C_{2s}) as

$$V_{C_{1s}} = V_{C_{2s}} = -V_{os} - V_{no} \quad (1)$$

[0061] In the next phase, Φ_1 may be turned off, the channel charge of switch SW_1 may flow out to both the output node and the negative input node of the op-amp 310. The injected charge may be approximated as equal under fast clock transition. The half-channel charge $Q_{SW1}/2$ going to the negative input of the op-amp 310 may cause a DC offset at the output while the other half may only cause a temporary glitch. When T_1 is turned on, the reference voltages may start to charge up the two sensing capacitors 316a, 316b. The charging current flowing through capacitor 316a (C_{1s}) and 316b (C_{2s}) may be substantially the same with that of the feedback capacitor 312 (C_f). Using conservation of charge at virtual ground node of op-amp 310 and taken into the non-ideal effects from low-frequency noise, DC offset and switch error, the analytical expression may be obtained as follows:

$$[V_{ref+} - V_{os} - V_{no} - (-V_{os} - V_{no})]C_{1s} + [V_{ref-} - V_{os} - V_{no} - (-V_{os} - V_{no})]C_{2s} = [V_{os} + V_{no} - V_{ol}(n)]C_f - Q_{SW1}(n)/2 \quad (2)$$

$$V_{ol}(n) = -\frac{C_{1s}V_{ref+} + C_{2s}V_{ref-}}{C_f} + \underline{V_{os} + V_{no}} - \underline{\frac{Q_{SW1}(n)}{2C_f}} \quad (3)$$

[0062] The output voltage $V_{ol}(n)$ may be sampled by capacitor 324a (C_{hl}). The last three terms (underlined) represent the abovementioned error sources.

[0063] After T_1 turns off, Φ_1 may be turned on, and the circuit arrangement may be in reset mode again. The sensing capacitors 316a, 316b may be charged to about the same value as given in Equation (1) previously.

$$V_{C_{1s}} = V_{C_{2s}} = -V_{os} - V_{no} \quad (4)$$

[0064] In next phase, after Φ_1 is turned on, a fraction of the channel charge may again cause a DC offset at the output. When T_2 is turned on, the interchanged reference voltages may charge up the sensing capacitors 316a, 316b. The resulting charge currents from sensing capacitors 316a, 316b may flow through the feedback capacitor 312 (C_f). Thus, we get

$$\begin{aligned} [V_{ref-} - V_{os} - V_{no} - (-V_{os} - V_{no})]C_{1s} + [V_{ref+} - V_{os} - V_{no} - (-V_{os} - V_{no})]C_{2s} = \\ [V_{os} + V_{no} - V_{o2}(n + \frac{1}{2})]C_f - Q_{SW1}(n + \frac{1}{2})/2 \end{aligned} \quad (5)$$

$$V_{o2}(n + \frac{1}{2}) = \frac{C_{1s}V_{ref+} + C_{2s}V_{ref-}}{C_f} + V_{os} + V_{no} - \frac{Q_{SW1}(n + \frac{1}{2})}{2C_f} \quad (6)$$

[0065] The output voltage $V_{o2}(n)$ may be sampled by capacitor 324b (C_{h2}). Apart from the opposite sign in signal by comparing to Equation (3), the overall DC error as indicated by the underline in (6) may be almost the same. More importantly, the two resulting error voltages may be regarded as common mode components which may be eliminated by the differential operation in the next stage.

[0066] Comparing Equations (3) and (6), we may observe that there is a half clock period delay between these two output signals. Since the sampling clock frequency (typical > 10 KHz) is much higher than the signal frequency (0 ~ 200 Hz), the delay may be deemed negligible. Differential operation may be needed to generate the final output of the readout circuit.

[0067] FIG. 3D is a schematic 300d of the circuit arrangement shown in FIG. 3A according to various embodiments with parasitic capacitance. The parasitic capacitance between the common middle sensing node 318 of the capacitive sensing pair 316a (C_{1s}) and 316b (C_{2s}) and ground may be represented by 328. A_v may be the

finite open-loop gain of the op-amp 310 and V_x may be the voltage at the inverting (negative) input node of the op-amp 310. The analysis may be given as follows:

$$[V_{o1}(n) - V_x]C_f = V_x C_p + (V_x - V_{ref+})C_{1s} + (V_x - V_{ref-})C_{2s} \quad (7)$$

$$V_o(n) = -A_v V_x \quad (8)$$

$$V_{o1}(n) = -\frac{V_{ref+}C_{1s}A_v + V_{ref-}C_{2s}A_v}{C_p + C_{1s} + C_{2s} + (1 + A_v)C_f} \quad (9)$$

$$[V_{o2}(n + \frac{1}{2}) - V_x]C_f = V_x C_p + (V_x - V_{ref+})C_{1s} + (V_x - V_{ref-})C_{2s} \quad (10)$$

$$V_o(n) = -A_v V_x \quad (11)$$

$$V_{o2}(n + \frac{1}{2}) = -\frac{V_{ref+}C_{1s}A_v + V_{ref-}C_{2s}A_v}{C_p + C_{1s} + C_{2s} + (1 + A_v)C_f} \quad (12)$$

[0068] If C_p is not too great, the open-loop gain of the op-amp 310 is made high enough, the value of $(1+A_v)C_f$ is much higher than the normal sensing capacitance values for capacitors 316a (C_{1s}), 316b (C_{2s}) as well as the parasitic capacitance (C_p), the finite gain error may become negligible.

[0069] FIG. 4A is a schematic 400a showing a circuit arrangement according to various embodiments. The circuit arrangement may include a charge sensing stage 402. The circuit arrangement may also include an input stage 404 coupled to the charge sensing stage 402. The input stage 404 may include an input switching mechanism configured to provide a first charge signal to the charge sensing stage 402 when a first control signal (T_1), the first control signal (T_1) including a first pulse with a rising edge and a falling edge, is applied to the input switching mechanism and to provide a second charge signal to the charge sensing stage when a second control signal (T_2), the second control signal (T_2) including a second pulse with a rising edge and a falling edge, is applied to the input switching mechanism. The circuit arrangement may further include an output stage 406 coupled to the charge sensing stage 404. The output stage 406 may include a first output node. The output stage may further include a second output node. The output stage 406 may additionally include

an output switching mechanism configured to couple the charge sensing stage 402 to the first output node when a third control signal (T_{1s}) is applied to the output switching mechanism, the third control signal (T_{1s}) including a third pulse with a rising edge behind the rising edge of the first control signal (T_1) and a falling edge before the falling edge of the first control signal (T_1); and to couple the charge sensing stage 402 to the second output node when a fourth control signal (T_{2s}) is applied to the output switching mechanism, the fourth control signal (T_{2s}) including a fourth pulse with a rising edge behind the rising edge of the second control signal (T_2) and a falling edge before the falling edge of the second control signal (T_2).

[0070] The charge sensing stage 402 may be similar to the charge sensing stage 302 shown in FIG. 3A and may include an amplifier 410 having a first input (inverting input), a second input (non-inverting input) and an output. The charge sensing stage 402 may also include a feedback capacitor 412 (C_f) having a first end coupled to the first input (inverting input) of the amplifier 410 and a second end coupled to the output of the amplifier 410. The charge sensing stage 402 may further include a reset switch mechanism 414 coupled in parallel to the feedback capacitor 412. The reset switch mechanism 414 may include reset switch.

[0071] The input stage 404 may include a first input capacitor 416a (C_{1s}) and a second input capacitor 416b (C_{2s}) connected in series. A node 418 between the first input capacitor 416a and the second input capacitor 416b may be coupled to the charge sensing stage.

[0072] The input switching mechanism may be configured to provide the first charge signal to the charge sensing stage 402 may include the input switching mechanism configured to apply the first capacitor 416a and the second capacitor 416b with a first potential difference when the first control signal is applied so that the first potential difference charges up the first input capacitor 416a and the second input capacitor 416b to provide the first charge signal.

[0073] The input switching mechanism may be configured to provide the second charge signal to the charge sensing stage 402 may include the input switching mechanism configured to apply the first capacitor 416a and the second capacitor 416b with a second potential difference when the second control signal is applied so that the second potential difference charges up the first input capacitor and the second input capacitor to provide the second charge signal.

[0074] The first potential difference and the second potential difference have the same magnitude but may be in opposing directions. The input stage 404 may include or may be configured to couple to a common reference voltage V_{ref} to supply the first potential difference and the second potential difference. In other words, the input stage 404 may include or may be configured to be coupled to one single reference voltage to generate both the first potential difference and the second potential difference.

[0075] The input stage 404 may include a first input switch 420a having a first end coupled to the first capacitor 416a and a second end coupled or configured to be coupled to the common reference voltage. The input stage 404 may include a second input switch 420b having a first end coupled to the second capacitor 416b and a second end coupled or configured to be coupled to the common reference voltage. The input stage 404 may include a third input switch 420c having a first end coupled to the first capacitor 416a and a second end coupled or configured to be coupled to ground. The input stage 404 may include a fourth input switch 420d having a first end coupled to the second capacitor 416b and a second end coupled or configured to be coupled to ground.

[0076] The output switching mechanism may include a first sample and hold circuit 422a and a second sample and hold circuit 422b. The first sample and hold circuit 422a may include a first output switch with a first end coupled to the output of the amplifier 410 and a second end coupled to a first output node (similar to FIG. 3A). The first sample and hold circuit 422a may also include a first output capacitor with a

first end be coupled to the first output node and a second end coupled or configured to be coupled to ground.

[0077] Likewise, the second sample and hold circuit 422b may include a second output switch with a first end coupled to the output of the amplifier 410 and a second end coupled to a second output node (similar to FIG. 3A). The second sample and hold circuit 422b may also include a second output capacitor with a first end be coupled to the second output node and a second end coupled or configured to be coupled to ground.

[0078] The reset switch 414 may be controlled by the reset signal Φ_1 . The first and fourth input switches 420a, 420d may be controlled by the first control signal T_1 while the second and third input switches 420b, 420c may be controlled by the second control signal T_2 . The first sample and hold circuit 422a may be controlled by the third control signal T_{1s} and the second sample and hold circuit 422b may be controlled by the fourth control signal T_{2s} .

[0079] FIG. 4B is a graph 400b illustrating the control signals (T_1 , T_2 , T_{1s} , T_{2s}) and reset signal (Φ_1) applied to the circuit arrangement according to various embodiments. 450a indicates the reset signal (Φ_1), 450b indicates the first control signal (T_1), 450c indicates the second control signal (T_2), 450d indicates the third control signal (T_{1s}) and 450e indicates the fourth control signal (T_{2s}). The signals indicated by 450a, 450b, 450c, 450d, 450e may also include a series of pulses. In other words, the signals 450a, 450b, 450c, 450d, 450e may include a plurality of logical highs and a plurality of logical lows, one logical high separated from a successive logical high by a logical low.

[0080] A pulse of the reset signal 450a may be separated from a further pulse of the reset signal 450a by a pulse of the third control signal 450d. The further pulse of the reset signal 450a may be separated from another pulse of the reset signal 450a by a pulse of the fourth control signal 450e. The portion of the fourth control signal 450e between the pulse and the further pulse of the reset signal 450a may be at logical low

and the portion of the third control signal 450d between the further pulse and another pulse of the reset signal 450a may be at logical low.

[0081] The third control signal 450d may be based on the first control signal 450b. A duration of a pulse of the third control signal 450d may be contained within a duration of a pulse of the first control signal 450b. The pulse of the third control signal 450d (herein also referred to as selected pulse) contained within a pulse of the first control signal 450b (herein also referred to as corresponding pulse) may have a rising edge that is behind the rising edge of the corresponding pulse and a falling edge that is before the falling edge of the corresponding pulse. The flat portion of the selected pulse of the third control signal 450d may be of a shorter duration than that of the flat portion of the corresponding pulse of the first control signal 450b.

[0082] Similarly, the fourth control signal 450e may be based on the second control signal 450c. A duration of a pulse of the fourth control signal 450e may be contained within a duration of a pulse of the second control signal 450c. The pulse of the fourth control signal 450e (herein also referred to as selected pulse) contained within a pulse of the second control signal 450c (herein also referred to as corresponding pulse) may have a rising edge that is behind the rising edge of the corresponding pulse and a falling edge that is before the falling edge of the corresponding pulse. The flat portion of the selected pulse of the fourth control signal 450e may be of a shorter duration than that of the flat portion of the corresponding pulse of the second control signal 450c.

[0083] In various embodiments, a duration of a pulse of the first control signal, i.e. the first pulse, may include a duration of a pulse of the third control signal (the third pulse) and a duration of a pulse of the reset signal (the reset pulse). A duration of a pulse of the second control signal, i.e. the second pulse, may include a duration of a pulse of the fourth control signal (the fourth pulse) and a duration of a pulse of the reset signal (the reset pulse). In other words, a third pulse and a reset pulse may occur

when there is a first pulse. A fourth pulse and a reset pulse may occur when there is a second pulse.

[0084] FIG. 4C is an illustration 400c showing the operation of a circuit arrangement according to various embodiments. The circuit arrangement may involve time-multiplexed control clock. The reset signal 450a (Φ_1) may reset the circuit arrangement by discharging the capacitors 416a, 416b. The reset signal 450a may further reset the op-amp 410. The circuit arrangement may involve two modes of charge transfer. During the first mode, the first control signal 450b (T_1) may be applied. The third control signal 450d (T_{1s}) may be based or derived from the first control signal 450b. The output voltage V_{o1} may be generated on the first output node. During the second mode, the second control signal 450c (T_2) may be applied. The fourth control signal 450e (T_{2s}) may be based or derived from the second control signal 450c. The output voltage V_{o2} may be generated on the second output node.

[0085] As shown in FIGS. 4A-C, the time-multiplexed differential output technique may also be implemented with a single voltage reference based time-multiplexed design. The multiplexing action may be based on the two switching periods T_1 and T_2 that involve the connection of respective switches associated with the sensing capacitors 416a (C_{1s}), 416b (C_{2s}) and the reset phase of amplifier 410. Contrasting to the differential voltage reference design shown in FIG. 3A, each switching period (T_1 or T_2) may embody two clock sequences. They are (i) a sub clock phase either T_{1s} or T_{2s} and (ii) a reset signal Φ_1 . With respective sample-and-hold circuits 422a, 422b located at the output of switched-capacitor amplifier 410, a time-multiplexed differential signal may be equally generated.

[0086] Various embodiments may reduce or eliminate the need of bulky Wheatstone bridge arrangement of 4 capacitive sensing elements whilst giving fully differential output using a single stage operational amplifier interfacing the differential sensing capacitor pair (e.g. C_{1s} and C_{2s}). Various embodiments may reduce the complexity and cost for manufacture of the capacitive sensing elements and readout interface circuitry

due to the use of single-ended operational amplifier circuitry architecture and still achieve fully differential operation.

[0087] Various embodiments may reduce the power consumption and complexity when compared with that of the conventional fully differential circuitry arrangement. Various embodiments may provide comparable output swing as that of conventional fully differential readout circuit but with almost double the output swing as compared to the conventional single-ended capacitive sensor readout circuits.

[0088] Various embodiments may provide the performance advantages such as improved signal / noise (S/N) ratio, DC offset and/or thermal drift with respect to the fully differential circuitry having larger component counts. Various embodiments may reduce the stringent requirement for device performance matching of components as compared to that of conventional differential CVC.

[0089] Various embodiments may eliminate or reduce stringent common-mode circuit design requirement, which is essential in conventional differential readout circuit design.

[0090] FIG. 5A is a schematic 500a illustrating a circuit arrangement according to various embodiments. The circuit arrangement may include a charge sensing stage 502. The circuit arrangement may also include an input stage 504 coupled to the charge sensing stage 502. The input stage 504 may include an input switching mechanism 530a configured to provide a first charge signal to the charge sensing stage 502 when a first control signal (T_1), the first control signal (T_1) including a first pulse with a rising edge and a falling edge, is applied to the input switching mechanism 530a and to provide a second charge signal to the charge sensing stage when a second control signal (T_2), the second control signal (T_2) including a second pulse with a rising edge and a falling edge, is applied to the input switching mechanism 530a. The circuit arrangement may further include an output stage 506 coupled to the charge sensing stage 504. The output stage 506 may include a first output node. The output stage may further include a second output node. The output

stage 506 may additionally include an output switching mechanism 532a configured to couple the charge sensing stage 502 to the first output node when a third control signal (T_{1s}) is applied to the output switching mechanism 532a, the third control signal (T_{1s}) including a third pulse with a rising edge behind the rising edge of the first control signal (T_1) and a falling edge before the falling edge of the first control signal (T_1); and to couple the charge sensing stage 502 to the second output node when a fourth control signal (T_{2s}) is applied to the output switching mechanism 532a, the fourth control signal (T_{2s}) including a fourth pulse with a rising edge behind the rising edge of the second control signal (T_2) and a falling edge before the falling edge of the second control signal (T_2).

[0091] The input stage 504 may further include a further input switching mechanism 530b configured to provide a further first charge signal to the charge sensing stage 502 when a further first control signal (P_1), the further first control signal (P_1) including a further first pulse with a rising edge and a falling edge, is applied to the further input switching mechanism and to provide a further second charge signal to the charge sensing stage 502 when a further second control signal (P_2), the further second control signal (P_2) including a further second pulse with a rising edge and a falling edge, is applied to the further input switching mechanism 530b. The output stage 506 may further include a further first output node and a further second output node. The output stage 506 may also include a further output switching mechanism 532b configured to couple the charge sensing stage 502 to the further first output node when a further third control signal (P_{1s}) is applied to the further output switching mechanism 532b, the further third control signal (P_{1s}) including a further third pulse with a rising edge behind the rising edge of the further first control signal (P_1) and a falling edge before the falling edge of the further first control signal (P_1). The further output switching mechanism 532b may be further configured to couple the charge sensing stage 502 to the second output node when a further fourth control signal (P_{2s}) is applied to the further output switching mechanism, the further fourth control signal

(P_{2s}) including a further fourth pulse with a rising edge behind the rising edge of the further second control signal (P₂) and a falling edge before the falling edge of the further second control signal (P₂).

[0092] The input stage 504 may further include another input switching mechanism 530c configured to provide another first charge signal to the charge sensing stage 502 when another first control signal (Q₁), the other first control signal (Q₁) including another first pulse with a rising edge and a falling edge, is applied to the other input switching mechanism and to provide another second charge signal to the charge sensing stage 502 when another second control signal (Q₂), the other second control signal (Q₂) including a further second pulse with a rising edge and a falling edge, is applied to the other input switching mechanism 530c. The output stage 506 may further include another first output node and another second output node. The output stage 506 may also include another output switching mechanism 532c configured to couple the charge sensing stage 502 to the other first output node when another third control signal (Q_{1s}) is applied to the other output switching mechanism, the other third control signal (Q_{1s}) including another third pulse with a rising edge behind the rising edge of the other first control signal (Q₁) and a falling edge before the falling edge of the other first control signal (Q₁). The other output switching mechanism may be further configured to couple the charge sensing stage 502 to the second output node when another fourth control signal (Q_{2s}) is applied to the other output switching mechanism 532c, the other fourth control signal (Q_{2s}) including another fourth pulse with a rising edge behind the rising edge of the other second control signal (Q₂) and a falling edge before the falling edge of the other second control signal (Q₂).

[0093] The circuit arrangement may also include an enable switching mechanism 534a coupling the input switching mechanism 530a to the charge sensing stage 502. The circuit arrangement may additionally include a further enable switching mechanism 534b coupling the further input switching mechanism 530b to the charge sensing stage 502. The circuit arrangement may also include another enable switching

mechanism 534c coupling the other input switching mechanism 530c to the charge sensing stage 502. The input switching mechanism 530a may be coupled to a first end of the enable switching mechanism 534a, while the charge sensing stage 502 may be coupled to a second end of the enable switching mechanism 534a. Likewise, the further input switching mechanism 530b may be coupled to a first end of the further enable switching mechanism 534b, while the charge sensing stage 502 may be coupled to a second end of the further enable switching mechanism 534b. The other input switching mechanism 530c may be coupled to a first end of the other enable switching mechanism 534c, while the charge sensing stage 502 may be coupled to a second end of the other enable switching mechanism 534c.

[0094] When the enable switching mechanism 534a is switched on, the input switching mechanism 530a may be connected to the charge sensing stage 502 and the first charge signal and/or the second charge signal may be provided to the charge sensing stage 502. Also, when the further enable switching mechanism 534b is switched on, the further input switching mechanism 530b may be connected to the charge sensing stage 502 and the further first charge signal and/or the further second charge signal may be provided to the charge sensing stage 502. When the other enable switching mechanism 534c is switched on, the other input switching mechanism 530c may be connected to the charge sensing stage 502 and the other first charge signal and/or the other second charge signal may be provided to the charge sensing stage 502.

[0095] When the enable switching mechanism 534a is deactivated or switched off, the first charge signal and/or the second charge signal may not be provided to the charge sensing stage 502. When the further enable switching mechanism 534b is deactivated or switched off, the further first charge signal and/or the further second charge signal may not be provided to the charge sensing stage 502. When the other enable switching mechanism 534c is deactivated or switched off, the other first charge signal

and/or the other second charge signal may not be provided to the charge sensing stage 502.

[0096] When the first control signal T_1 is applied to the input switching mechanism 530a, the third control signal T_{1s} may be applied to the output switching mechanism 532a. When the second control signal T_2 is applied to the input switching mechanism 530a, the fourth control signal T_{2s} may be applied to the output switching mechanism 532a. Similarly, when the further first control signal P_1 is applied to the further input switching mechanism 530b, the further third control signal P_{1s} may be applied to the further output switching mechanism 532b. When the further second control signal P_2 is applied to the further input switching mechanism 530b, the further fourth control signal P_{2s} may be applied to the further output switching mechanism 532b. When the other first control signal Q_1 is applied to the other input switching mechanism 530c, the other third control signal Q_{1s} may be applied to the other output switching mechanism 532c. When the other second control signal Q_2 is applied to the other input switching mechanism 530c, the other fourth control signal Q_{2s} may be applied to the other output switching mechanism 532c.

[0097] In general, the input stage 504 may further include one or more subsequent input switching mechanisms to form a plurality of input switching mechanisms. Each of the plurality of switching mechanisms may be configured to provide a respective first charge signal to the charge sensing stage 502 when a respective first control signal, the respective first control signal including a respective first pulse with a rising edge and a falling edge, is applied to the respective input switching mechanism and to provide a respective second charge signal to the charge sensing stage 502 when a respective second control signal, the respective second control signal including a respective second pulse with a rising edge and a falling edge, is applied to the respective input switching mechanism. The output stage 506 may further include one or more subsequent first output nodes to form a plurality of first output nodes and one or more subsequent second output nodes to form a plurality of second output nodes.

Each of the plurality of first output nodes may form one paired circuit with one respective second output node. In other words, the output stage 506 may include a plurality of paired circuits, each paired circuit including one respective first output node and one respective second output node. The output stage 506 may include one or more subsequent output switching mechanisms to form a plurality of output switching mechanisms. Each paired circuit may also include one respective output switching mechanism of the plurality of switching mechanisms, the respective output switching mechanism configured to couple the charge sensing stage 502 to the respective first output node when a respective third control signal is applied to the respective output switching mechanism, the respective third control signal including a respective third pulse with a rising edge behind the rising edge of the respective first control signal and a falling edge before the falling edge of the respective first control signal. The respective output switching mechanism may be further configured to couple the charge sensing stage 502 to the respective second output node when a respective fourth control signal is applied to the respective output switching mechanism, the respective fourth control signal including a respective fourth pulse with a rising edge behind the rising edge of the respective second control signal and a falling edge before the falling edge of the respective second control signal.

[0098] The circuit arrangement may also include a respective enable switching mechanism coupling each input switching mechanism to the charge sensing stage. Each input switching mechanism may be coupled to a first end of the respective enable switching mechanism, while the charge sensing stage 502 may be coupled to a second end of the respective enable switching mechanism. When the respective enable switching mechanism is switched on, the respective input switching mechanism may be connected to the charge sensing stage and the respective first charge signal and/or the respective second charge signal may be provided to the charge sensing stage. When the respective enable switching mechanism is deactivated or switched off, the respective first charge signal and/or the second charge signal may

not be provided the charge sensing stage 502. In other words, the first charge signal and/or the second charge signal may be provided to the charge sensing stage 502 by the respective input switching mechanism only when the respective enable switching mechanism coupled to the respective input switching mechanism is activated or turned on.

[0099] Each third control signal may be triggered by a respective first control signal and each fourth control signal may be triggered by a respective second control signal.

[00100] The charge sensing stage 502 may be similar to the charge sensing stage 302 shown in FIG. 3A and may include an amplifier 510 having a first input (inverting input), a second input (non-inverting input) and an output. The charge sensing stage 502 may also include a feedback capacitor 512 (C_f) having a first end coupled to the first input (inverting input) of the amplifier 510 and a second end coupled to the output of the amplifier 510. The charge sensing stage 502 may further include a reset switch mechanism 514 coupled in parallel to the feedback capacitor 512. The reset switch mechanism 514 may include reset switch. The reset switch 514 may be controlled by the reset signal Φ_1 .

[00101] Each input switching mechanism may be coupled to or may include a first input capacitor C_{1s} and a second input capacitor C_{2s} connected in series. A node between the first input capacitor C_{1s} and the second input capacitor C_{2s} may be coupled to the charge sensing stage 502. For instance, input switching mechanism 530a may be coupled to or may include a first input capacitor 516a and a second input capacitor 516b (which are connected in series). Node 518a between first input capacitor 516a and second input capacitor 516b may be coupled to the charge sensing stage 502. Further input switching mechanism 530b may be coupled to or may include a further first input capacitor 516c and a further second input capacitor 516d (which are connected in series). A further node 518b between further first input capacitor 516c and further second input capacitor 516d may be coupled to the charge sensing stage 502. Other input switching mechanism 530c may be coupled to or may

include an other first input capacitor 516e and another second input capacitor 516f (which are connected in series). Another node 518c between the other first input capacitor 516e and the other second input capacitor 516f may be coupled to the charge sensing stage 502.

[00102] In general, each input switching mechanism may be coupled to or may include a respective first input capacitor and a respective second input capacitor (which are connected in series). A respective node between the respective first input capacitor and the respective second input capacitor may be coupled to the charge sensing stage 502.

[00103] Each input switching mechanism may be configured to provide the respective first charge signal to the charge sensing stage 502. Each input switching mechanism may be configured to apply the respective first capacitor and the respective second capacitor with a respective first potential difference when the respective first control signal is applied so that the respective first potential difference charges up the respective first input capacitor and the respective second input capacitor to provide the respective first charge signal.

[00104] Each input switching mechanism may be configured to provide the respective second charge signal to the charge sensing stage 502. Each input switching mechanism may be configured to apply the respective first capacitor and the respective second capacitor with a respective second potential difference when the respective second control signal is applied so that the respective second potential difference charges up the respective first input capacitor and the respective second input capacitor to provide the respective second charge signal.

[00105] The respective first potential difference and the respective second potential difference have the same magnitude but may be in opposing directions. The input stage 504 may include or may be configured to be coupled to a first reference voltage ($V_{\text{ref}+}$) and a second reference voltage ($V_{\text{ref}-}$) to supply the respective first potential difference and the respective second potential difference. Both the first reference

voltage and the second reference voltage may be coupled via each switching mechanism to the respective first capacitor and the respective second capacitor.

[00106] Each output switching mechanism may include a respective first sample and hold circuit and a respective second sample and hold circuit. Output mechanism 532a may include a first sample and hold circuit 522a and a second sample and hold circuit 522b, further output mechanism 532b may include a further first sample and hold circuit 522c and a further second sample and hold circuit 522d, other output mechanism 532c may include another first sample and hold circuit 522e and another second sample and hold circuit 522f.

[00107] Each respective first sample and hold circuit may include a respective first output switch with a first end coupled to the output of the amplifier 510 and a second end coupled to a respective first output node (similar to FIG. 3A). The respective first sample and hold circuit may also include a respective first output capacitor with a first end be coupled to the respective first output node and a second end coupled or configured to be coupled to ground.

[00108] Likewise, the respective second sample and hold circuit may include a respective second output switch with a first end coupled to the output of the amplifier 510 and a second end coupled to a respective second output node (similar to FIG. 3A). The respective second sample and hold circuit may also include a respective second output capacitor with a first end be coupled to the respective second output node and a second end coupled or configured to be coupled to ground.

[00109] Various embodiments may relate to a multi-channel TMD-CVC. One input switching mechanism and an output switching mechanism corresponding to the input switching mechanism may form one channel.

[00110] FIG. 5B is a graph 500b illustrating the control signals (T_1 , T_2 , T_{1s} , T_{2s} , P_1 , P_2 , P_{1s} , P_{2s} , Q_1 , Q_2 , Q_{1s} , Q_{2s}), enable signals (T_{en} , P_{en} , Q_{en}) and reset signal (Φ_1) applied to the circuit arrangement according to various embodiments. The signals may be for the circuit arrangement illustrated in FIG. 5A. 550 indicates the reset signal

(Φ_1), 552a indicates the enable signal (T_{en}), 552b indicates the first control signal (T_1), 552c indicates the second control signal (T_2), 552d indicates the third control signal (T_{1s}) and 552e indicates the fourth control signal (T_{2s}). 554a indicates the further enable signal (P_{en}), 554b indicates the further first control signal (P_1), 554c indicates the further second control signal (P_2), 554d indicates the further third control signal (P_{1s}) and 554e indicates the further fourth control signal (P_{2s}). 556a indicates the other enable signal (Q_{en}), 556b indicates the other first control signal (Q_1), 556c indicates the other second control signal (Q_2), 556d indicates the other third control signal (Q_{1s}) and 556e indicates the other fourth control signal (Q_{2s}).

[00111] The signals indicated by 550, 552a-552e, 554a-554e, 556a-556e may also include a series of pulses. In other words, the signals 550, 552a-552e, 554a-554e, 556a-556e may include a plurality of logical highs and a plurality of logical lows, one logical high separated from a successive logical high by a logical low. An enable signal applied to each input switching mechanism may have a pulse that covers or extends over a respective pulse of a respective first control signal and a respective pulse of a respective second control signal applied to the particular switching mechanism. In other words, for instance, enable signal 552a may include a pulse with a flat portion that completely contains a pulse of first control signal 552b and a pulse of second control signal 552c. When an enable signal is applied to one enable switching mechanism, the other enable switching mechanisms may not be activated. Similar to the diagrams shown in FIGS. 3B, 4B, a pulse of each third control signal may have a rising edge behind the rising edge of a corresponding or respective first control signal and a falling edge before a falling edge of the corresponding or respective first control signal. One signal may correspond to a further signal when the one signal is based on the further signal or the one signal is triggered by the further signal. In various embodiments, the reset signal may include a first reset pulse between a pulse of the third control signal and a pulse of the fourth control signal and a second reset pulse between the pulse of the fourth control signal and a successive

pulse of the third control signal. Additionally or alternatively, the reset signal may include a first reset pulse between a pulse of the first control signal and a pulse of the second control signal and a second reset pulse between the pulse of the second control signal and a successive pulse of the first control signal.

[00112] FIG. 5C is an illustration 500c showing the operation of a circuit arrangement according to various embodiments. The circuit arrangement may be the circuit arrangement illustrated in FIG. 5A and may involve time-multiplexed control clock. The reset signal 550 (Φ_1) may reset the circuit arrangement by discharging the capacitors 516a – 516f. The reset signal 550 may further reset the op-amp 510. The circuit arrangement may involve two modes of charge transfer. During the first mode, the first control signals 552b, 554b, 556b (T_1 , P_1 , Q_1) may be applied. The third control signals 552d, 554d, 556d (T_{1s} , P_{1s} , Q_{1s}) may be based or derived from the first control signals 552b, 554b, 556b (T_1 , P_1 , Q_1). During the second mode, the second control signal 552c, 554c, 556c (T_2 , P_2 , Q_2) may be applied. The fourth control signals 552e, 554e, 556e (T_{2s} , P_{2s} , Q_{2s}) may be based or derived from the second control signals 552c, 554c, 556c (T_2 , P_2 , Q_2). The first and second output voltages may be detected and the differences between the respective first and second output voltages (ΔV_{o1} , ΔV_{o2} , ΔV_{o3}) may be determined.

[00113] FIG. 6A is a schematic 600a illustrating a circuit arrangement according to various embodiments. The circuit arrangement may include a charge sensing stage 602. The circuit arrangement may also include an input stage 604 coupled to the charge sensing stage 602. The input stage 604 may include a plurality of input switching mechanisms 630a, 630b, 630c, each input switching mechanism configured to provide a respective first charge signal to the charge sensing stage 602 when a respective first control signal (T_1 , P_1 or Q_1), the respective first control signal (T_1 , P_1 or Q_1) including a respective first pulse with a rising edge and a falling edge, is applied to the respective input switching mechanism and to provide a respective second charge signal to the charge sensing stage 602 when a respective second control

signal (T_2 , P_2 or Q_2), the respective second control signal (T_2 , P_2 or Q_2) including a respective second pulse with a rising edge and a falling edge, is applied to the respective input switching mechanism. The circuit arrangement may further include an output stage 606 coupled to the charge sensing stage 604. The output stage 606 may include a plurality of first output nodes. The output stage may further include a plurality of second output nodes. The output stage 606 may additionally include a plurality of output switching mechanisms 632a, 632b, 632c. Each of the output switching mechanisms may be configured to couple the charge sensing stage 602 to a respective first output node when a respective third control signal (T_{1s} , P_{1s} or Q_{1s}) is applied to respective output switching mechanism, the respective third control signal (T_{1s} , P_{1s} or Q_{1s}) including a respective third pulse with a rising edge behind the rising edge of the respective or corresponding first control signal (T_1 , P_1 or Q_1) and a falling edge before the falling edge of the respective or corresponding first control signal (T_1 , P_1 or Q_1); and to couple the charge sensing stage 602 to the respective second output node when a respective fourth control signal (T_{2s} , P_{2s} or Q_{2s}) is applied to the respective output switching mechanism, the respective fourth control signal (T_{2s} , P_{2s} or Q_{2s}) including a respective fourth pulse with a rising edge behind the rising edge of the respective or corresponding second control signal (T_2 , P_2 or Q_2) and a falling edge before the falling edge of the respective or corresponding second control signal (T_2 , P_2 or Q_2).

[00114] The circuit arrangement shown in FIG. 6A may be similar to the circuit arrangement showing 6A but with a common reference voltage instead of two reference voltages. Various embodiments may relate to a multi-channel single reference voltage based TMD-CVC.

[00115] The charge sensing stage 602 may include amplifier 610, feedback capacitor 612 and reset mechanism 614. The input stage 604 may include a plurality of switching mechanisms 630a, 630b, 630c. Each switching mechanism may include a respective first capacitor and a respective second capacitor. A respective node

between the respective first capacitor and the respective second capacitor may be configured to provide the respective first charge signal and/or respective second charge signal to the amplifier stage 602. For instance, switching mechanism 630a may include first capacitor 616a and second capacitor 616b with node 618a between first capacitor 616a and second capacitor 616b, further switching mechanism 630b may include further first capacitor 616c and further second capacitor 616d with further node 618b between further first capacitor 616c and further second capacitor 616d, another switching mechanism 630c may include another first capacitor 616e and another second capacitor 616f with another node 618c between the other first capacitor 616e and the other second capacitor 616f.

[00116] Each input switching mechanism may be configured to provide the respective first charge signal to the charge sensing stage 602. Each input switching mechanism may be configured to apply the respective first capacitor and the respective second capacitor with a respective first potential difference when the respective first control signal is applied so that the respective first potential difference charges up the respective first input capacitor and the respective second input capacitor to provide the respective first charge signal.

[00117] Each input switching mechanism may be configured to provide the respective second charge signal to the charge sensing stage 602. Each input switching mechanism may be configured to apply the respective first capacitor and the respective second capacitor with a respective second potential difference when the respective second control signal is applied so that the respective second potential difference charges up the respective first input capacitor and the respective second input capacitor to provide the respective second charge signal.

[00118] The respective first potential difference and the respective second potential difference have the same magnitude but may be in opposing directions. The input stage 604 may include or may be configured to be coupled to a common reference voltage (V_{ref}) to supply the respective first potential difference and the respective

second potential difference. The common reference voltage may be coupled via each switching mechanism to the respective first capacitor and the respective second capacitor.

[00119] The output stage 606 may be similar to the output stage 506 shown in FIG. 5A. Each output switching mechanism may include a respective first sample and hold circuit and a respective second sample and hold circuit. Output mechanism 632a may include a first sample and hold circuit 622a and a second sample and hold circuit 622b, further output mechanism 632b may include a further first sample and hold circuit 622c and a further second sample and hold circuit 622d, another output mechanism 632c may include another first sample and hold circuit 622e and another second sample and hold circuit 622f.

[00120] FIG. 6B is a graph 600b illustrating the control signals (T_1 , T_2 , T_{1s} , T_{2s} , P_1 , P_2 , P_{1s} , P_{2s} , Q_1 , Q_2 , Q_{1s} , Q_{2s}), enable signals (T_{en} , P_{en} , Q_{en}) and reset signal (Φ_1) applied to the circuit arrangement according to various embodiments. The signals may be for the circuit arrangement illustrated in FIG. 6A. 650 indicates the reset signal (Φ_1), 652a indicates the enable signal (T_{en}), 652b indicates the first control signal (T_1), 652c indicates the second control signal (T_2), 652d indicates the third control signal (T_{1s}) and 652e indicates the fourth control signal (T_{2s}). 654a indicates the further enable signal (P_{en}), 654b indicates the further first control signal (P_1), 654c indicates the further second control signal (P_2), 654d indicates the further third control signal (P_{1s}) and 654e indicates the further fourth control signal (P_{2s}). 656a indicates the other enable signal (Q_{en}), 656b indicates the other first control signal (Q_1), 656c indicates the other second control signal (Q_2), 656d indicates the other third control signal (Q_{1s}) and 656e indicates the other fourth control signal (Q_{2s}).

[00121] The operation of the signals may be similar to that illustrated in FIG. 5B. In various embodiments, the reset signal may include a first reset pulse between a pulse of the third control signal and a pulse of the fourth control signal and a second

reset pulse between the pulse of the fourth control signal and a successive pulse of the third control signal.

[00122] FIG. 6C is an illustration 600c showing the operation of a circuit arrangement according to various embodiments. The circuit arrangement may be the circuit arrangement illustrated in FIG. 6A and may involve time-multiplexed control clock. The operation of the circuit arrangement may be similar to that illustrated in FIG. 5C.

[00123] FIGS. 5A-C and FIGS. 6A-C show that the schemes shown in FIG. 3A-B and FIG. 4A-B may be extended to multi-channel time-multiplexed version. By properly choosing the charge transfer control clocks and enabling clocks, it may be easy to achieve multi-channel time-multiplexed differential output with a single-ended CVC. The channel enabling control clocks can provide the activation between respective sensor and readout circuit whilst isolating other unused sensing elements.

[00124] Various embodiments may relate to a time-multiplexed differential capacitor sampling method for generating a time-multiplexed differential output signal via a single-ended SC-CVC basic circuit structure operating between an input and output time-multiplexed circuit networks. The method may include the steps of: a. reset phase Φ_1 prior to 1st charge transfer phase, b. 1st charge transfer and sample-and-hold the sensor signal during T_1 and $T_{1s} \rightarrow V_{o1}$, c. reset phase Φ_1 prior to 2nd charge transfer phase, d. 2nd charge transfer and sample-and-hold the negated sensor signal during T_2 and $T_{2s} \rightarrow V_{o2}$.

[00125] The output results arising from the two transfer phases may be in differential format. Various embodiments may relate to a multi-rate switched-capacitor design in which the fundamental clock frequency (Φ_1) of the readout circuit is m times faster than that of the multiplexed clock rate.

[00126] The special sample-and-hold sub clock phases, T_{1s} and T_{2s} may be designed to rise up later and fall down earlier than the corresponding charge transfer clock phases T_1 and T_2 to provide glitch-free output signals.

[00127] The time-multiplexed differential capacitance-to-voltage converter (TMD-CVC) may include a differential capacitive sensor, a sampling amplifier, and two sample-and-hold networks.

[00128] The switched-capacitor amplifier may be a single-ended structure.

[00129] The virtual ground node of the SC op-amp is connected to sensor's middle point (between the two input capacitors). The sensing network may inject differential charges to virtual ground node. The single-ended output of the SC op-amp may be sampled by two sensor signal sample-and-hold networks formed by the holding capacitors together with respective switches under the control of the corresponding sub clock signals.

[00130] In various embodiments, a time-multiplexed differential CVC with single reference voltage design may be achieved by arranging the switch networks with the switching periods (T_1 and T_2), the op-amp with a reset phase Φ_1 and two sample-and-hold circuits controlled by respective sub clock phases T_{1s} and T_{2s} . The functioning steps may consist of: e. T_2 and Φ_1 are on, T_{1s} and T_{2s} are off, the capacitor C_{2s} is charged up by the reference voltage V_{ref} , while the capacitor C_{1s} is discharged and the feedback capacitor C_f is reset, f. T_2 and Φ_1 are off, T_1 turns on, the capacitor C_{2s} is discharged while the capacitor C_{1s} is charged up to the reference voltage V_{ref} . By charge conservation theory, a first amount of charge will be transferred to the feedback capacitor C_f and a first output voltage is developed, g. T_{1s} turns on, the output voltage is sampled by the first sample and hold circuit, h. T_{1s} turns off while T_1 is still on, Φ_1 turns on again to reset the feedback capacitor C_f while the capacitor C_{2s} remains discharged and the capacitor C_{1s} remains being charged by the reference voltage V_{ref} , i. T_1 and Φ_1 turn off, T_2 turns on, the capacitor C_{2s} is charged up by the reference voltage V_{ref} , while the capacitor C_{1s} is discharged. By charge conservation theory, a second amount of charge will be transferred to the feedback capacitor C_f and a second output voltage is developed, j. T_{2s} turns on, the second output voltage is sampled by the second sample and hold circuit, k. The process may be repeated again.

[00131] FIG. 7 is a schematic 700 illustrating a method of operating a circuit arrangement. The method may include, in 702, providing a first control signal, the first control signal including a pulse with a rising edge and a falling edge, to an input switching mechanism of an input stage so that the input switching mechanism provides a first charge signal to a charge sensing stage coupled to the input stage. The method may also include, in 704, providing a second control signal, the second control signal including a pulse with a rising edge and a falling edge, to the input switching mechanism of the input stage so that the input switching mechanism provides a second charge signal to the charge sensing stage. The method may further include, in 706, providing a third control signal, the third control signal including a third pulse with a rising edge behind the rising pulse of the first control signal and a falling edge before the falling edge of the first control signal, to an output switching mechanism of an output stage so that the charge sensing stage is coupled to a first output node of the output stage. The method may additionally include, in 708, providing a fourth control signal, the fourth control signal including a fourth pulse with a rising edge behind the rising pulse of the second control signal and a falling edge before the falling edge of the second control signal, to the output switching mechanism of the output stage so that the charge sensing stage is coupled to a second output node of the output stage.

[00132] In other words, a first control signal and a second control signal may determine whether a first charge signal is applied to the charge sensing stage or a second charge signal is applied to the charge sensing stage. When the first control signal having a first pulse, the first pulse including a rising edge and a falling edge, is applied to the input switching mechanism, a first charge signal may be provided to the charge sensing stage. Correspondingly, when a second control signal having a second pulse, the second pulse including a rising edge and a falling edge, is applied to the input switching mechanism, a second charge signal may be provided to the charge sensing stage. Similarly, a third control signal and a fourth control signal may

determine whether a first output node of an output stage may be coupled to the charge sensing stage or whether a second output node of the output stage may be coupled to the charge sensing stage. The first output node may be coupled to the charge sensing stage when the third control signal having a third pulse is applied to the output switching mechanism. The second output node may be coupled to the charge sensing stage when the fourth control signal having a fourth pulse is applied to the output switching mechanism. The third pulse may overlap with the first pulse and may be contained within the duration of the first pulse. The duration of the third pulse may be shorter the duration of the first pulse. The fourth pulse may overlap with the second pulse and may be contained within the duration of the second pulse. The duration of the fourth pulse may be shorter the duration of the second pulse.

[00133] In various embodiments, the first pulse may occur before the second pulse. In various other embodiments, the second pulse may occur before the first pulse.

[00134] The first control signal may include a plurality of first pulses. The durations of the first pulses may be substantially equal to one another. The first pulses may represent a logical high. The first control signal may include a plurality of first troughs between the first pulses. The first troughs may represent a logical low. For instance the first control signal may include a first pulse, a first trough, followed by a further first pulse, a further first trough, and another first pulse.

[00135] Similarly, the second control signal may include a plurality of second pulses. The durations of the second pulses may be substantially equal to one another. The second pulses may represent a logical high. The second control signal may include a plurality of second troughs between the second pulses. The second troughs may represent a logical low. For instance the second control signal may include a second pulse, a second trough, followed by a further second pulse, a further second trough, and another second pulse.

[00136] The third control signal may include a plurality of third pulses. The durations of the third pulses may be substantially equal to one another. The third

pulses may represent a logical high. The third control signal may include a plurality of third troughs between the third pulses. The third troughs may represent a logical low. For instance the third control signal may include a third pulse, a third trough, followed by a further third pulse, a further third trough, and another third pulse.

[00137] Also, the fourth control signal may include a plurality of fourth pulses. The durations of the fourth pulses may be substantially equal to one another. The fourth pulses may represent a logical high. The fourth control signal may include a plurality of fourth troughs between the fourth pulses. The fourth troughs may represent a logical low. For instance the fourth control signal may include a fourth pulse, a fourth trough, followed by a further fourth pulse, a further fourth trough, and another fourth pulse.

[00138] The reset signal may also include a plurality of reset pulses. The durations of the reset pulses may be substantially equal to one another. The reset pulses may represent a logical high. The reset signal may include a plurality of reset troughs between the reset pulses. The reset troughs may represent a logical low. For instance the reset signal may include a reset pulse, a reset trough, followed by a further reset pulse, a further reset trough and another reset pulse.

[00139] In various embodiments, a third pulse may be between a reset pulse and a further reset pulse, and a fourth pulse may be between a further reset pulse and another reset pulse. In various embodiments, a first pulse may be between a reset pulse and a further reset pulse, and a second pulse may be between a further reset pulse and another reset pulse.

[00140] The method may include providing a reset signal to a reset switch mechanism, the reset signal including a reset pulse between the third pulse and the fourth pulse and a further reset pulse between the fourth pulse and a further third pulse. Alternatively or additionally, the reset pulse may be between the first pulse and the second pulse and a further reset pulse may be between the second pulse and a further first pulse.

[00141] In various embodiments, the third control signal may be triggered by the first control signal. In various embodiments, the fourth control signal may be triggered by the second control signal. The third control signal and the fourth control signal may not be synchronous signals.

[00142] Various embodiments relate to a time-multiplexed differential capacitor sampling technique for generating a time-multiplexed differential output signal via a single-ended switched-capacitor amplifier operating between input and output time-multiplexed circuit networks. Each time-multiplexed differential sensing cycle may include two complete reset, charge transfer and sample-and-hold phases. Since the voltage references, $V_{\text{ref}+}$ and $V_{\text{ref}-}$ are interchanged during the second charge transfer phase, the generated output voltage V_{o1} and V_{o2} may be opposite. Therefore, two time-multiplexed differential signals V_{o1} and V_{o2} may be established. In brief, the sequence of the clock signals to control the operation of TMD-CVC may be summarized as follows: (1) reset phase Φ_1 prior to 1st charge transfer phase, (2) 1st charge transfer and sample-and-hold the sensor signal during T_1 and $T_{1s} \rightarrow V_{o1}$, (3) reset phase Φ_1 prior to 2nd charge transfer phase (4) 2nd charge transfer and sample-and-hold the negated sensor signal during T_2 and $T_{2s} \rightarrow V_{o2}$, (5) Repeat the process.

[00143] The special sample-and-hold sub clock, T_{1s} or T_{2s} , which rises up later and falls down earlier than the corresponding single charge transfer clock phase T_1 or T_2 , may be generated to minimize the impact of spikes caused by the charging and discharging actions in CVC. These two control clocks may ensure that the corresponding output signal being sampled to the associated holding capacitor is isolated first prior to the arrival of big spikes for the stated switching transitions. Therefore, the sampled output voltage may be isolated from the effect of these charging and discharging spikes under heavy parasitic capacitances condition.

[00144] This time-multiplexed differential output technique may be realized in a single voltage reference design with identical performance. The multiplexing action may include (i) the two switching periods T_1 and T_2 that involve the connection of

respective switches associated with the sensing capacitors C_{1s} , C_{2s} , (ii) the reset phase of amplifier and (iii) the sample-and-hold process. Contrasting to the differential voltage reference design, each switching period (T_1 or T_2) may embody two clock sequences. They are (i) a sub clock phase either T_{1s} or T_{2s} for corresponding sample-and-hold circuit and (ii) a reset signal Φ_1 for amplifier. A time-multiplexed differential signal may be equally generated. Finally, both of these two time-multiplexed differential output techniques may be extended to multi-channel operation by inserting an extra control switch between each switch network and each virtual ground of sensor readout circuit.

[00145] Methods described herein may further contain analogous features of any device or circuit arrangement described herein. Correspondingly, devices or circuit arrangement described herein may further contain analogous features of any methods described herein.

[00146] While the invention has been particularly shown and described with reference to specific embodiments, it should be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention as defined by the appended claims. The scope of the invention is thus indicated by the appended claims and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced.

CLAIMS

1. A circuit arrangement comprising:

a charge sensing stage;

an input stage coupled to the charge sensing stage, the input stage

comprising:

an input switching mechanism configured to provide a first charge signal to the charge sensing stage when a first control signal, the first control signal comprising a first pulse with a rising edge and a falling edge, is applied to the input switching mechanism and to provide a second charge signal to the charge sensing stage when a second control signal, the second control signal comprising a second pulse with a rising edge and a falling edge, is applied to the input switching mechanism; and

an output stage coupled to the charge sensing stage, the output stage comprising:

a first output node;

a second output node; and

an output switching mechanism configured to couple the charge sensing stage to the first output node when a third control signal is applied to the output switching mechanism, the third control signal comprising a third pulse with a rising edge behind the rising edge of the first control signal and a falling edge before the falling edge of the first control signal; and to couple the charge sensing stage to the second output node when a fourth control signal is applied to the output switching mechanism, the fourth control signal comprising a fourth pulse with a rising edge behind the rising edge of the second control signal and a falling edge before the falling edge of the second control signal.

2. The circuit arrangement according to claim 1,
wherein the charge sensing stage comprises:
an amplifier having a first input, a second input and an output; and
a feedback capacitor having a first end coupled to the first input of the
amplifier and a second end coupled to the output of the amplifier.
3. The circuit arrangement according to claim 2,
wherein the charge sensing stage further comprises:
a reset switch mechanism coupled in parallel to the feedback capacitor.
4. The circuit arrangement according to claim 2 or claim 3,
wherein the second input of the amplifier is configured to be coupled to
ground.
5. The circuit arrangement according to any of claims 2 to 4,
wherein the first input of the amplifier is coupled to the input stage.
6. The circuit arrangement according to any of claims 2 to 5,
wherein the output of the amplifier is coupled to the output stage.
7. The circuit arrangement according to any of claims 1 to 6,
wherein the input stage comprises a first input capacitor and a second input
capacitor connected in series.
8. The circuit arrangement according to any of claims 7,
wherein a node between the first input capacitor and the second input
capacitor is coupled to the charge sensing stage.

9. The circuit arrangement according to claim 8,
wherein the input switching mechanism configured to provide the first charge signal to the charge sensing stage comprises the input switching mechanism configured to apply the first capacitor and the second capacitor with a first potential difference when the first control signal is applied so that the first potential difference charges up the first input capacitor and the second input capacitor to provide the first charge signal; and
wherein the input switching mechanism configured to provide the second charge signal to the charge sensing stage comprises the input switching mechanism configured to apply the first capacitor and the second capacitor with a second potential difference when the second control signal is applied so that the second potential difference charges up the first input capacitor and the second input capacitor to provide the second charge signal.
10. The circuit arrangement according to claim 9,
wherein the first potential difference and the second potential difference are in opposing directions.
11. The circuit arrangement according to claim 9 or claim 10,
wherein the first potential difference and the second potential difference have the same magnitude.
12. The circuit arrangement according to any of claims 9 to 11,
wherein the input stage comprises a first reference voltage and a second reference voltage to supply the first potential difference and the second potential difference.
13. The circuit arrangement according to any of claims 9 to 11,

wherein the input stage comprises a common reference voltage to supply the first potential difference and the second potential difference.

14. The circuit arrangement according to any of claims 1 to 13, the circuit arrangement further comprising:

a first coupling circuit coupling the input stage to the output stage, the first coupling circuit configured to generate the third control signal for the output switching mechanism when the first control signal is applied to the first coupling circuit.

15. The circuit arrangement according to any of claims 1 to 14, the circuit arrangement further comprising:

a second coupling circuit coupling the input stage to the output stage, the second coupling circuit configured to generate the fourth control signal for the output switching mechanism when the second control signal is applied to the second coupling circuit.

16. The circuit arrangement according to any of claims 1 to 15,

wherein the input stage further comprises a further input switching mechanism configured to provide a further first charge signal to the charge sensing stage when a further first control signal, the further first control signal comprising a further first pulse with a rising edge and a falling edge, is applied to the further input switching mechanism and to provide a further second charge signal to the charge sensing stage when a further second control signal, the further second control signal comprising a further second pulse with a rising edge and a falling edge, is applied to the further input switching mechanism; and
wherein the output stage further comprises

a further first output node;
a further second output node; and
a further output switching mechanism configured to couple the charge sensing stage to the further first output node when a further third control signal is applied to the further output switching mechanism, the further third control signal comprising a further third pulse with a rising edge behind the rising edge of the further first control signal and a falling edge before the falling edge of the further first control signal; and to couple the charge sensing stage to the further second output node when a further fourth control signal is applied to the further output switching mechanism, the further fourth control signal comprising a further fourth pulse with a rising edge behind the rising edge of the further second control signal and a falling edge before the falling edge of the further second control signal.

17. The circuit arrangement according to claim 16 further comprising:

an enable switching mechanism coupling the input switching mechanism to the charge sensing stage; and a
further enable switching mechanism coupling the further input switching mechanism to the charge sensing stage.

18. A method of operating a circuit arrangement, the method comprising:

providing a first control signal, the first control signal comprising a pulse with a rising edge and a falling edge, to an input switching mechanism of an input stage so that the input switching mechanism provides a first charge signal to a charge sensing stage coupled to the input stage;
providing a second control signal, the second control signal comprising a pulse with a rising edge and a falling edge, to the input switching mechanism

of the input stage so that the input switching mechanism provides a second charge signal to the charge sensing stage;

providing a third control signal, the third control signal comprising a third pulse with a rising edge behind the rising pulse of the first control signal and a falling edge before the falling edge of the first control signal, to an output switching mechanism of an output stage so that the charge sensing stage is coupled to a first output node of the output stage; and

providing a fourth control signal, the fourth control signal comprising a fourth pulse with a rising edge behind the rising pulse of the second control signal and a falling edge before the falling edge of the second control signal, to the output switching mechanism of the output stage so that the charge sensing stage is coupled to a second output node of the output stage.

19. The method according to claim 18, the method further comprising:

providing a reset signal to a reset switch mechanism, the reset signal comprising a reset pulse between the third pulse and the fourth pulse and a further reset pulse between the fourth pulse and a further third pulse.

20. The method according to claim 18 or claim 19,

wherein the third control signal is triggered by the first control signal and the fourth control signal is triggered by the second control signal.