Description

Background of the Invention

This invention relates, in general, to semiconductor devices, and more particularly to a method of fabricating a semiconductor device which has vertical transistors and a self-aligned buried oxide region.

The advantages of an oxide isolated bipolar integrated circuit structure are well recognized, and include, in particular, increased circuit operating speed and increased packing density. In such a structure, isolation between adjacent devices is provided by an insulating oxide which extends through the epitaxial layer to the underlying substrate. Devices are thus isolated on the edge by the oxide and on the bottom by the PN junction between the epitaxial layer and the substrate. To fully realize the optimum in packing density, device contact areas must be self-aligned since otherwise valuable space must be expended to provide for possible misalignment tolerances.

However, the above structure is limited in the speed of the device due to parasitics such as base-collector capacitance and base resistance. A need therefore existed for a device structure and a method for its fabrication which would reduce such speed-limiting parasitic time constants while maintaining optimum packing density and isolation.

Summary of the Invention

Accordingly, it is an object of the present invention to provide an improved method for manufacturing a semiconductor device.

Another object of the present invention is to provide a method to increase the operating speed of an integrated circuit.

It is an additional object of the present invention to provide an improved method to manufacture an integrated circuit with low base-collector capacitance.

Yet a further object of the present invention is to provide a process for minimizing the size of the inactive device region in a vertical or lateral transistor.

The foregoing and other objects and advantages are achieved in the present invention which, as part thereof, makes use of a method for fabricating self-aligned, buried oxide integrated circuit devices as defined in the claims. The self-aligned, buried oxide is provided between an electrode region of a transistor and the integrated circuit substrate. This reduces parasitic capacitance of the transistor. The depth or thickness of the silicon in the electrode region is then built up to reduce the resistance of the electrode region. Use of the buried oxide provides a means for down-scaling or shrinking of the active device region which in turn increases the speed of the device.

A more complete understanding of the present invention along with further advantages thereof can be attained from the following detailed description in conjunction with the accompanying drawings.

Brief Description of the Drawings

FIG. 1 illustrates a sectional view of a portion of a semiconductor device found in the prior art;
FIG. 2 illustrates the sectional view of FIG. 1 with the intrinsic, extrinsic and parasitic regions illustrated;
FIGS. 3-10 illustrate, in sectional views, process steps for fabrication of an integrated bipolar transistor in accordance with one embodiment of the invention;
FIG. 11 illustrates a sectional view of an alternate embodiment; and
FIGS. 12-14 illustrate a sectional view of still another embodiment.

Detailed Description of the Drawings

FIG. 1 illustrates a sectional view of a portion of a semiconductor device found in the prior art. The device is an NPN transistor which, together with other devices (not shown), form a portion of a monolithic integrated circuit. The semiconductor device is fabricated with N-type buried layer 21 diffused into P-type silicon substrate 20. The device is isolated from adjacent devices by isolating oxide 23 and on the bottom by a PN junction formed between buried layer 21 and substrate 20. The device includes base 24, base enhancement 19, emitter 26, and deep N+ collector contact 27, which are isolated from each other at the device surface by oxide spacers 25. These device electrodes are located in N-type epitaxial layer 22. Base 24 is doped with boron (P) while base enhancement 19 is heavily doped with boron (P+).

FIG. 2 illustrates the same sectional view found in FIG. 1 except that the intrinsic, extrinsic and parasitic regions are illustrated. Base-collector capacitance 28 and base resistance 29, both parasitics, are formed when a P type region, base 24, is diffused into an N-type region such as epitaxial layer 22. Area 50 is designated the active or the intrinsic device region with area 52 being the intrinsic base. Area 51 is the extrinsic base. The extrinsic base does not contribute directly to the transistor action, but does provide contact to the intrinsic base as well as adding undesired capacitance and resistance to the device.

In the present invention, the structure described in FIGS. 1 and 2 is improved by minimizing

the size of both active device 50 and extrinsic base 51, and lowering the values for base-collector capacitance 28 as will be more apparent hereinafter.

FIGS. 3-10 illustrate process steps followed in accordance with one embodiment of the invention for the fabrication of an improved vertical NPN integrated circuit transistor. As illustrated in FIG. 10, for example, the finished transistor includes a buried oxide that is self aligned to the emitter region to reduce base to collector capacitance, and additional silicon is added above the buried oxide region to insure that the extrinsic base region has a low resistance.

FIG. 3 illustrates a sectional view of a portion of a integrated circuit NPN transistor fabricated in accordance with the present invention. In this embodiment a silicon substrate 20 has been provided with a buried layer region 33. Overlying the substrate 20 and buried layer 33 is an epitaxial layer 34. While an integrated circuit substrate would contain a large plurality of such isolated epitaxial regions, only one such region is shown in FIGS. 3-14 as one such region is sufficient to demonstrate the practice of the invention. In a preferred embodiment of the present invention, epitaxial layer 34 will be used for the fabrication of a bipolar transistor which will likely be one of many in an integrated circuit structure. In this example, the substrate 20 is P-type, and the buried layer region 33 is heavily doped N-type. The epitaxial region 34 is, for example, 1.5 micrometers in thickness and doped to about 0.4 ohm centimeter N-type. This structure also includes oxide isolation regions 23 which isolate the structure from adjacent devices. The process used to achieve the structure thus described is well known in the semiconductor art, and hence will not be further described.

To continue with the fabrication of the structure described hereinbefore, an oxide layer 30 of approximately 70 nanometers (nm), for example, is formed over epitaxial layer 34 and isolation oxide 23. A nitride layer 31 is deposited over oxide layer 30 and is approximately 100 nm thick. These two layers are used in succeeding etch and implant steps. A plasma oxide 32 of approximately 600 nm thick is deposited over nitride layer 31. Plasma oxide 32 is used as an oxygen implant mask in a subsequent step.

FIG. 4 illustrates a sectional view of the device after the structure has been etched. Using conventional masking and etching techniques known in the art, openings 55 and 56 are formed in plasma oxide 32, nitride layer 31, and oxide layer 30.

FIG. 5 illustrates a sectional view of the device with the addition of a layer of oxide 35. Oxide layer 35 is deposited over plasma oxide 32 and in openings 55 and 56 that were formed in the previous step. Oxide layer 35 is approximately 200 nm thick.

FIG. 6 illustrates a sectional view of the device with the addition of buried oxide 37 and the formation of oxide sidewalls 36. Oxide sidewalls 36 are formed by the unmasked reactive ion etching (R.I.E.) of oxide layer 35. R.I.E. is an anisotropic etch which removes the oxide on the horizontal plane but not on the vertical plane. Oxide sidewalls 36 are used in the preferred embodiment of this invention but it is understood that the use of sidewalls 36 may be optional. Buried oxide 37 is formed by ion implanting oxygen at a dose of 1.2E18 cm^2 and at an energy of 400 KeV. Implanting oxygen into openings 55 and 56 and using plasma oxide 32 and sidewall oxide 36 as a mask to prevent selected areas from being implanted, the oxygen is implanted approximately 200 to 400 nm below the surface of epitaxial layer 34. Buried oxide 37 is approximately 200 to 400 nm thick and is self-aligned to sidewalls 36. Although described in this embodiment as a "buried oxide", region 37 is not limited to just oxide but may include any dielectric which may be formed through implantation. An example would be the implanting of nitrogen to form silicon nitride.

FIG. 7 illustrates a sectional view of the device after epitaxial layer 38 is selectively grown in openings 55 and 56. The epitaxial layer is directly over buried oxide 37 and is approximately 200 nm thick. Epitaxial layer 38 is used to increase the thickness of the extrinsic base region which aids in lowering the base resistance. Boron is then implanted through openings 55 and 56 and is annealed to drive the dopant through epitaxial layer 38 and through that portion of epitaxial layer 34 that is above buried oxide 37. The implant region between epitaxial layer 38 and buried oxide 37 is designated by reference number 39 and now has a sheet resistance of <200 ohms per square and a junction depth of 0.3± 0.1 micrometres. This boron implant (P+) is analogous to base enhancement 19 found in FIGS. 1-2. The combination of implanted doped epitaxial layer 38 and region 39 is referred to as the extrinsic base region which is designated in FIGS. 9-10 by reference number 58.

FIG. 8 illustrates a sectional view of the device after a reactive ion etch and the implantation of dopants into the emitter and collector regions. Plasma oxide 32 and portions, but not all, of oxide sidewall 36 are removed using standard reactive ion etching techniques. An oxide layer 40 approximately 200 nm thick is selectively grown over epitaxial layer 38 to protect layer 38 and to provide dielectric isolation.

The remainder of nitride layer 31 is then removed from the structure by etching while oxide layer 40 protects the surface of epitaxial layer 38. Boron (P-) is implanted through oxide layer 30 into selected regions to form intrinsic base 59. Oxide

layer 30 is removed and arsenic (N) is then implanted to form emitter 41 and collector 42. To form deep collector contact 43 phosphorus (N+) is implanted into collector 42. An anneal step is necessary after the implants in order to drive in the dopants and to repair any crystal damage that may have occurred during implantation. The anneal comprises a heat treatment at 1040°C for 20 minutes. A photoresist mask is used when only selected regions of the device are to be implanted. After anneal, emitter region 41 has a sheet resistance of approximately 25± 25% ohms per square and a junction depth of 0.25 ±.05 micrometres and deep collector 43 has a sheet resistance of approximately 30 ohms per square and a junction depth of 1.3 ±.2 micrometres. Intrinsic base 59 has a sheet resistance of approximately 500±.10% ohms per square and a junction depth of 0.35± 0.1 micrometres.

FIG. 9 illustrates a sectional view of the completed device with the addition of metal contacts 44 over extrinsic base, emitter and collector regions 58, 41, and 42 respectively. Metal contact 44 is formed by depositing a layer of approximately 650 to 850 nm of copper and silicon doped aluminum, for example, over the device and using conventional masking and etching techniques known in the art.

FIG. 10 illustrates the same sectional view found in FIG. 9 except that intrinsic, extrinsic and parasitic regions of the invention are illustrated. Area 57 is considered the active device or the intrinsic region and area 58 is the extrinsic base with area 59 being the intrinsic base. The parasitics of this device are illustrated as base-collector capacitance 53 and base resistance 54.

In comparing FIG. 10 with FIG. 2 of the prior art, it is apparent that extrinsic base 58 of FIG. 10 is smaller than the extrinsic base found in FIG. 2. It is also apparent that the base-collector capacitance and the base resistance found in FIG. 10 would have lower values than what is found in FIG. 2. Base-collector capacitance 53 is reduced due to buried oxide 37, which is self-aligned to the emitter region, and base resistance 54 is reduced due to both the highly doped (low resistance) of the extrinsic base and the additional epitaxial layer 38 which increases the thickness of the extrinsic base.

Improvements of implanted transistors with a polysilicon emitter have been well documented. Some of these improvements include lower emitter-base capacitance, higher current gain due to better emitter performance, and improved emitter-base breakdown characteristics. FIG. 11 illustrates a sectional view of an alternate embodiment of an integrated NPN transistor in accordance with the present invention which incorporates the improvements of the polysilicon emitter. In this FIG. 11 embodiment, and referring back to the structure illustrated in FIG. 3, a polysilicon layer of approximately 250 nm is applied over the device prior to oxide layer 30. Basically, all of the implants and etching steps that have been described hereinbefore are the same except that a polysilicon emitter 45 is formed over intrinsic base 59 from the previously deposited polysilicon layer. Region 41 is formed and becomes part of the emitter after polysilicon emitter 45 is implanted with a dopant and annealed.

FIGS. 12-14 illustrate sectional views of still another embodiment of the invention to achieve essentially the same structure as shown in FIG. 9. The differences in this embodiment include the use of a polysilicon layer 61 instead of epitaxial layer 38 and the elimination of oxide sidewall 36.

The device illustrated in FIG. 12 is a sectional view of an NPN transistor that is fabricated on a substrate 20 and is isolated from adjacent devices by oxide 23. Included in the device is buried layer 33, epitaxial layer 34, and buried oxide 37. Oxide layer 30 is grown over epitaxial layer 34. Nitride layer 31 is deposited over oxide layer 30 followed by the deposition of a layer of plasma oxide 32. One of the features that is new in this embodiment is the use of a high dose, shallow implantation of boron to form a region 60 in epitaxial layer 34 above buried oxide regions 37. This region 60 serves the same purpose of epitaxial layer 38, which is to lower the resistance in the electrode area of the resulting transistor.

FIG. 13 illustrates a sectional view of the transistor structure with the addition of a layer of polysilicon 61. Polysilicon layer 61 is approximately 300 nm thick with a range of 200 to 400 nm.

After polysilicon layer 61 has been deposited, the device is then annealed at 1000°C for 30 minutes. The anneal causes boron from region 60 to diffuse into epitaxial layer 34 and to stop at buried oxide 37 and also to diffuse into polysilicon 61. The diffused boron doped region that is located within epitaxial layer 34 is designated by reference number 63. The boron doped region that is out diffused into polysilicon layer 61 is designated by reference number 62.

FIG. 14 illustrates a sectional view of the device structure after the undoped polysilicon layer 61 and plasma oxide 32 has been removed. A solution of hot potassium hydroxide (KOH), for example, is used to selectively etch the undoped regions of polysilicon layer 61 leaving boron doped polysilicon areas 62. Plasma oxide 32 is removed and polysilicon 62 is oxidized to convert the remaining doped polysilicon to a silicon dioxide layer. The remainder of the process is the same as what is described in the description of FIGS. 7-9 except for epitaxial layer 38 which has been re-

placed by oxidized polysilicon 62 and the elimination of oxide sidewalls 36. In this embodiment, polysilicon 62 is used to provide additional silicon to the extrinsic base region which in turn will lower the extrinsic base resistance. Also, as in the previous embodiment, the buried oxide region is self-aligned to the emitter region, thereby increasing the packing density of the device and simplifying the manufacturing process.

Thus it is apparent that there has been provided an improved semiconductor device and method for its manufacture which fully meet the objects and advantages set forth above. The resulting device is a vertical transistor having a buried oxide region thereby providing an active device region with minimal area and parasitics with minimized values.

Having thus described the invention, it will be apparent to those skilled in the art that various modifications can be made within the scope of the present invention. For example, changing the ion implantation dopant will change the conductivity type of the device. Instead of a NPN vertical transistor, or a PNP vertical, a PNP lateral transistor could be fabricated. By changing, among other things, the emitter to a gate and dividing the base into a source and drain region, the device structure could become a field-effect transistor.

Claims

1. A method for fabricating self-aligned, buried oxide integrated circuit devices which comprises:

providing a semiconductor substrate (20) having a first epitaxial layer (34) at a surface thereof;

forming an implant mask over selected regions of the first epitaxial layer (34) thereby leaving unmasked regions therein;

implanting oxygen into the unmasked regions of the first epitaxial layer (34) to form a buried oxide region (37) therein;

selectively applying a second epitaxial layer (38) on the first epitaxial layer (34) over the buried oxide region (37);

forming an extrinsic base region (39) by selectively applying conductivity determining impurities into the second epitaxial layer (38);

diffusing the impurities through the second epitaxial layer (38) and the first epitaxial layer (34) down to the buried oxide (37);

forming an intrinsic base region (59) by selectively applying conductivity determining impurities into the first epitaxial layer (34) adjacent to the extrinsic base region (39); and

forming an emitter region (41) by selectively applying conductivity determining impurities into the intrinsic base region (59).

2. A semiconductor device formed on a substrate (20) comprising:

an epitaxial layer (34) formed on the substrate (20);

a buried oxide region (37) formed in a selected region of the epitaxial layer (34);

a first base region (39) formed in the epitaxial layer (34) above the buried oxide region (37) joined by a smaller base region (59) formed adjacent to the large base region (39), the smaller base region (59) not being over a buried oxide region (37);

an additional region (38) formed over the first base region (39) to increase the size of the first base region (39);

an emitter (41) formed in the smaller base region (59); and

the collector (42) being provided by the epitaxial layer (34).

3. A method of fabricating a semiconductor device on a substrate (20), comprising:

forming an epitaxial region (34) over the substrate (20);

forming a buried oxide region (37) in a selected region of the epitaxial region (34);

forming a first base region (39) for the semiconductor device over the buried oxide region (37);

forming a second base region (59) joining the first base region (39) so that the second base region (59) is not over the buried oxide region (37);

forming an emitter (41) in the second base region (59); and

using the epitaxial region (34) as a collector (42).

4. The method of claim 3 further including forming a heavily doped region (33) between the substrate (20) and the the epitaxial region (34).

5. A method for fabricating self-aligned, buried oxide integrated circuit devices which comprises:

providing a semiconductor substrate (20) having an epitaxial layer (34) at a surface thereof;

forming an implant mask over selected regions of the epitaxial layer (34), thereby leaving unmasked regions therein;

implanting oxygen into the unmasked regions of the epitaxial layer (34) to form a buried oxide region (37) therein;

forming an extrinsic base region (63) by selectively applying conductivity determining

placed by oxidized polysilicon 62 and the elimination of oxide sidewalls 36. In this embodiment, polysilicon 62 is used to provide additional silicon to the extrinsic base region which in turn will lower the extrinsic base resistance. Also, as in the previous embodiment, the buried oxide region is self-aligned to the emitter region, thereby increasing the packing density of the device and simplifying the manufacturing process.

Thus it is apparent that there has been provided an improved semiconductor device and method for its manufacture which fully meet the objects and advantages set forth above. The resulting device is a vertical transistor having a buried oxide region thereby providing an active device region with minimal area and parasitics with minimized values.

Having thus described the invention, it will be apparent to those skilled in the art that various modifications can be made within the scope of the present invention. For example, changing the ion implantation dopant will change the conductivity type of the device. Instead of a NPN vertical transistor, or a PNP vertical, a PNP lateral transistor could be fabricated. By changing, among other things, the emitter to a gate and dividing the base into a source and drain region, the device structure could become a field-effect transistor.

Claims

1. A method for fabricating self-aligned, buried oxide integrated circuit devices which comprises:

providing a semiconductor substrate (20) having a first epitaxial layer (34) at a surface thereof;

forming an implant mask over selected regions of the first epitaxial layer (34) thereby leaving unmasked regions therein;

implanting oxygen into the unmasked regions of the first epitaxial layer (34) to form a buried oxide region (37) therein;

selectively applying a second epitaxial layer (38) on the first epitaxial layer (34) over the buried oxide region (37);

forming an extrinsic base region (39) by selectively applying conductivity determining impurities into the second epitaxial layer (38);

diffusing the impurities through the second epitaxial layer (38) and the first epitaxial layer (34) down to the buried oxide (37);

forming an intrinsic base region (59) by selectively applying conductivity determining impurities into the first epitaxial layer (34) adjacent to the extrinsic base region (39); and

forming an emitter region (41) by selectively applying conductivity determining impurities into the intrinsic base region (59).

2. A semiconductor device formed on a substrate (20) comprising:

an epitaxial layer (34) formed on the substrate (20);

a buried oxide region (37) formed in a selected region of the epitaxial layer (34);

a first base region (39) formed in the epitaxial layer (34) above the buried oxide region (37) joined by a smaller base region (59) formed adjacent to the large base region (39), the smaller base region (59) not being over a buried oxide region (37);

an additional region (38) formed over the first base region (39) to increase the size of the first base region (39);

an emitter (41) formed in the smaller base region (59); and

the collector (42) being provided by the epitaxial layer (34).

3. A method of fabricating a semiconductor device on a substrate (20), comprising:

forming an epitaxial region (34) over the substrate (20);

forming a buried oxide region (37) in a selected region of the epitaxial region (34);

forming a first base region (39) for the semiconductor device over the buried oxide region (37);

forming a second base region (59) joining the first base region (39) so that the second base region (59) is not over the buried oxide region (37);

forming an emitter (41) in the second base region (59); and

using the epitaxial region (34) as a collector (42).

4. The method of claim 3 further including forming a heavily doped region (33) between the substrate (20) and the the epitaxial region (34).

5. A method for fabricating self-aligned, buried oxide integrated circuit devices which comprises:

providing a semiconductor substrate (20) having an epitaxial layer (34) at a surface thereof;

forming an implant mask over selected regions of the epitaxial layer (34), thereby leaving unmasked regions therein;

implanting oxygen into the unmasked regions of the epitaxial layer (34) to form a buried oxide region (37) therein;

forming an extrinsic base region (63) by selectively applying conductivity determining

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impurities into the epitaxial layer (34) above the buried oxide region (37);

depositing a layer of polysilicon (61) over the extrinsic base region (63);

diffusing the impurities through the epitaxial layer (34) down to the buried oxide (37), and up through portions of the polysilicon layer (61);

selectively etching an undoped portion of the polysilicon layer (61); and

oxidizing the remaining polysilicon (61) to form a layer of silicon dioxide.

Revendications

1. Procédé de fabrication de dispositifs de circuit intégré à oxyde enterré auto-aligné comprenant:

la fourniture d'un substrat semiconducteur (20) comportant une première couche épitaxiale (34) au niveau d'une de ses surfaces ;

la formation d'un masque d'implantation sur des régions sélectionnées de la première couche épitaxiale (34) en y laissant ainsi des régions non masquées ;

l'implantation d'oxygène à l'intérieur des régions non masquées de la première couche épitaxiale (34) pour y former une région d'oxyde enterré (37) ;

l'application de manière sélective d'une seconde couche épitaxiale (38) sur la première couche épitaxiale (34) au-dessus de la région d'oxyde enterré (37) ;

la formation d'une région de base extrinsèque (39) par application de manière sélective d'impuretés de détermination de conductivité dans la seconde couche épitaxiale (38) ;

la diffusion des impuretés au travers de la seconde couche épitaxiale (38) et de la première couche épitaxiale (34) vers le bas jusqu'à l'oxyde enterré (37) ;

la formation d'une région de base intrinsèque (59) par application de manière sélective d'impuretés de détermination de conductivité dans la première couche épitaxiale (34) qui est adjacente à la région de base extrinsèque (39) ; et

la formation d'une région d'émetteur (41) par application de manière sélective d'impuretés de détermination de conductivité dans la région de base intrinsèque (59).

2. Dispositif à semiconducteur formé sur un substrat (20), comprenant :

une couche épitaxiale (34) formée sur le substrat (20) ;

une région d'oxyde enterré (37) formée dans une région sélectionnée de la couche épitaxiale (34) ;

une première région de base (39) formée dans la couche épitaxiale (34) au-dessus de la région d'oxyde enterré (37), jointe par une petite région de base (59) formée de manière à être adjacente à la grande région de base (39), la région de base plus petite (59) n'étant pas sur une région d'oxyde enterré (37) ;

une région supplémentaire (38) formée sur la première région de base (39) afin d'augmenter la taille de la première région de base (39) ;

un émetteur (41) formé dans la région de base plus petite (59) ; et

le collecteur (42) étant constitué par la couche épitaxiale (34).

3. Procédé de fabrication d'un dispositif à semiconducteur sur un substrat (20), comprenant :

la formation d'une région épitaxiale (34) sur le substrat (20) ;

la formation d'une région d'oxyde enterré (37) dans une région sélectionnée de la région épitaxiale (34) ;

la formation d'une première région de base (39) pour le dispositif à semiconducteur sur la région d'oxyde enterré (37) ;

la formation d'une seconde région de base (59) qui joint la première région de base (39) de telle sorte que la seconde région de base (59) ne soit pas sur la région d'oxyde enterré (37) ;

la formation d'un émetteur (41) dans la seconde région de base (59) ; et

l'utilisation de la région épitaxiale (34) en tant que collecteur (42).

4. Procédé selon la revendication 3, incluant en outre la formation d'une région fortement dopée (33) entre le substrat (20) et la région épitaxiale (34).

5. Procédé de fabrication de dispositifs de circuit intégré à oxyde enterré auto-aligné comprenant:

la fourniture d'un substrat semiconducteur (20) comportant une couche épitaxiale (34) au niveau d'une de ses surfaces ;

la formation d'un masque d'implantation sur des régions sélectionnées de la couche épitaxiale (34) pour ainsi y laisser des régions non masquées ;

l'implantation d'oxygène dans les régions non masquées de la couche épitaxiale (34) pour y former une région d'oxyde enterré (37) ;

la formation d'une région de base extrinsèque (63) en appliquant de manière sélective des impuretés de détermination de conductivi-

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té dans la couche épitaxiale (34) au-dessus de la région d'oxyde enterré (37) ;

le dépôt d'une couche de polysilicium (61) sur la région de base extrinsèque (63) ;

la diffusion des impuretés au travers de la couche épitaxiale (34) vers le bas jusqu'à l'oxyde enterré (37), et vers le haut au travers de parties de la couche de polysilicium (61) ;

la gravure de manière sélective d'une partie non dopée de la couche de polysilicium (61) ; et

l'oxydation du polysilicium restant (61) pour former une couche de dioxide de silicium.

Patentansprüche

1. Verfahren zum Herstellen von selbsausgerichteten, integrierten Schaltkreisvorrichtungen mit vergrabenem Oxyd, welches umfaßt:

Bereitstellen eines Halbleitersubstrats (20) mit einer ersten Epitaxieschicht (34) auf einer seiner Oberflächen;

Formen einer Implantationsmaske über ausgewählten Bereichen der ersten Epitaxieschicht (34), wodurch unmaskierte Bereich darauf belassen werden;

Implantieren von Sauerstoff in die unmaskierten Bereich der ersten Epitaxieschicht (34), um einen vergrabenen Oxydbereich (37) darin zu bilden;

selektives Aufbringen einer zweiten Epitaxieschicht (38) auf die erste Epitaxieschicht (34) über dem vergrabenen Oxydbereich (37);

Bilden eines extrinsischen Basisbereichs (39) durch selektives Einbringen von die Leitfähigkeit bestimmenden Verunreinigungen in die zweite Epitaxieschicht (38);

Diffundieren der Verunreinigungen durch die zweite Epitaxieschicht (38) und die erste Epitaxieschicht (34) hinab bis zum vergrabenen Oxyd (37);

Bilden eines intrinsischen Basisbereichs (59) durch selektives Einbringen von die Leitfähigkeit bestimmenden Verunreinigungen in die erste Epitaxieschicht ((34) neben dem extrinsischen Basisbereich (39); und

Bilden eines Emitterbereichs (41) durch selektives Einbringen von die Leitfähigkeit bestimmenden Verunreinigungen in den intrinsischen Basisbereich (59).

2. Auf einem Substrat (20) geformte Halbleitervorrichtung mit:

einer auf dem Substrat (20) geformten Epitaxieschicht (34);

einem in einem ausgewählten Bereich der Epitaxieschicht (34) geformten vergrabenem Oxydbereich (37);

einer in der Epitaxieschicht (34) über dem vergrabenen Oxydbereich (37) geformten ersten Basisbereich (39), der mit einem kleineren Basisbereich (59) verbunden ist, der neben dem größeren Basisbereich (39) geformt ist, wobei sich der kleinere Basisbereich (59) nicht über einem vergrabenen Oxydbereich (37) befindet;

einem zusätzlichen, über dem ersten Basisbereich (39) gebildeten Bereich (38) zum Vergrößern der Größe des ersten Basisbereichs (39);

einem in dem kleineren Basisbereich (59) geformten Emitter (41); und

wobei der Kollektor (42) durch die Epitaxieschicht (34) gebildet wird.

3. Verfahren zum Herstellen einer Halbleitervorrichtung auf einem Substrat, welches umfaßt:

Bilden eines epitaktischen Bereichs (34) über dem Substrat (20);

Bilden eines vergrabenen Oxydbereichs (37) in einem ausgewählten Bereich des epitaktischen Bereichs (34);

Bilden eines ersten Basisbereichs (39) für die Halbleitervorrichtung über dem vergrabenen Oxydbereich (37);

Bilden eines zweiten Basisbereich (59), der an den ersten Basisbereich (39) angrenzt, so daß sich der zweite Basisbereich (59) nicht über dem vergrabenen Oxydbereich (37) befindet;

Bilden eines Emitters (41) in dem zweiten Basisbereich (59); und

Verwenden des epitaktischen Bereichs (34) als Kollektor (42).

4. Verfahren nach Anspruch 3, das außerdem das Bilden eines stark dotierten Bereichs (33) zwischen dem Substrat (20) und dem epitaktischen Bereich (34) umfaßt.

5. Verfahren zum Herstellen von selbsausgerichteten, integrierten Schaltkreisvorrichtungen mit vergrabenem Oxyd, welches umfaßt:

Bereitstellen eines Halbleitersubstrats (20) mit einer Epitaxieschicht (34) auf einer seiner Oberflächen;

Formen einer Implantationsmaske über ausgewählten Bereichen der Epitaxieschicht (34), wodurch unmaskierte Bereich darauf belassen werden;

Implantieren von Sauerstoff in die unmaskierten Bereich der Epitaxieschicht (34), um einen vergrabenen Oxydbereich (37) darin zu bilden;

Bilden eines extrinsischen Basisbereichs (63) durch selektives Einbringen von die Leitfä-

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higkeit bestimmenden Verunreinigungen in die Epitaxieschicht (34) über dem vergrabenen Oxydbereich (37);

Abscheiden einer Schicht aus Polysilizium (61) über dem extrinsischen Basisbereich (63);

Diffundieren der Verunreinigungen durch die Epitaxieschicht (34) hinab bis zum vergrabenen Oxyd (37) und hinauf durch Teile der Polysiliziumschicht (61);

selektives Ätzen eines undotierten Teils der Polysiliziumschicht (61); und

Oxydieren des verbleibenden Polysiliziums (61), um eine Schicht aus Siliziumdioxyd zu bilden.