

FIG. 1(A)

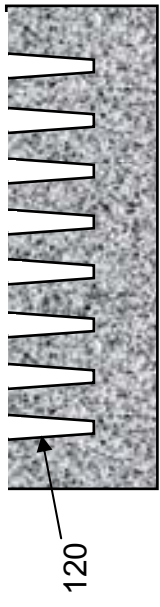


FIG. 1(B)

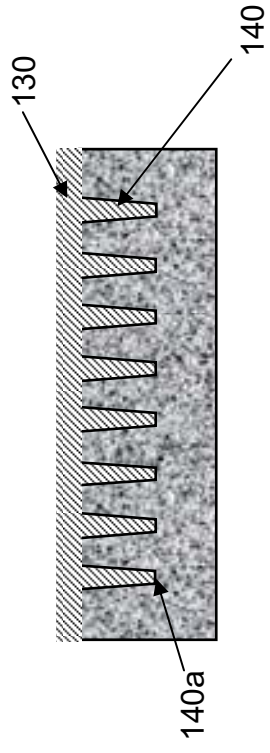


FIG. 1(C)

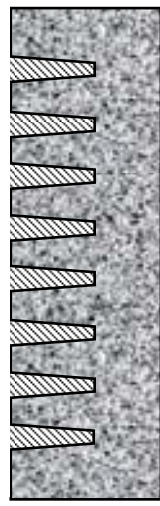


FIG. 1(D)

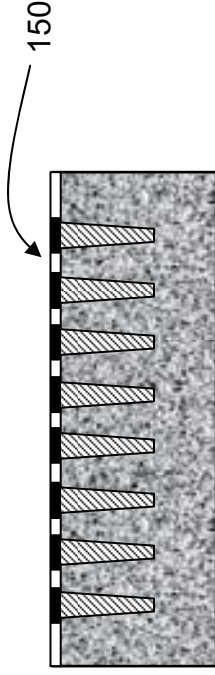
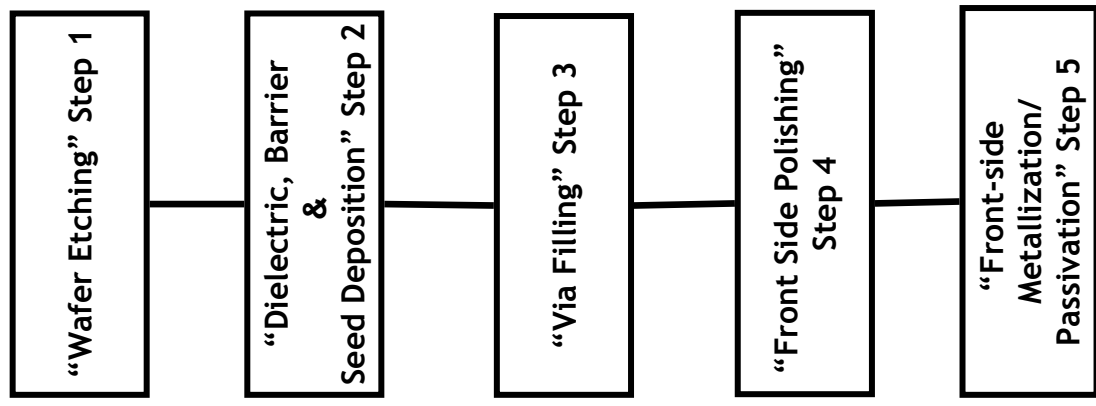


FIG. 1(E)

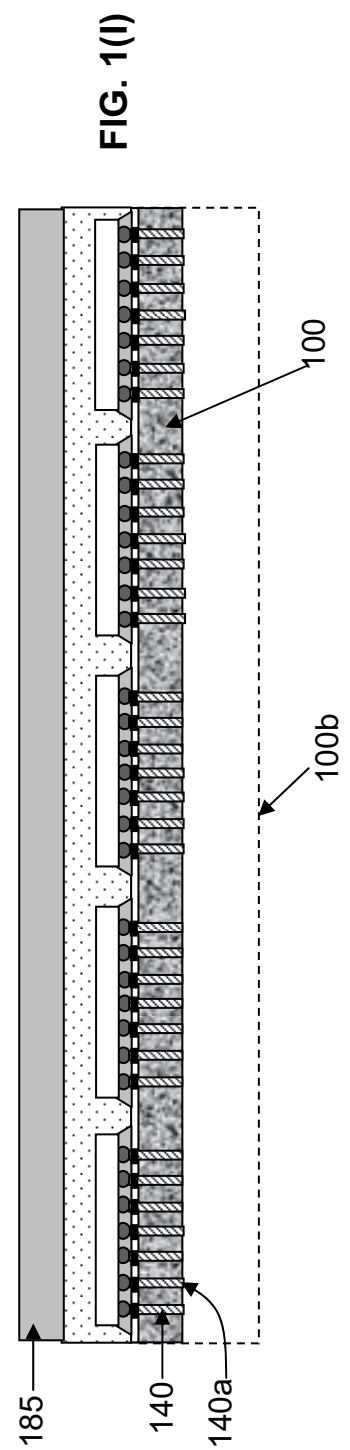
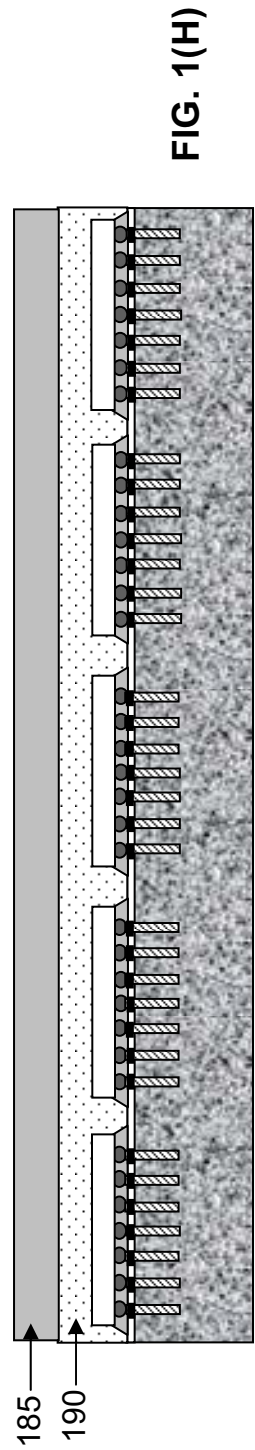
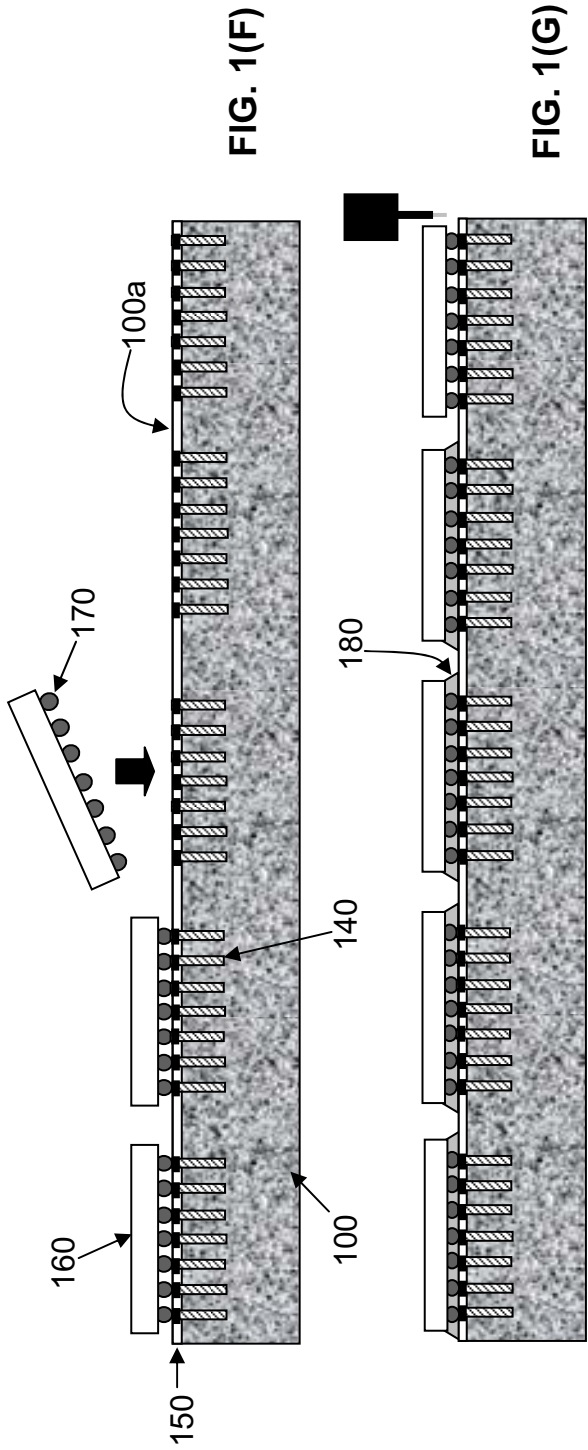


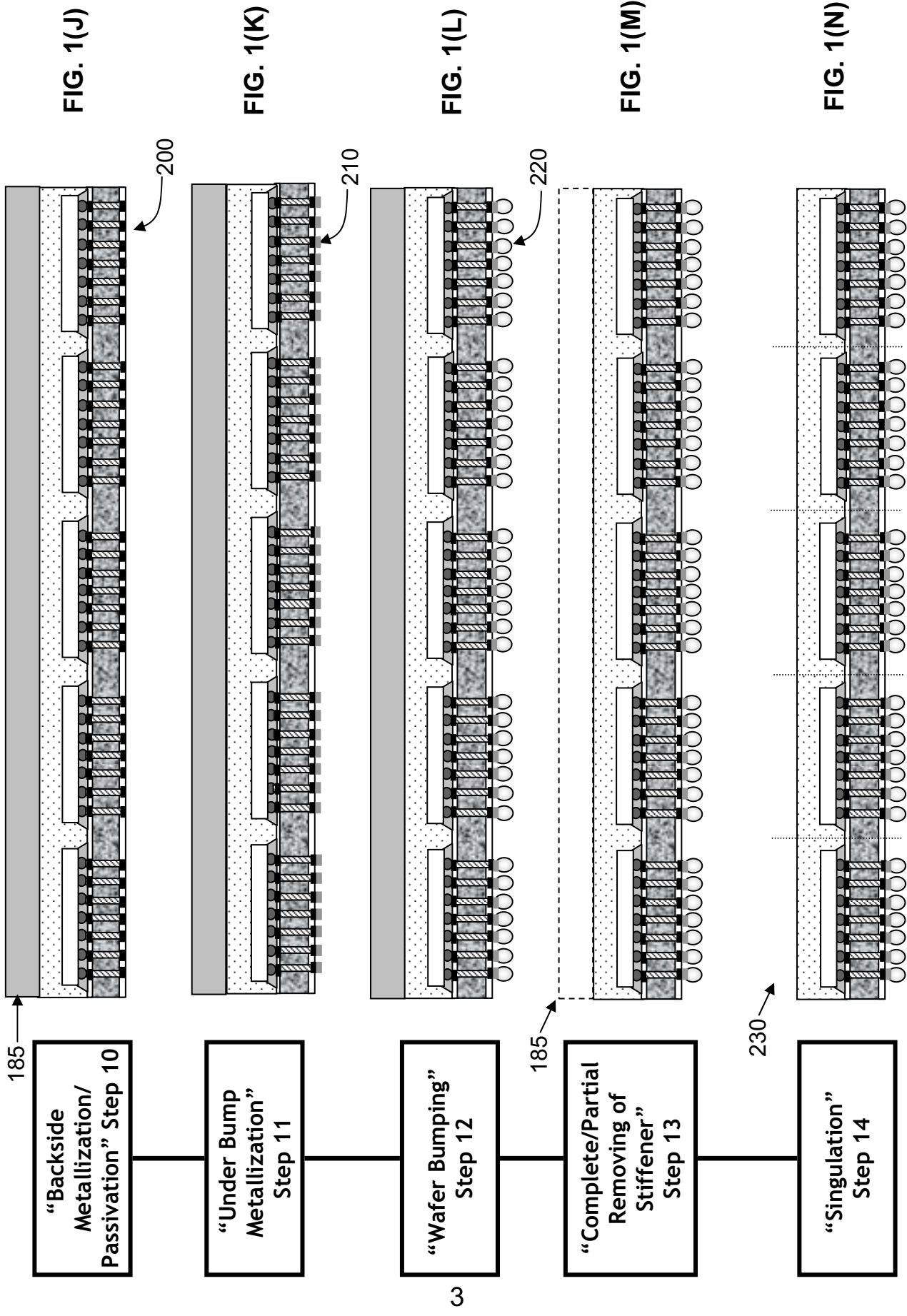
“Chip-to-Wafer
Attachment”
Step 6

“Under-filling”
Step 7

“Wafer Level
Molding”
Step 8

“Wafer Thinning”
Step 9





“Chip-To-Substrate
Attachment
& Under-filling”
or Over-molding”
Step 15

“Solder Ball
Mounting
& Singulation”
Step 16

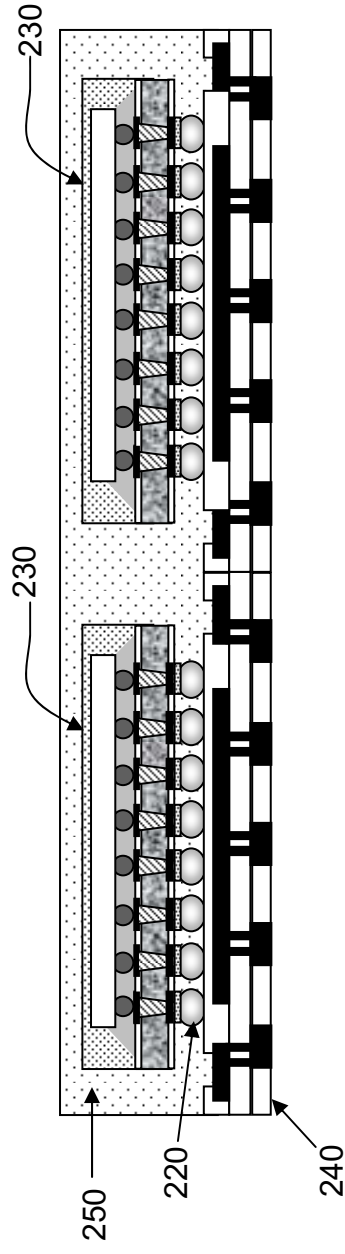


FIG. 1(O)

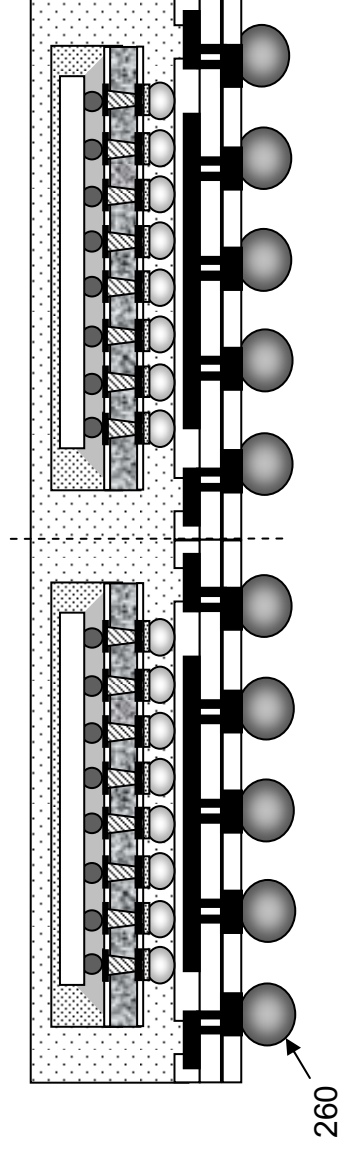


FIG. 1(P)

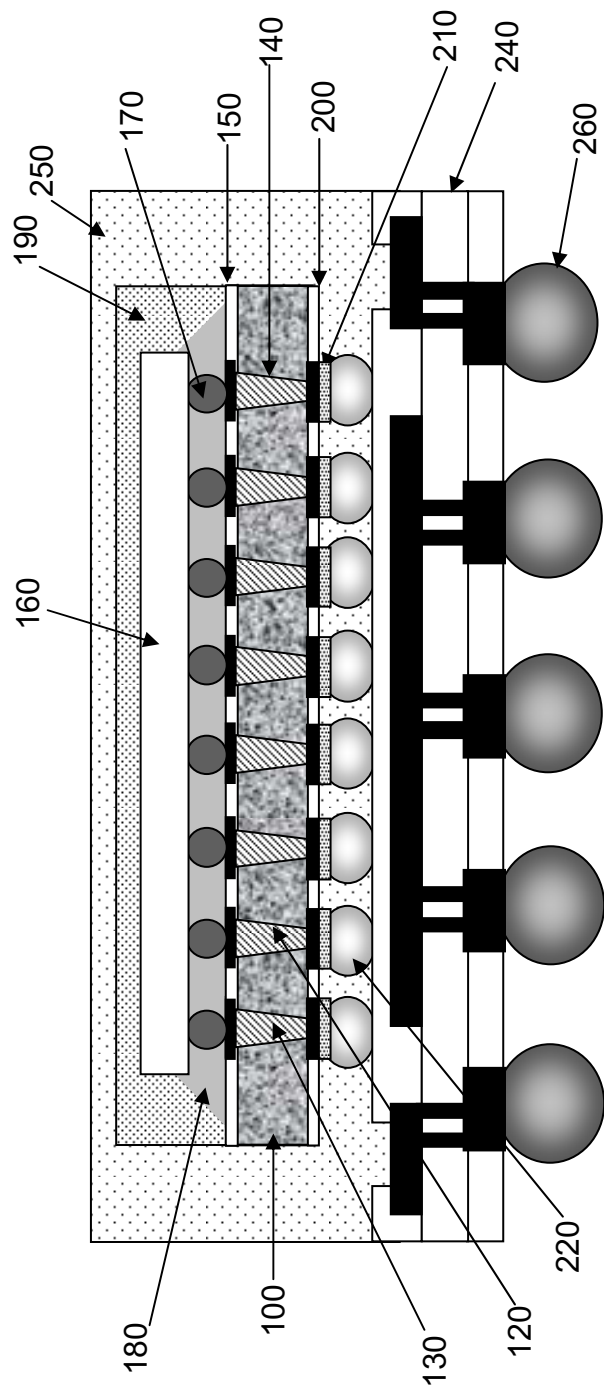


FIG. 2(A)

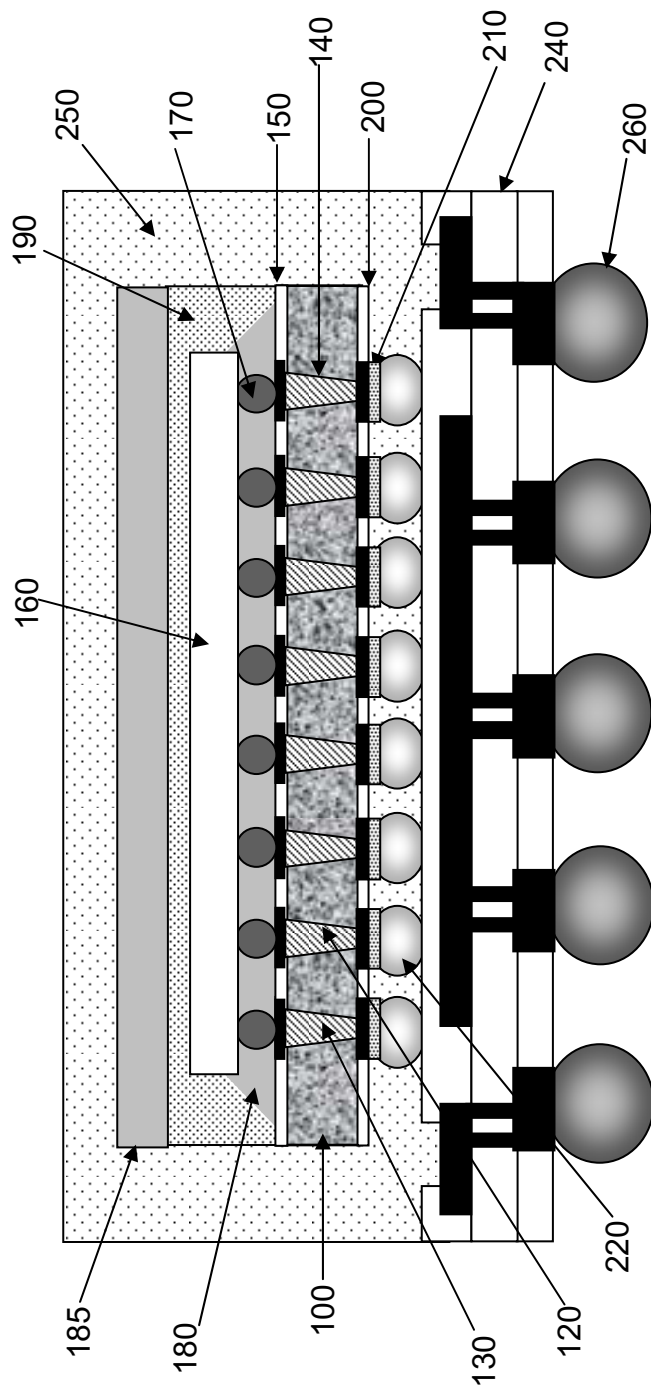


FIG. 2(B)

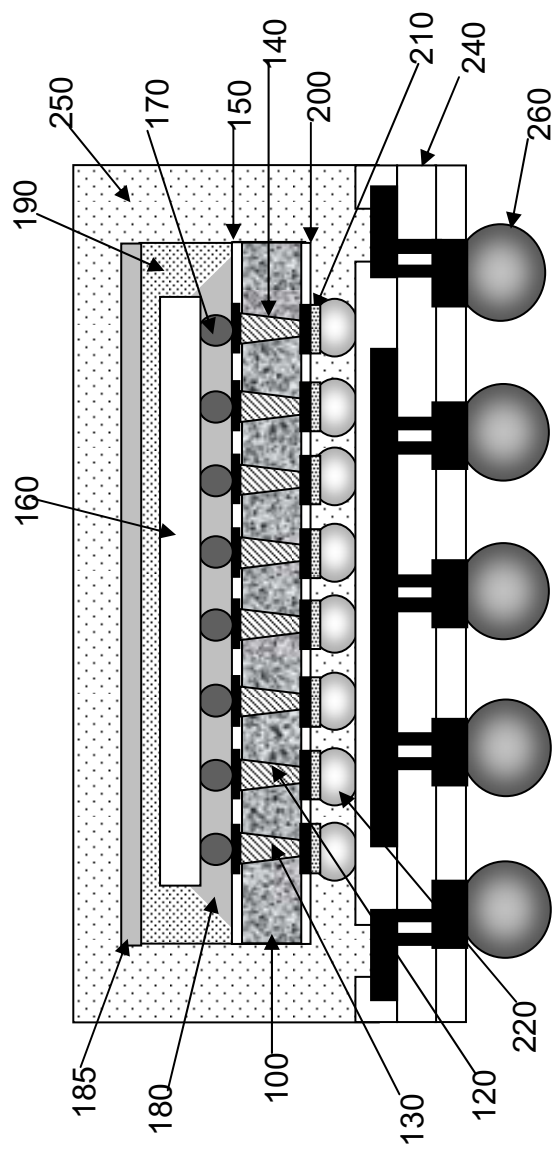


FIG. 2(C)

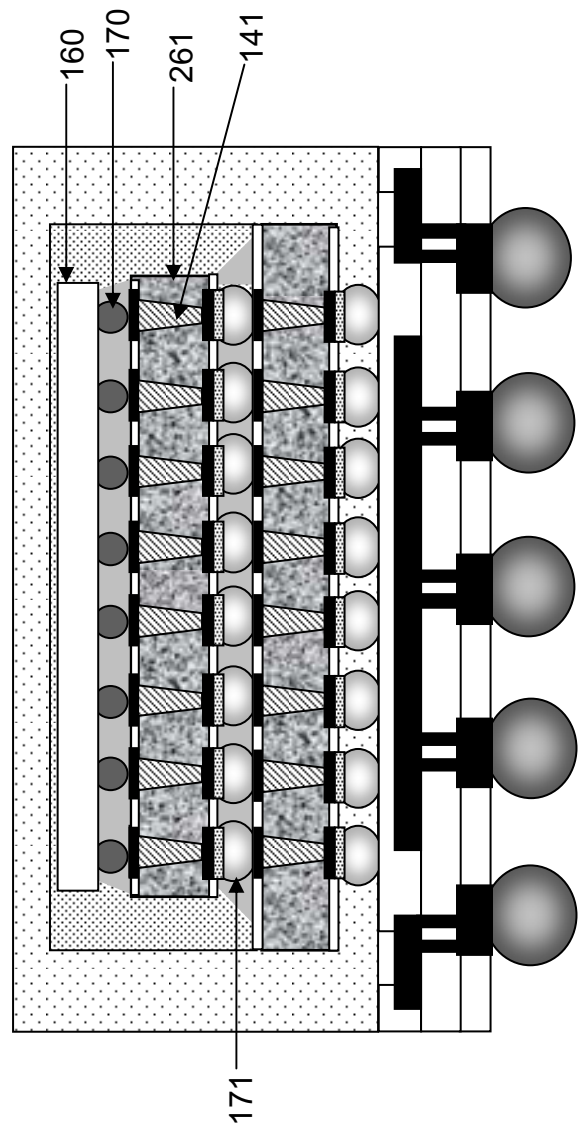


FIG. 2(D)

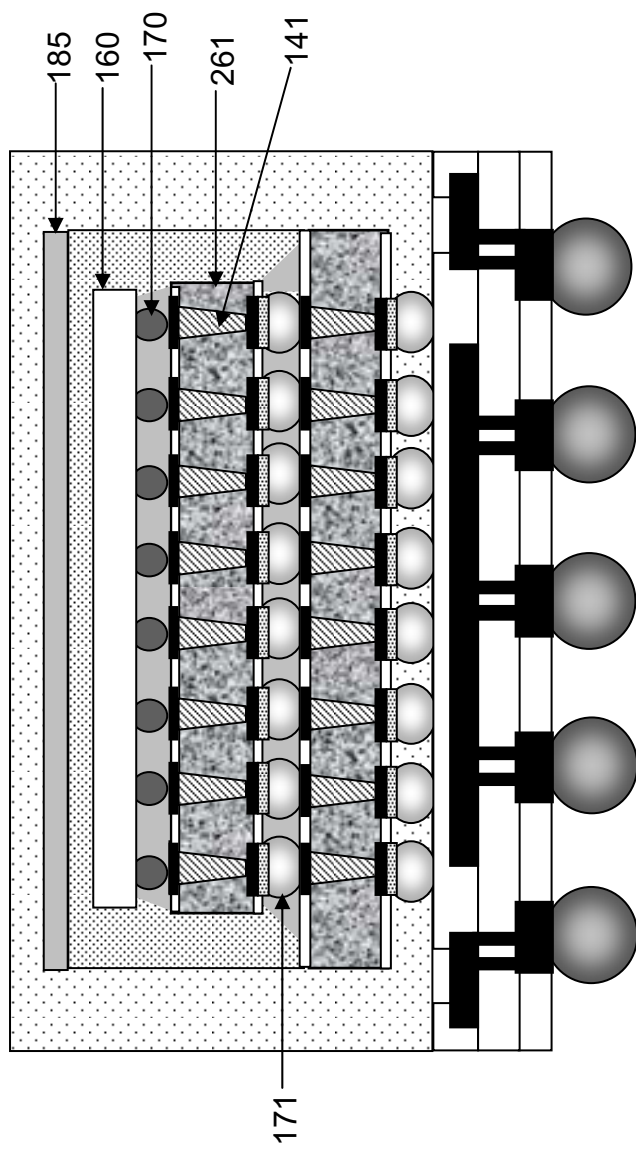


FIG. 2(E)

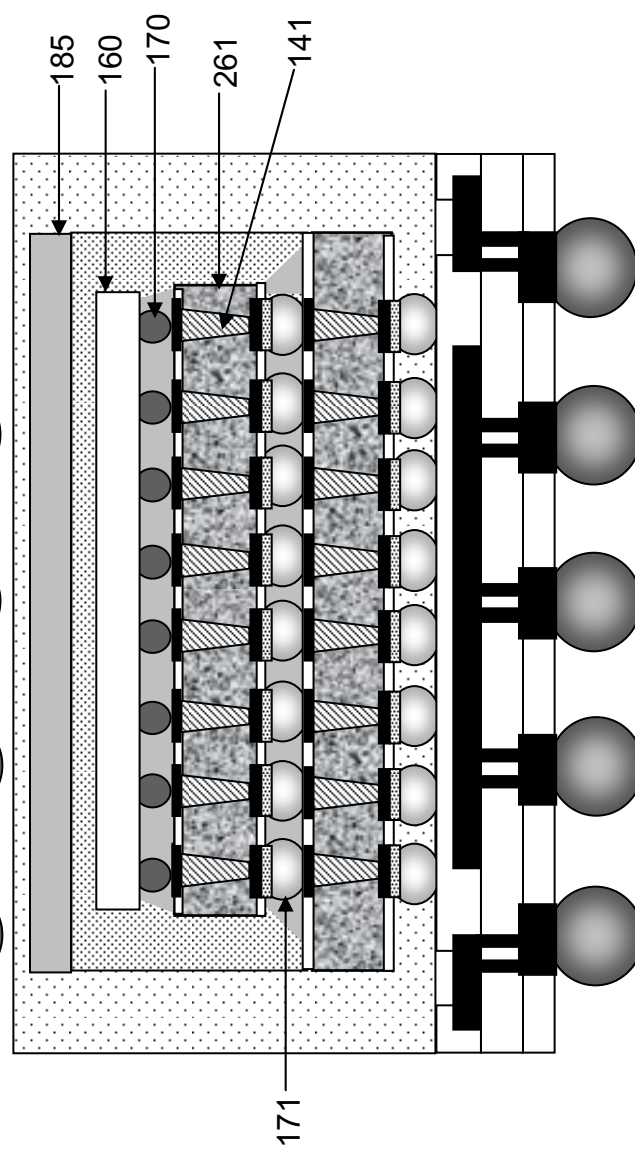


FIG. 2(F)

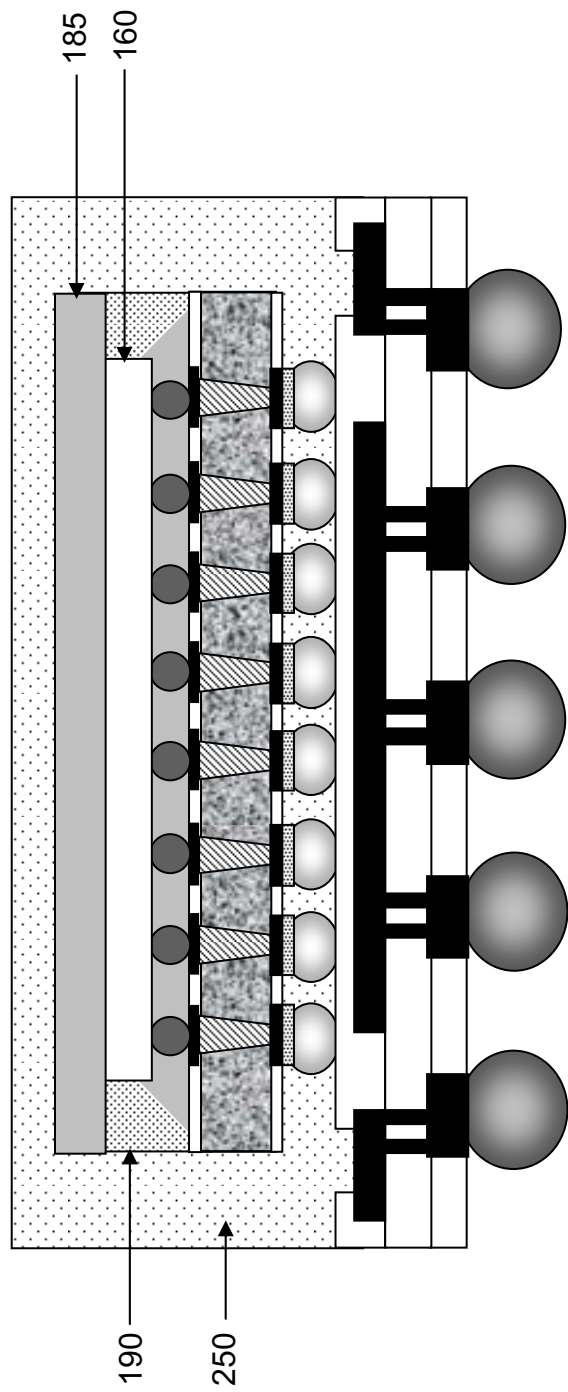


FIG. 2(G)

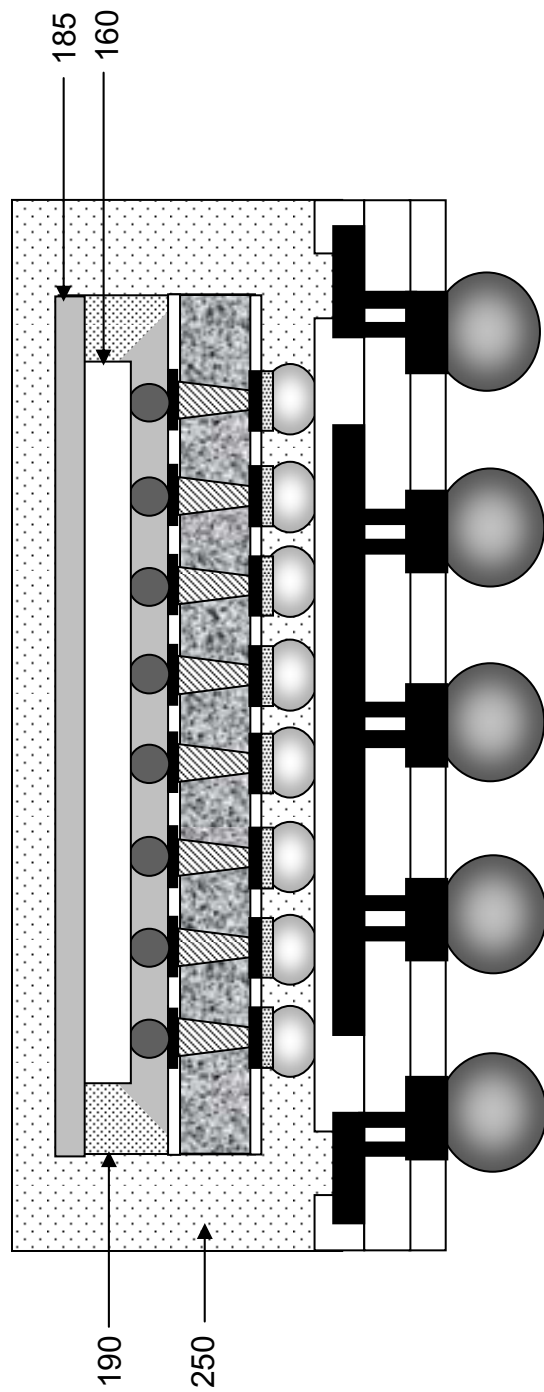


FIG. 2(H)

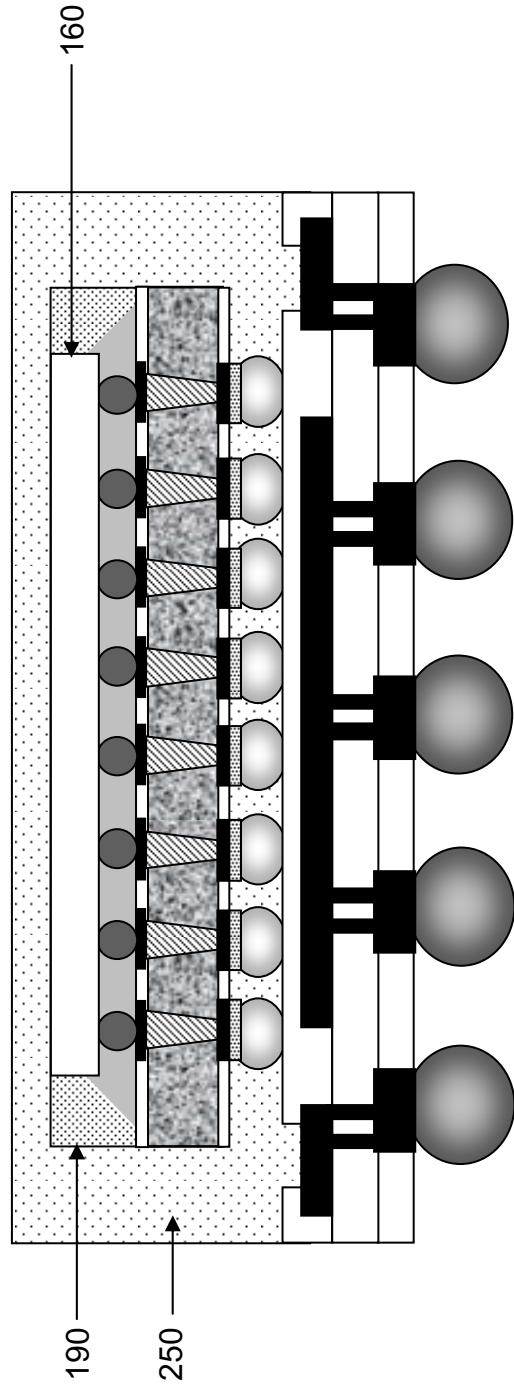


FIG. 2(I)

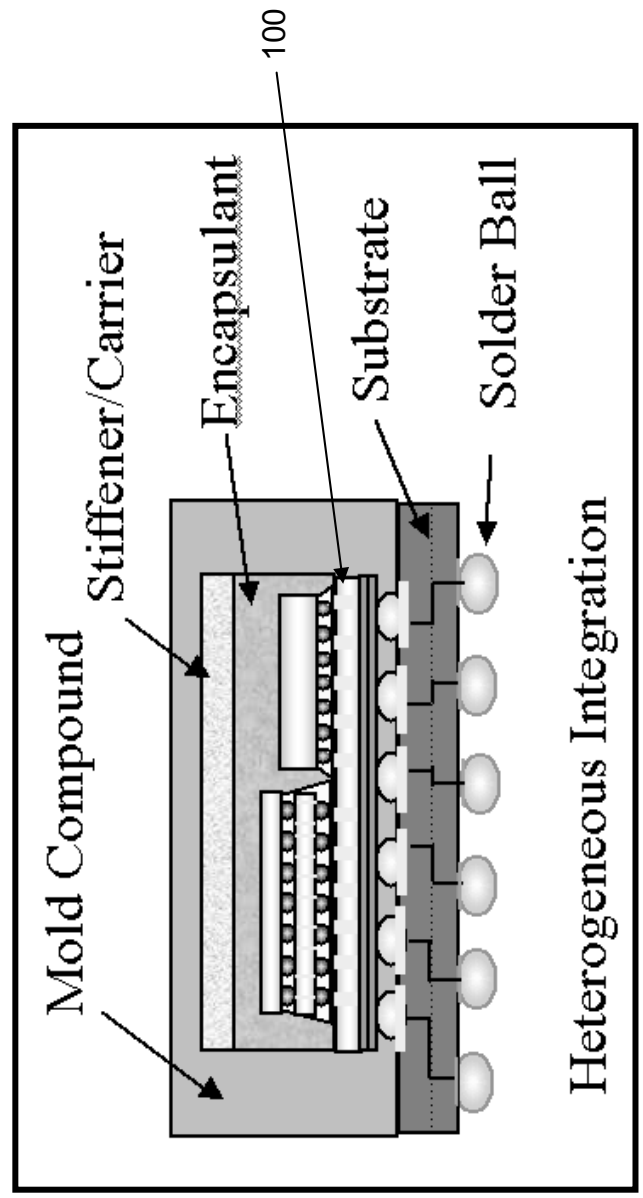


FIG. 2(J)

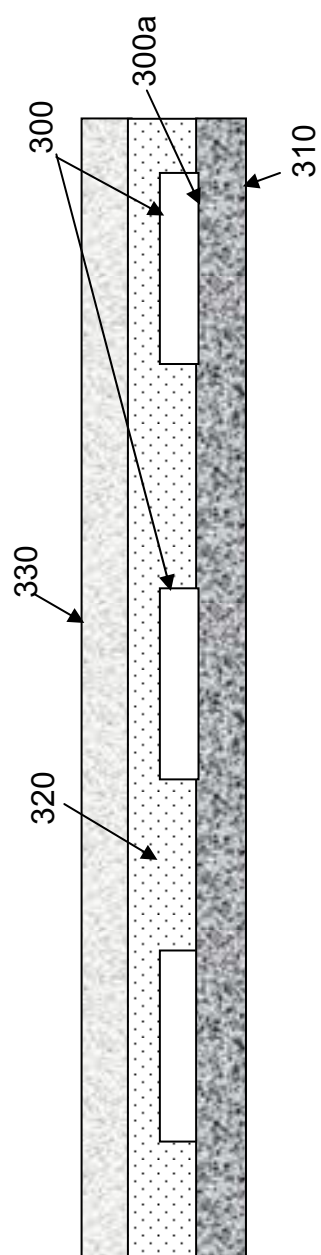


FIG. 3(A)

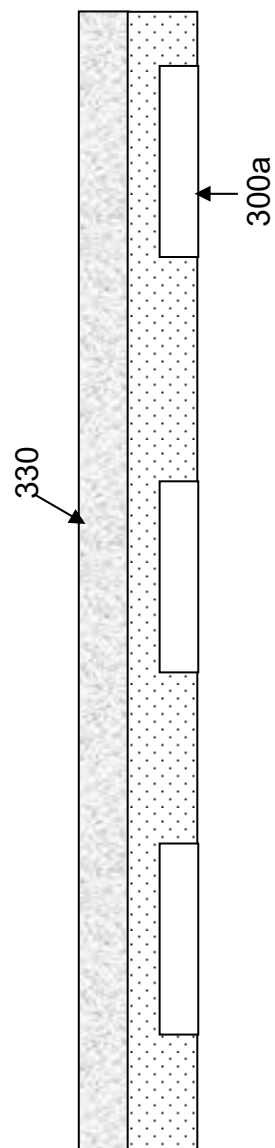


FIG. 3(B)

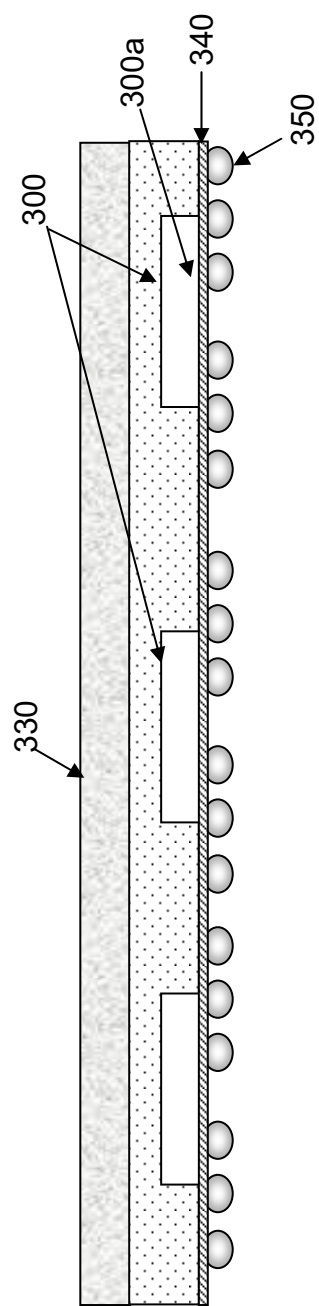


FIG. 3(C)

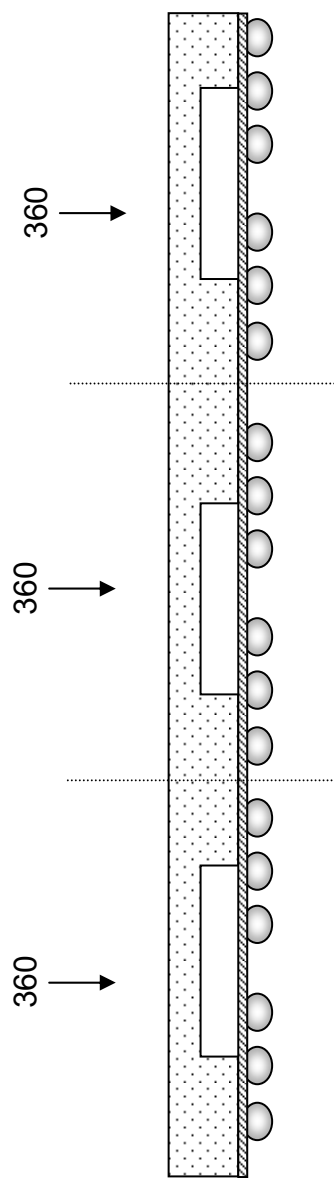


FIG. 3(D)

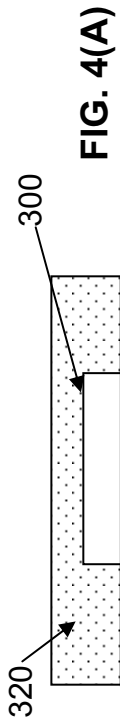


FIG. 4(A)

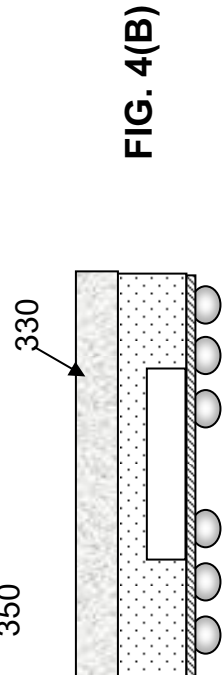


FIG. 4(B)

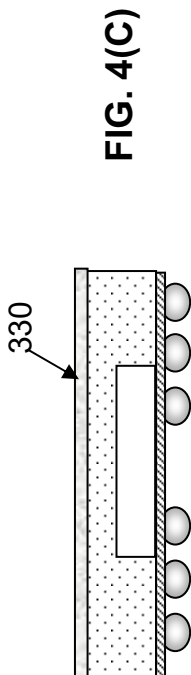


FIG. 4(C)

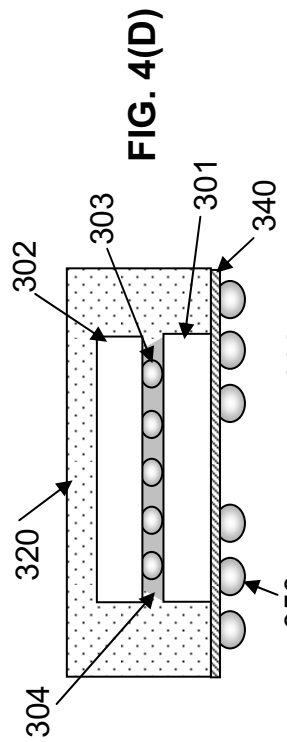


FIG. 4(D)

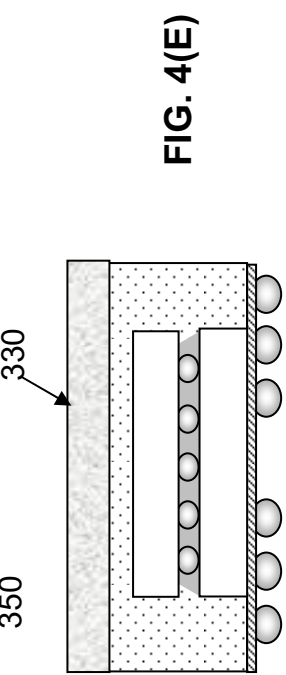


FIG. 4(E)

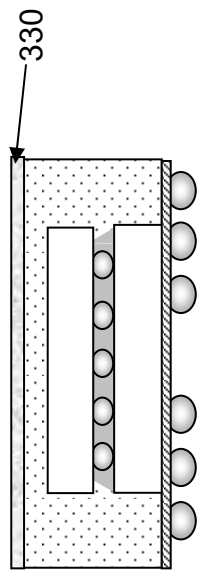


FIG. 4(F)

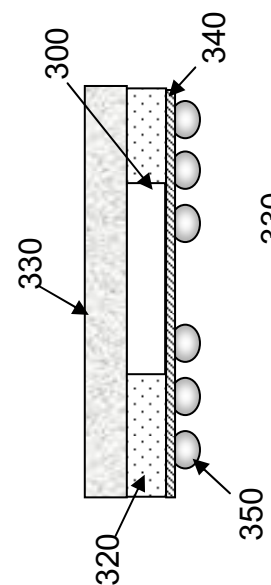


FIG. 4(G)

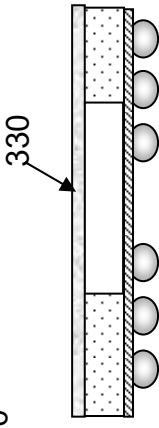


FIG. 4(H)

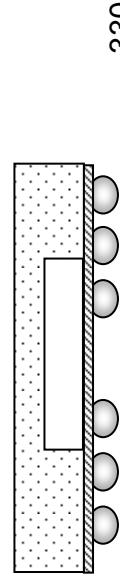


FIG. 4(I)

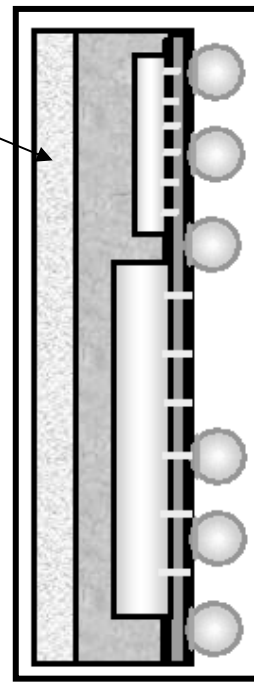
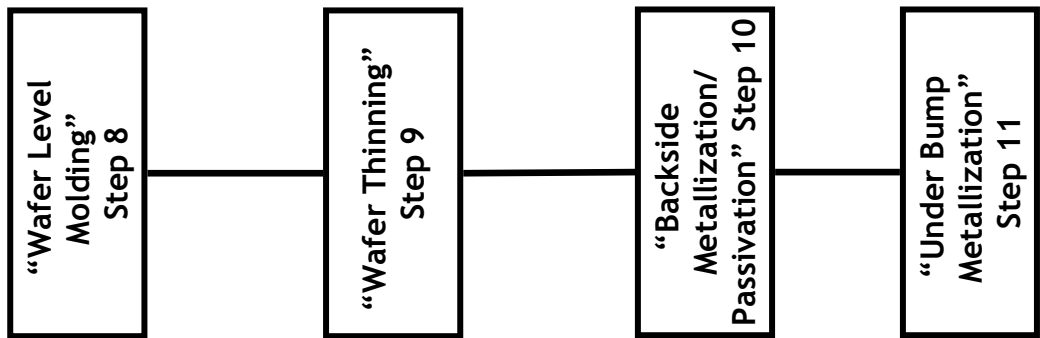
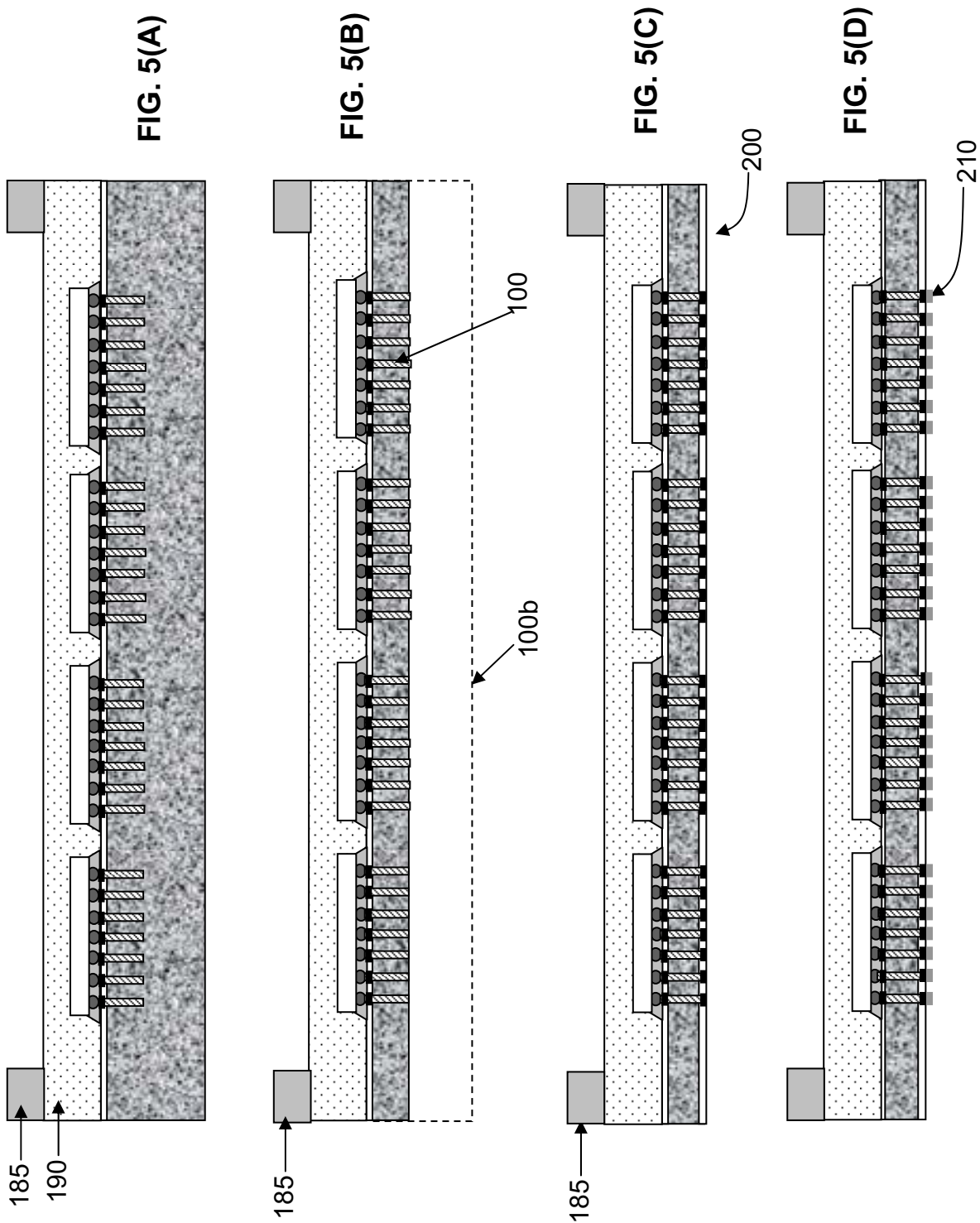


FIG. 4(J)



“Wafer Bumping”
Step 12

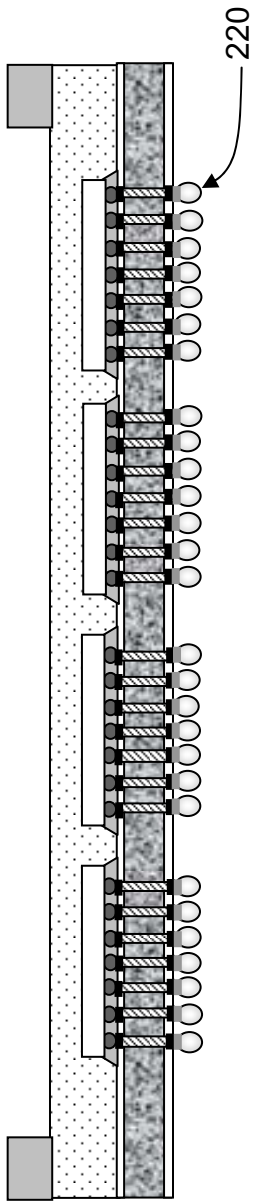


FIG. 5(E)

“Singulation”
Step 14

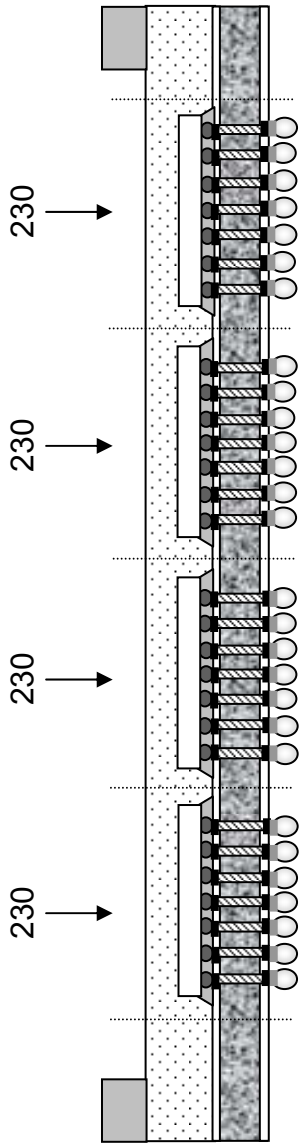


FIG. 5(F)

“Wafer Level
Molding”
Step 8

“Wafer Thinning”
Step 9

“Backside
Metallization/
Passivation” Step 10

“Under Bump
Metallization”
Step 11

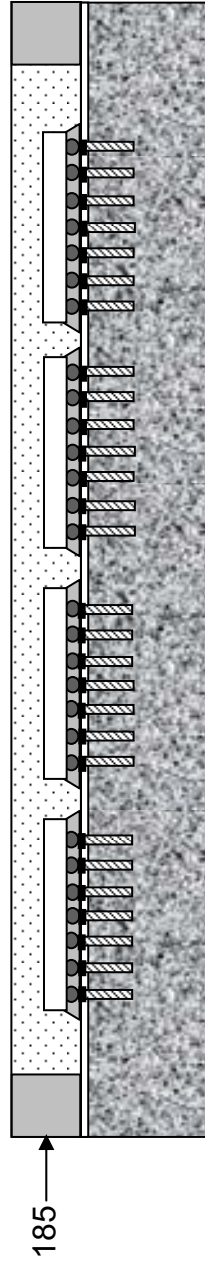


FIG. 6(A)

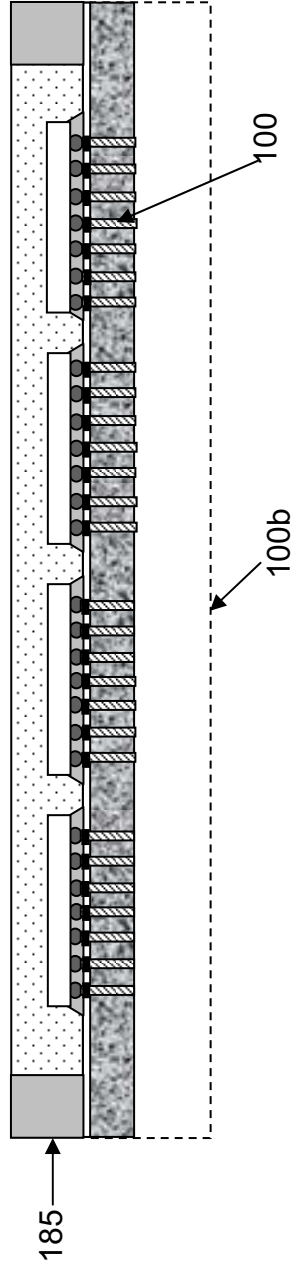


FIG. 6(B)

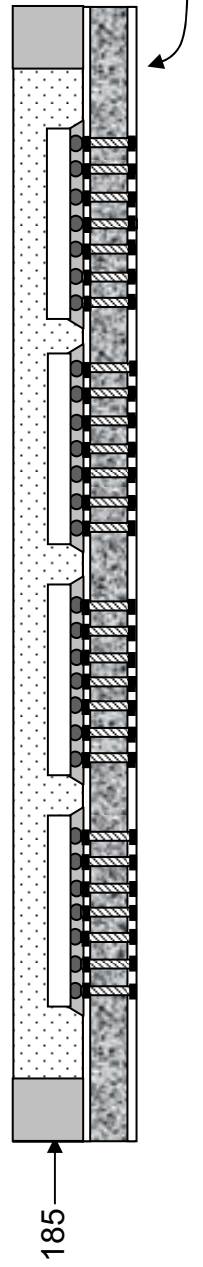


FIG. 6(C)

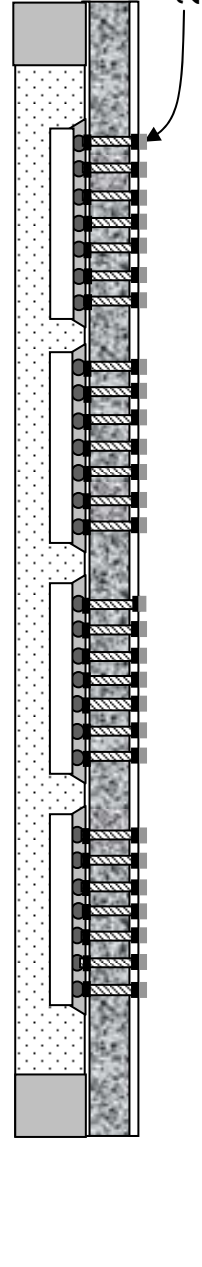


FIG. 6(D)

“Wafer Bumping”
Step 12

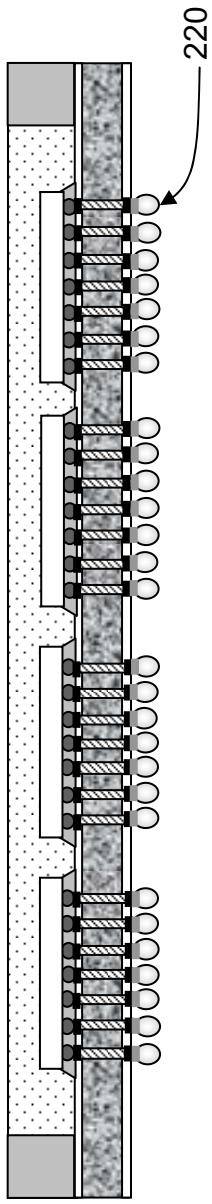


FIG. 6(E)

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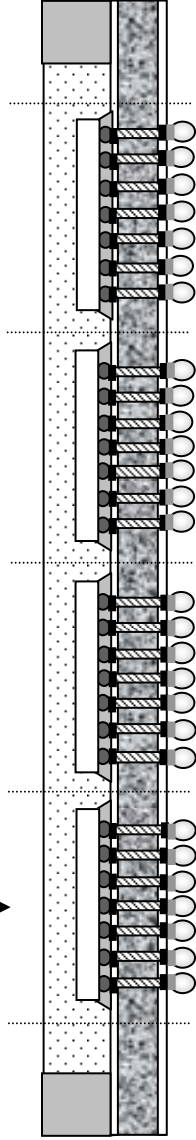


FIG. 6(F)

“Singulation”
Step 14