

the one or more second circuits each comprises an input receiving the aggregated indication from a respective buffer of the second plurality of buffers, and

the communication path is configured as a loop comprising a forward path and a backward path, the forward path sequentially connecting buffers of the first plurality of buffers and the backward path sequentially connecting buffers of the second plurality of buffers.

6. The system of claim 1, wherein the system is an automatic testing system and at least a portion of the messages represent the failure of a test in the automatic testing system.

7. The system of claim 6, wherein the plurality of first circuits and/or the one or more second circuits comprise test pattern generators.

8. The system of claim 6, wherein:
the system comprises a backplane and a plurality of instrument modules coupled through the backplane, and
the plurality of first circuits and/or the one or more second circuits comprise instrument modules of the plurality of instrument modules.

~~9. The system of claim 1, wherein the messages are event indications.~~

910. The system of claim 2, wherein the second plurality of buffers are configured to simultaneously provide the aggregated indication to the plurality of second circuits.

1011. The system of claim 1, wherein:
the first plurality of buffers are coupled to the communication path in an order,
the aggregated indication comprises a signal with a plurality of time slots, and

the communication path is configured to perform aggregation of the messages by setting values within time slots of the plurality of time slots based on messages from respective first circuits of the plurality of first circuits.

1112. The system of claim 1011, wherein:

the communication path comprises at least one track, a first track of the at least one tracks configured to receive a message during each cycle from one of a subset of the first plurality of buffers, and

the communication path is configured to perform aggregation of the messages by aggregating on the first track the messages received from buffers of the subset.

1213. The system of claim 1112, wherein the subset of the first plurality of buffers comprises N buffers and the communication path is configured to propagate an aggregated indication from a first end of the communication path to a second end of the communication path in N cycles.

1314. The system of claim 1213, wherein the one or more second circuits comprises a memory configured to store historical data, and wherein the system is configured to keep or discard data in the memory based on the aggregated indicator.

~~15. The system of claim 14, wherein the dwell time of the memory is N cycles.~~

1416. The system of claim 2, wherein:

the first plurality of buffers are coupled to the communication path in an order, and

the first plurality of buffers are configured to provide respective messages indicating events at a first time during successive periods based on the order of the first plurality of buffers, wherein a period is a fixed number of cycles.

1517. The system of claim 1416, wherein:

the plurality of first circuits are configured to simultaneously output messages indicating events at the first time to each of the first plurality of buffers, and

the second plurality of buffers are each configured to simultaneously provide an aggregated indication of events at the first time to the respective second circuit.

~~18. The system of claim 17, wherein:~~

~~the communication path comprises a plurality of tracks,~~

~~the first plurality of buffers are configured to, during each cycle, provide a message to successive tracks, and~~

~~the communication path is configured to perform aggregation of the messages by aggregating messages within the plurality of tracks.~~

1619. A method of processing event information in a plurality of successive cycles, the method comprising:

during a first cycle, generating a message at each of a plurality of first circuits;

buffering each message for a variable length of time in one of a first plurality of buffers, each of the first plurality of buffers associated with one of the plurality of first circuits;

during a second cycle, setting a value at a first position of the communication path coupled to a first buffer of the first plurality of buffers, wherein the first plurality of buffers are coupled to the communication path in a first order;

in each of a plurality of cycles following the second cycle, communicating the value along the communication path to a subsequent position along the communication path, the subsequent position associated with a subsequent buffer in the first order and updating the value by aggregating the value with a message from the buffer at the subsequent position, thereby generating an aggregated indication; and

during a third cycle, providing the aggregated indication to each of one or more second circuits.

1720. The method of claim 1619, additionally comprising, subsequent to generating the aggregated indication and prior to the third cycle:

in each of a plurality of cycles, communicating the aggregated indication along the communication path to a second plurality of buffers, the second plurality of buffers coupled to the communication path in a second order; and

buffering the aggregated indication in each of the second plurality of buffers for a variable length of time, wherein

each second circuit is associated with one of the second plurality of buffers.

1821. The method of claim 1619, wherein the plurality of first circuits and the plurality of second circuits consist of the same plurality of circuits.

1922. The method of claim 1821, wherein the communication path is configured as a loop comprising a forward path and a backward path, the forward path sequentially connecting buffers of the first plurality of buffers and the backward path sequentially connecting buffers of the second plurality of buffers.

2023. The method of claim 1619, wherein the system is an automatic testing system and at least a portion of the messages represent the failure of a test in the automatic testing system.

2124. The method of claim 2023, wherein the plurality of first circuits and/or the plurality of second circuits comprise test pattern generators.

2225. The method of claim 1619, wherein:

the aggregated indication comprises a signal with a plurality of time slots, and
updating the value comprises aggregating the value within a time slot of the plurality of time slots by aggregating the value communicated along the communication path with a message from a respective buffer of the first plurality of buffers.

~~26. The method of claim 25, wherein:~~

~~the communication path comprises at least one track;~~

~~a first track of the at least one tracks receives a message during each cycle from one of a subset of the first plurality of buffers, and
updating the value comprises aggregating the value with a message received from buffers of the subset.~~

~~27. The method of claim 26, wherein:~~

~~the second plurality of buffers comprises a memory configured to store historical data, and~~

~~data in the memory is kept or discarded based on the aggregated indicator.~~

~~28. The method of claim 19, wherein:~~

~~the first plurality of buffers provide respective messages during successive cycles based on the order of the first plurality of buffers.~~

~~29. The method of claim 28, wherein:~~

~~the communication path comprises a plurality of tracks,~~

~~the first plurality of buffers provide a message to successive tracks during each cycle, and~~

~~updating the value comprises aggregating the value within the plurality of tracks.~~

~~30. The method of claim 19, wherein the messages are event indications.~~

2334. An interface circuit for an automatic test system in which a communication path carries messages, comprising:

a plurality of input ports;

a plurality of output ports;

a reference clock input;

a first plurality of buffers coupled to the reference clock input, each buffer of the first plurality of buffers coupled to an input port and configured to receive messages at a time controlled by the reference clock;

a communication path configured to receive the plurality of messages from the first plurality of buffers and to perform aggregation of the messages, thereby generating an aggregated indication; and

a second plurality of buffers, each buffer of the second plurality of buffers coupled to an output port, configured to store an aggregated indication and to synchronously output the aggregated indication to a respective output port.

2432. The interface circuit of claim 2331, wherein buffers of the first plurality of buffers and the second plurality of buffers are First In First Out (FIFO) buffers.

2533. The interface circuit of claim 2331, wherein:

the communication path is configured as a loop comprising a forward path and a backward path, the forward path sequentially connecting buffers of the first plurality of buffers and the backward path sequentially connecting buffers of the second plurality of buffers.

2634. The interface circuit of claim 2331, wherein the interface circuit is a backplane interface circuit configured to be used in an automatic testing system and at least a portion of the messages represent the failure of a test in the automatic testing system.

~~35. The interface circuit of claim 31, wherein the messages are event indications.~~

~~36. The interface circuit of claim 31, wherein the second plurality of buffers are configured to simultaneously provide the aggregated indication to the output ports.~~

2737. The interface circuit of claim 2331, wherein:

the first plurality of buffers are coupled to the communication path in an order, the aggregated indication comprises a signal with a plurality of time slots, and the communication path is configured to perform aggregation of the messages by setting values within time slots of the plurality of time slots based on messages from respective input ports of the plurality of input ports.

2838. The interface circuit of claim 2737, wherein:

the communication path comprises at least one track, a first track of the at least one tracks configured to receive a message during each cycle from one of a subset of the first plurality of buffers, and

the communication path is configured to perform aggregation of the messages by aggregating on the first track the messages received from buffers of the subset.

~~39. The interface circuit of claim 38, wherein the subset of the first plurality of buffers comprises N buffers and the communication path is configured to propagate an aggregated indication from a first end of the communication path to a second end of the communication path in N cycles.~~

~~40. The interface circuit of claim 31, wherein:~~

~~the first plurality of buffers are coupled to the communication path in an order, and~~

~~the first plurality of buffers are configured to provide respective messages indicating events at a first time during successive cycles based on the order of the first plurality of buffers.~~

~~41. The interface circuit of claim 40, wherein:~~

~~the second plurality of buffers are each configured to simultaneously provide an aggregated indication of events at the first time to the respective output port.~~

~~42. The interface circuit of claim 41, wherein:~~

~~the communication path comprises a plurality of tracks,~~

~~the first plurality of buffers are configured to, during each cycle, provide a message to successive tracks, and~~

~~the communication path is configured to perform aggregation of the messages by aggregating messages within the plurality of tracks.~~