Claims

1. A thermal plate, configured to overlay a temperature controlled base plate of a substrate support assembly used to support a semiconductor substrate in a semiconductor processing apparatus, the thermal plate comprising:

an electrically insulating plate;

planar thermal zones comprising at least first, second, third and fourth planar thermal zones, each comprising one or more Peltier devices as thermoelectric elements, the planar thermal zones laterally distributed across the electrically insulating plate and operable to tune a spatial temperature profile on the substrate;

positive voltage lines comprising first and second electrically conductive positive voltage lines laterally distributed across the electrically insulating plate;

negative voltage lines comprising first and second electrically conductive negative voltage lines laterally distributed across the electrically insulating plate;

common lines comprising first and second electrically conductive common lines laterally distributed across the electrically insulating plate;

first, second, third, fourth, fifth, sixth, seventh and eighth diodes laterally distributed across the electrically insulating plate;

wherein:

an anode of the first diode is connected to the first positive voltage line and a cathode of the first diode is connected to the first planar thermal zone;

an anode of the second diode is connected to the first planar thermal zone and a cathode of the second diode is connected to the first negative voltage line;

an anode of the third diode is connected to the first positive voltage line and a cathode of the third diode is connected to the second planar thermal zone;

an anode of the fourth diode is connected to the second planar thermal zone and a cathode of the fourth diode is connected to the first negative voltage line;

an anode of the fifth diode is connected to the second positive voltage line and a cathode of the fifth diode is connected to the third planar thermal zone;

an anode of the sixth diode is connected to the third planar thermal zone and a cathode of the sixth diode is connected to the second negative voltage line;

an anode of the seventh diode is connected to the second positive voltage line and a cathode of the seventh diode is connected to the fourth planar thermal zone;

an anode of the eighth diode is connected to the fourth planar thermal zone and a cathode of the eighth diode is connected to the second negative voltage line;

the first common line is connected to both the first and third planar thermal zones; and

the second common line is connected to both the second and fourth planar thermal zones.

2. The thermal plate of claim 1, wherein the planar thermal zones do not comprise any resistive heater elements.

3. The thermal plate of claim 1, wherein

(a) the Peltier devices of each of the planar thermal zones are located in an upper portion of the electrically insulating plate; the positive voltage and negative voltage lines are disposed below the Peltier devices and electrically connected to the diodes by vias extending vertically in the electrically insulating plate; the common lines are below the positive and negative voltage lines and are electrically connected to the planar thermal zones by vias extending vertically in the electrically insulating plate.

4. The thermal plate of claim 1, wherein the planar thermal zones are sized such that:

(a) each planar thermal zone is not larger than four device dies being manufactured on the semiconductor substrate,

(b) each planar thermal zone is not larger than two device dies being manufactured on the semiconductor substrate,

(c) each planar thermal zone is not larger than one device die being manufactured on the semiconductor substrate, or

(d) each planar thermal zone is scaled with sizes of device dies on the semiconductor substrate and the overall size of the semiconductor substrate.

5. The thermal plate of claim 1, wherein the planar thermal zones are sized such that:

(a) each planar thermal zone is 0.1 to 1 cm^2,

(b) each planar thermal zone is 2 to 3 cm^2,

(c) each planar thermal zone is 1 to 15 cm^2, or

(d) each planar thermal zone is 16 to 100 cm^2.

6. The thermal plate of claim 1, wherein the thermal plate includes 16 to 400 planar thermal zones.

7. The thermal plate of claim 1, wherein the electrically insulating plate comprises one or more layers of a polymer material, a ceramic material, a fiberglass composite, or a combination thereof.

8. The thermal plate of claim 1, wherein the total number of positive voltage lines is equal to or less than one half the total number of the planar thermal zones, and/or the total number of the common lines is equal to or less than one half the total number of the planar thermal zones.

9. The thermal plate of claim 1, wherein a total area of the planar thermal zones is from 50% to 100% of an upper surface of the thermal plate.

10. The thermal plate of claim 1, wherein the planar thermal zones are arranged in a rectangular grid, hexagonal grid or polar array; and the planar thermal zones are separated from each other by gaps at least 1 millimeter in width and at most 10 millimeters in width.

11. A substrate support assembly comprising:

an electrostatic chuck (ESC) including at least one electrostatic clamping electrode configured to electrostatically clamp a semiconductor substrate on the substrate support assembly;

an upper side of the thermal plate of claim 1 supporting the ESC; and

a temperature controlled base plate attached to a lower side of the thermal plate.

12. The substrate support assembly of claim 11, further comprising at least one primary heater layer arranged above or below the thermal plate, wherein the primary heater layer is electrically insulated from the planar thermal zones, the primary heater layer includes at least one resistance heater which provides mean temperature control of the semiconductor substrate; the planar thermal zones provide radial and azimuthal temperature profile control of the semiconductor substrate, during processing thereof.

13. A method for manufacturing the thermal plate of claim 1, comprising:

pressing a mixture of ceramic powder, binder and liquid into sheets;

drying the sheets;

forming vias in the sheets by punching holes therein;

forming the positive voltage, negative voltage and common lines on the sheets;

aligning the sheets;

bonding the sheets by adhesive or sintering to form the thermal plate;

filling the vias with a slurry of conducting powder;

bonding Peltier devices and diodes onto the thermal plate such that Peltier device(s) in each planar thermal zone are connected to a pair of positive and negative lines and one common line such that no two Peltier devices in different planar thermal zones share the same common line and pair of positive and negative lines.

14. The method of claim 13, wherein the positive, negative and common lines are formed by screen printing a slurry of conducting powder, pressing a precut metal foil, or spraying a slurry of conducting powder.

15. A method for manufacturing the thermal plate of claim 1, comprising:

(a) bonding a metal sheet onto a fiberglass composite plate, or a metal plate covered by an electrically insulating polymer film;

(b) applying a patterned resist film to the surface of the metal sheet wherein the openings in the patterned resist film define the shapes and positions of a group of conductor lines corresponding to positive voltage, negative voltage and/or common lines;

(c) forming the group of conductor lines by chemically etching portions of the metal sheet exposed through the openings in the patterned resist film;

(d) removing the resist film;

(e) applying an electrically insulating polymer film on the metal sheet;

(f) optionally repeat steps (b)-(e) one or more times;

(g) forming vias by punching holes through the metal sheet(s) and the electrically insulating polymer film(s) and filling the holes with at least one of metal, a slurry of conducting powder, conductive adhesive or conductive polymer;

(h) bonding Peltier devices and diodes to one or more electrically insulating polymer films and assembling the films to form the thermal plate such that Peltier devices in each

planar thermal zone are connected to a pair of positive and negative lines and one common line and no two Peltier devices in different planar thermal zones share the same common line and pair of positive and negative lines.

16. A method for plasma processing semiconductor substrates in a plasma processing chamber containing the substrate support assembly of claim 11, comprising:

(a) loading a semiconductor substrate into the processing chamber and positioning the semiconductor substrate on the substrate support assembly;

(b) determining a temperature profile that compensates for processing conditions affecting critical dimension (CD) uniformity;

(c) heating the semiconductor substrate to conform to the temperature profile using the substrate support assembly;

(d) igniting plasma and processing the semiconductor substrate while controlling the temperature profile by independently controlled heating or cooling of the planar thermal zones;

(e) unloading the semiconductor substrate from the processing chamber and repeating steps (a)-(e) with a different semiconductor substrate.

17. The substrate support assembly of claim 12, wherein the primary heater layer includes two or more heaters.

18. The thermal plate of claim 1, wherein the thermal plate is configured to support an electrostatic clamping layer.

We Claim:

1. A thermal plate, configured to overlay a temperature controlled base plate of a substrate support assembly used to support a semiconductor substrate in a semiconductor processing apparatus, the thermal plate comprising:

an electrically insulating plate;

planar thermal zones comprising at least first, second, third and fourth planar thermal zones, each comprising one or more Peltier devices as thermoelectric elements, the planar thermal zones laterally distributed across the electrically insulating plate and operable to tune a spatial temperature profile on the substrate;

positive voltage lines comprising first and second electrically conductive positive voltage lines laterally distributed across the electrically insulating plate;

negative voltage lines comprising first and second electrically conductive negative voltage lines laterally distributed across the electrically insulating plate;

common lines comprising first and second electrically conductive common lines laterally distributed across the electrically insulating plate;

first, second, third, fourth, fifth, sixth, seventh and eighth diodes laterally distributed across the electrically insulating plate;

wherein:

an anode of the first diode is connected to the first positive voltage line and a cathode of the first diode is connected to the first planar thermal zone;

an anode of the second diode is connected to the first planar thermal zone and a cathode of the second diode is connected to the first negative voltage line;

an anode of the third diode is connected to the first positive voltage line and a cathode of the third diode is connected to the second planar thermal zone;

an anode of the fourth diode is connected to the second planar thermal zone and a cathode of the fourth diode is connected to the first negative voltage line;

an anode of the fifth diode is connected to the second positive voltage line and a cathode of the fifth diode is connected to the third planar thermal zone;

an anode of the sixth diode is connected to the third planar thermal zone and a cathode of the sixth diode is connected to the second negative voltage line;

an anode of the seventh diode is connected to the second positive voltage line and a cathode of the seventh diode is connected to the fourth planar thermal zone;

an anode of the eighth diode is connected to the fourth planar thermal zone and a cathode of the eighth diode is connected to the second negative voltage line;

the first common line is connected to both the first and third planar thermal zones; and

the second common line is connected to both the second and fourth planar thermal zones.

2. The thermal plate of Claim 1, wherein the planar thermal zones do not comprise any resistive heater elements.

3. The thermal plate of Claim 1, wherein

(a) the Peltier devices of each of the planar thermal zones are located in an upper portion of the electrically insulating plate; the positive voltage and negative voltage lines are disposed below the Peltier devices and electrically connected to the diodes by vias extending vertically in the electrically insulating plate; the common lines are below the positive and negative voltage lines and are electrically connected to the planar thermal zones by vias extending vertically in the electrically insulating plate.

4. The thermal plate of Claim 1, wherein the planar thermal zones are sized such that:

(a) each planar thermal zone is not larger than four device dies being manufactured on the semiconductor substrate,

(b) each planar thermal zone is not larger than two device dies being manufactured on the semiconductor substrate,

(c) each planar thermal zone is not larger than one device die being manufactured on the semiconductor substrate, or

(d) each planar thermal zone is scaled with sizes of device dies on the semiconductor substrate and the overall size of the semiconductor substrate.

5. The thermal plate of Claim 1, wherein the planar thermal zones are sized such that:

(a) each planar thermal zone is 0.1 to 1 cm^2,

(b) each planar thermal zone is 2 to 3 cm^2,

(c) each planar thermal zone is 1 to 15 cm^2, or

(d) each planar thermal zone is 16 to 100 cm^2.

6. The thermal plate of Claim 1, wherein the thermal plate includes 16 to 400 planar thermal zones.

7. The thermal plate of Claim 1, wherein the electrically insulating plate comprises one or more layers of a polymer material, a ceramic material, a fiberglass composite, or a combination thereof.

8. The thermal plate of Claim 1, wherein the total number of positive voltage lines is equal to or less than one half the total number of the planar thermal zones, and/or the total number of the common lines is equal to or less than one half the total number of the planar thermal zones.

9. The thermal plate of Claim 1, wherein a total area of the planar thermal zones is from 50% to 100% of an upper surface of the thermal plate.

10. The thermal plate of Claim 1, wherein the planar thermal zones are arranged in a rectangular grid, hexagonal grid or polar array; and the planar thermal zones are separated from each other by gaps at least 1 millimeter in width and at most 10 millimeters in width.

11. A substrate support assembly comprising:

an electrostatic chuck (ESC) including at least one electrostatic clamping electrode configured to electrostatically clamp a semiconductor substrate on the substrate support assembly;

an upper side of the thermal plate of Claim 1 supporting the ESC; and

a temperature controlled base plate attached to a lower side of the thermal plate.

12. The substrate support assembly of Claim 11, further comprising at least one primary heater layer arranged above or below the thermal plate, wherein the primary heater layer is electrically insulated from the planar thermal zones, the primary heater layer includes at least one resistance heater which provides mean temperature control of the semiconductor substrate; the planar thermal zones provide radial and azimuthal temperature profile control of the semiconductor substrate, during processing thereof.

13. A method for manufacturing the thermal plate of Claim 1, comprising:

pressing a mixture of ceramic powder, binder and liquid into sheets;

drying the sheets;

forming vias in the sheets by punching holes therein;

forming the positive voltage, negative voltage and common lines on the sheets;

aligning the sheets;

bonding the sheets by adhesive or sintering to form the thermal plate;

filling the vias with a slurry of conducting powder;

bonding Peltier devices and diodes onto the thermal plate such that Peltier device(s) in each planar thermal zone are connected to a pair of positive and negative lines and one common line such that no two Peltier devices in different planar thermal zones share the same common line and pair of positive and negative lines.

14. The method of Claim 13, wherein the positive, negative and common lines are formed by screen printing a slurry of conducting powder, pressing a precut metal foil, or spraying a slurry of conducting powder.

15. A method for manufacturing the thermal plate of Claim 1, comprising:

(a) bonding a metal sheet onto a fiberglass composite plate, or a metal plate covered by an electrically insulating polymer film;

(b) applying a patterned resist film to the surface of the metal sheet wherein the openings in the patterned resist film define the shapes and positions of a group of conductor lines corresponding to positive voltage, negative voltage and/or common lines;

(c) forming the group of conductor lines by chemically etching portions of the metal sheet exposed through the openings in the patterned resist film;

(d) removing the resist film;

(e) applying an electrically insulating polymer film on the metal sheet;

(f) optionally repeat steps (b)-(e) one or more times;

(g) forming vias by punching holes through the metal sheet(s) and the electrically insulating polymer film(s) and filling the holes with at least one of metal, a slurry of conducting powder, conductive adhesive or conductive polymer;

(h) bonding Peltier devices and diodes to one or more electrically insulating polymer films and assembling the films to form the thermal plate such that Peltier devices in each planar thermal zone are connected to a pair of positive and negative lines and one common

line and no two Peltier devices in different planar thermal zones share the same common line and pair of positive and negative lines.

16. A method for plasma processing semiconductor substrates in a plasma processing chamber containing the substrate support assembly of Claim 11, comprising:

(a) loading a semiconductor substrate into the processing chamber and positioning the semiconductor substrate on the substrate support assembly;

(b) determining a temperature profile that compensates for processing conditions affecting critical dimension (CD) uniformity;

(c) heating the semiconductor substrate to conform to the temperature profile using the substrate support assembly;

(d) igniting plasma and processing the semiconductor substrate while controlling the temperature profile by independently controlled heating or cooling of the planar thermal zones;

(e) unloading the semiconductor substrate from the processing chamber and repeating steps (a)-(e) with a different semiconductor substrate.

17. The substrate support assembly of Claim 12, wherein the primary heater layer includes two or more heaters.

18. The thermal plate of Claim 1, wherein the thermal plate is configured to support an electrostatic clamping layer.