Claims

1. A system configured to determine overlay error between different patterned features of a design printed on a wafer in a multi-patterning step process, comprising:

an output acquisition subsystem comprising at least an energy source and a detector, wherein the energy source is configured to generate energy that is directed to a wafer, wherein the detector is configured to detect energy from the wafer and to generate output responsive to the detected energy, wherein first and second patterned features are printed on a level of the wafer with first and second patterning steps, respectively, and wherein a design for the level of the wafer comprises a design for the first patterned features and a design for the second patterned features; and

one or more computer subsystems configured for:

aligning the design for the level of the wafer to an image for the wafer generated from the output by aligning the design for the first patterned features to the first patterned features in the image thereby aligning all of the design for the level to the first patterned features;

shifting only the design for the second patterned features from a position of the design for the second patterned features, determined by said aligning all of the design, to a shifted position of the design for the second patterned features by aligning only the design for the second patterned features to only the second patterned features in the image; and

determining an offset between the position of the design for the second patterned features and the shifted position of the design for the second patterned features, wherein the offset is equal to relative overlay error between the

first patterned features on the wafer and the second patterned features on the wafer.

2. The system of claim 1, wherein the design for the level of the wafer further comprises a design for third patterned features, wherein the third patterned features are printed on the level of the wafer with a third patterning step, and wherein the one or more computer subsystems are further configured for:

shifting only the design for the third patterned features from a position of the design for the third patterned features, determined by said aligning all of the design, to a shifted position of the design for the third patterned features by aligning only the design for the third patterned features to only the third patterned features in the image; and

determining an offset between the position of the design for the third patterned features and the shifted position of the design for the third patterned features, wherein the offset for the third patterned features is equal to relative overlay error between the first patterned features on the wafer and the third patterned features on the wafer.

3. The system of claim 2, wherein the one or more computer subsystems are further configured for determining relative overlay error between the second patterned features on the wafer and the third patterned features on the wafer based on the offset determined for the second patterned features and the offset determined for the third patterned features.

4. The system of claim 1, wherein the one or more computer subsystems are further configured for determining design-based center lines of the first and second patterned features in the design and design-based center lines of spaces in the design.

5. The system of claim 4, wherein the one or more computer subsystems are further configured for determining image-based center lines of the first and second patterned features in the image and image-based center lines of the spaces in the image.

6. The system of claim 5, wherein the one or more computer subsystems are further configured for determining additional offsets between 1) a position of each of the image-based center lines of the first patterned features in the image and a position of a corresponding one of the design-based center lines determined for the first patterned features and 2) a position of each of the image-based center lines of the spaces between the first patterned features in the image and a position of a corresponding one of the design-based center lines determined for the spaces between the first patterned features, and wherein the position of each of the corresponding one of the design-based center lines used to determine the additional offsets is determined with respect to a position of the design for the first patterned features, determined by said aligning all of the design.

7. The system of claim 6, wherein the one or more computer subsystems are further configured for determining other additional offsets between 1) a position of each of the image-based center lines of the second patterned features in the image and a position of a corresponding one of the design-based center lines determined for the second patterned features and 2) a position of each of the image-based center lines of the spaces between the second patterned features in the image and a position of a corresponding one of the design-based center lines determined for the spaces between the second patterned features, and wherein the position of each of the corresponding one of the design-based center lines used to determine the other additional offsets is determined with respect to the shifted position of the design for the second patterned features.

8. The system of claim 7, wherein the one or more computer subsystems are further configured for performing global alignment of two or more of 1) the image-based center lines of the first patterned features and the design-based center lines corresponding to the first patterned features and 2) the image-based center lines of the spaces between the first patterned features and

the design-based center lines corresponding to the spaces between the first patterned features by finding a global minimum of the additional offsets between the two or more of 1) the image-based center lines of the first patterned features and the design-based center lines corresponding to the first patterned features and 2) the image-based center lines of the spaces between the first patterned features and the design-based center lines corresponding to the spaces between the first patterned features.

9. The system of claim 8, wherein the one or more computer subsystems are further configured for modifying the offset determined between the position of the design for the second patterned features and the shifted position of the design for the second patterned features based on results of performing the global alignment, and wherein said modifying the offset generates a modified offset.

10. The system of claim 9, wherein the one or more computer subsystems are further configured for determining a second offset for the design for the second patterned features by performing global alignment of two or more of 1) the image-based center lines of the second patterned features and the design-based center lines corresponding to the second patterned features and 2) the image-based center lines of the spaces between the second patterned features and the design-based center lines corresponding to the spaces between the second patterned features by finding a global minimum of the other additional offsets between the two or more of 1) the image-based center lines of the second patterned features and the design-based center lines corresponding to the second patterned features and 2) the image-based center lines of the spaces between the second patterned features and the design-based center lines corresponding to the spaces between the second patterned features.

11. (Original) The system of claim 10, wherein the one or more computer subsystems are further configured for determining a final offset by applying the second offset to the modified offset, and wherein the final offset is equal to fine relative overlay error between the first patterned features on the wafer and the second patterned features on the wafer.

12. The system of claim 11, wherein the one or more computer subsystems are capable of determining fine relative overlay errors equal to or smaller than 5 nm.

13. The system of claim 11, wherein the design for the level of the wafer further comprises a design for third patterned features, wherein the third patterned features are printed on the level of the wafer with a third patterning step, and wherein the one or more computer subsystems are further configured for:

shifting only the design for the third patterned features from a position of the design for the third patterned features, determined by said aligning all of the design, to a shifted position of the design for the third patterned features by aligning only the design for the third patterned features to only the third patterned features in the image;

determining an offset between the position of the design for the third patterned features and the shifted position of the design for the third patterned features, wherein the offset for the third patterned features is equal to relative overlay error between the first patterned features on the wafer and the third patterned features on the wafer;

modifying the offset for the third patterned features based on results of performing the global alignment for the first patterned features and the spaces between the first patterned features, wherein said modifying the offset for the third patterned features generates a modified offset for the third patterned features;

performing said determining design-based center lines and said determining image-based center lines for the third patterned features and spaces between the third patterned features;

determining further additional offsets between 1) a position of each of the image-based center lines of the third patterned features in the image and a position of a

corresponding one of the design-based center lines determined for the third patterned features and 2) a position of each of the image-based centered lines of the spaces between the third patterned features in the image and a position of a corresponding one of the design-based center lines determined for the spaces between the third patterned features, wherein the position of each of the corresponding one of the design-based center lines used to determine the further additional offsets is determined with respect to the shifted position of the design for the third patterned features;

determining a third offset for the design for the third patterned features by performing global alignment of two or more of 1) the image-based center lines of the third patterned features and the design-based center lines corresponding to the third patterned features and 2) the image-based center lines of the spaces between the third patterned features and the design-based center lines corresponding to the spaces between the third patterned features by finding a global minimum of the further additional offsets between the two or more of 1) the image-based center lines of the third patterned features and the design-based center lines corresponding to the third patterned features and 2) the image-based center lines of the spaces between the third patterned features and the design-based center lines corresponding to the spaces between the third patterned features; and

determining another final offset by applying the third offset to the modified offset for the third patterned features, wherein the other final offset is equal to fine relative overlay error between the first patterned features on the wafer and the third patterned features on the wafer.

14. The system of claim 13, wherein the one or more computer subsystems are further configured for determining fine relative overlay error between the second patterned features on the wafer and the third patterned features on the wafer based on the final offset and the other final offset.

15. The system of claim 1, wherein the first and second patterned features are formed in a die on the wafer.

16. The system of claim 1, wherein the first and second patterned features for which said aligning, said shifting, and said determining are performed are not selected by a user.

17. The system of claim 1, wherein the first and second patterned features for which said aligning, said shifting, and said determining are performed are not selected based on symmetry of the first and second patterned features along an imaginary axis.

18. The system of claim 1, wherein the first and second patterned features for which said aligning, said shifting, and said determining are performed comprise any patterned features formed in a die on the wafer.

19. The system of claim 1, wherein the energy directed to the wafer comprises light, and wherein the energy detected from the wafer comprises light.

20. The system of claim 1, wherein the energy directed to the wafer comprises electrons, and wherein the energy detected from the wafer comprises electrons.

21. A non-transitory computer-readable medium, storing program instructions executable on a computer system for performing a computer-implemented method for determining overlay error between different patterned features of a design printed on a wafer in a multi-patterning step process, wherein the computer-implemented method comprises:

aligning a design for a level of a wafer to an image for the wafer generated from output generated by an output acquisition system comprising at least an energy source and a detector, wherein the energy source is configured to generate energy that is directed to a wafer, wherein the detector is configured to detect energy from the

wafer and to generate output responsive to the detected energy, wherein first and second patterned features are printed on the level of the wafer with first and second patterning steps, respectively, wherein a design for the level of the wafer comprises a design for the first patterned features and a design for the second patterned features, and wherein said aligning comprises aligning the design for the first patterned features to the first patterned features in the image thereby aligning all of the design for the level to the first patterned features;

shifting only the design for the second patterned features from a position of the design for the second patterned features, determined by said aligning all of the design, to a shifted position of the design for the second patterned features by aligning only the design for the second patterned features to only the second patterned features in the image; and

determining an offset between the position of the design for the second patterned features and the shifted position of the design for the second patterned features, wherein the offset is equal to relative overlay error between the first patterned features on the wafer and the second patterned features on the wafer, and wherein said aligning, said shifting, and said determining are performed by the computer system.

22. A computer-implemented method for determining overlay error between different patterned features of a design printed on a wafer in a multi-patterning step process, comprising:

aligning a design for a level of a wafer to an image for the wafer generated from output generated by an output acquisition system comprising at least an energy source and a detector, wherein the energy source is configured to generate energy that is directed to a wafer, wherein the detector is configured to detect energy from the wafer and to generate output responsive to the detected energy, wherein first and second patterned features are printed on the level of the wafer with first and

second patterning steps, respectively, wherein a design for the level of the wafer comprises a design for the first patterned features and a design for the second patterned features, and wherein said aligning comprises aligning the design for the first patterned features to the first patterned features in the image thereby aligning all of the design for the level to the first patterned features;

shifting only the design for the second patterned features from a position of the design for the second patterned features, determined by said aligning all of the design, to a shifted position of the design for the second patterned features by aligning only the design for the second patterned features to only the second patterned features in the image; and

determining an offset between the position of the design for the second patterned features and the shifted position of the design for the second patterned features, wherein the offset is equal to relative overlay error between the first patterned features on the wafer and the second patterned features on the wafer, and wherein said aligning, said shifting, and said determining are performed by one or more computer systems.