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Discrete-time signal processing system.

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The invention relates to a discrete-time signal processing system comprising a signal sampling circuit and a sampling signal generator whose sampling frequency is adjustable, the sampling signal generator including an oscillator for generating a signal which has a fixed frequency, and a frequency divider.

- 5 In discrete-time signal processing circuits the sampling frequency for sampling an analog or digital input signal to be processed is often generated by converting, by means of a frequency divider, a high-frequency output signal of an oscillator into a sampling signal (clock signal) having a lower frequency. Needless to observe that the oscillation frequency of the oscillator is to be accurate and stable,
- 10 which is mostly achieved by the use of a crystal oscillator. The above means that the sampling frequencies are restricted to f_{osc}/n , where f_{osc} is the oscillation frequency and n the dividend of the frequency divider. If the oscillation frequency f_{osc} is relatively low compared to the clock frequency, this denotes that the clock frequency can be adjusted only in coarse steps. Conversely, if a specific clock frequency is desired, the choice of
- 15 the frequency divider will then determine the oscillation frequency which in many cases does not correspond to the frequencies belonging to the oscillator crystals which are commercially available (and thus cost effective). Furthermore, it may happen that more than one sampling frequency is necessary, such as, for example, in sampling frequency converters. This would require two (precision) oscillators, which is more expensive and
- 20 more cumbersome compared to a circuit comprising a single oscillator.

It is an object of the invention to provide a discrete-time signal processing system in which, starting from a single stable oscillator frequency, a clock signal having a desired frequency is available, the ratio between the oscillator frequency and the clock frequency not being restricted to positive integers.

- 25 It is a further object of the invention to provide a discrete-time signal processing system in which the frequency spectrum of the sampled signal is not corrupted by the frequency spectrum of the sampling signal (clock signal).

It is a further object of the invention to provide a discrete-time signal



processing system in which more than one desired clock frequency are derived from a fixed oscillator frequency, the ratio between oscillator frequency and clock frequency not being restricted to integers.

A discrete-time signal processing system according to the invention is
5 characterized, in that the frequency divider is switchable between at least two states, in a first state the dividend of the frequency divider being n ($n = \text{integer}$) and in a second state the dividend being k , where $k \geq n+x$, where x is an integer and ≥ 1 , and in that a control input of the frequency divider for switching the frequency divider from one state to the other is connected to an output of a sigma-delta modulator (Σ - Δ modulator)
10 which is supplied with a control signal for realising an effective dividend m , where $n \leq m \leq k$.

The discrete-time signal processing system according to the invention provides the possibility of selecting with a high degree of freedom a sampling frequency which is derived from a higher clock frequency, whereas the sampling frequency is not
15 restricted to the number of integer dividends.

If with a given oscillator frequency the dividends n and k are suitably selected, usually n and $n+1$, a sampling signal can be generated with a desired frequency, so that its frequency spectrum is such that the frequency spectrum of the sampled signal is not corrupted by the spectrum of the sampling signal.

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The invention will be further explained with reference to the embodiments represented in the drawing, in which:

Fig. 1 shows in a block diagram a discrete-time signal processing system
25 according to the invention,

Fig. 2 shows in a block diagram a preferred embodiment of a discrete-time signal processing system according to the invention,

Fig. 3 shows in a block diagram a further embodiment of a discrete-time signal processing system according to the invention, and

30 Fig. 4 shows in a block diagram part of a discrete-time signal processing system suitable for a sampling frequency converter.

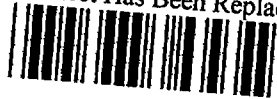


Fig. 1 shows a discrete-time signal processing system 10 according to the invention, comprising a sample-and-hold circuit 1, a decimation filter 3 connected thereto, an oscillator 5, an adjustable frequency divider 7 and a sigma-delta modulator 9 (to be denoted Σ - Δ modulator hereinafter). The sample-and-hold circuit 1 receives on its input 11 a signal to be sampled and receives on a control input 13 a sampling signal *i.e.* clock signal which is generated by means of the oscillator 5, the frequency divider 7 and the Σ - Δ modulator 9. The signal sampled by the sample-and-hold circuit 1 is further processed by the decimation filter 3.

The sampling signal to be applied to the sample-and-hold circuit 1 has a frequency which is obtained by alternately dividing the oscillation signal of the oscillator 5 in the frequency divider by either a first dividend n or a second dividend $k = n+x$. This achieves that the ratio m between the oscillation frequency and the sampling frequency may be situated between n and $n+x$ (or is equal to either n or $n+x$ if the frequency divider is not switched over). The switch-over takes place under the control of the output signal on output 15 of the Σ - Δ modulator 9 which thereto receives a control signal ϕ on the input 17. This control signal ϕ may be a DC signal, if the Σ - Δ modulator 9 is half analog and half digital, or a digital signal which may be one bit or more bits in width.

Fig. 2 shows a preferred embodiment of a discrete-time signal processing system 20 according to the invention. The system 20 comprises an input signal processor 21 and a phase comparator 23 in addition to the components 1, 3, 5, 7 and 9 described with reference to Fig. 1 and having like functions in Fig. 2. The input signal processor 21 extracts from a radio stereo signal received on input 27 the audio component, which is applied to the sample-and-hold circuit 1, and the 19 kHz pilot tone, which is applied to the input 29 of the phase comparator 23. The phase comparator 23 further receives through a divide-by-two divider 25 the output signal of the frequency divider 7 and forms from these two signals the control signal ϕ for the Σ - Δ modulator 9.

A further embodiment of a discrete-time signal processing system 30 according to the invention is shown in Fig. 3, in which all the components corresponding to those of Fig. 2 have like reference numbers and like functions. However, between the frequency divider 7 and the input 13 of the sample-and-hold circuit 1, a bandpass filter 31 is inserted, which passes a frequency band around the



desired sampling frequency. This achieves an additional reduction of the high-frequency phase-noise in the sampled signal on the control input 13 of the sample-and-hold circuit 1. The bandpass filter 31 may be arranged as an analog bandpass filter, for example a ceramic filter, or as an analog phase locked loop, by which loop a large control range
 5 can be covered in a relatively simple and cost-effective manner. The signal passed by the bandpass filter 31 is applied to a phase comparator 35. Furthermore, an input signal processor 33 is provided which extracts from a received stereo signal the audio component, which is applied to the sample-and-hold circuit 1, and derives from the 19 kHz pilot tone a double frequency signal (38 kHz) which is applied to a phase
 10 comparator 35. The phase comparator 35 applies a control signal ϕ to the Σ - Δ modulator 9.

Fig. 4 shows a further embodiment of the invention which is pre-eminently suitable for use in a sampling frequency converter. In sampling frequency converters the sampling frequency f_i for the incoming signal differs from the sampling
 15 frequency f_o for the outgoing signal. Depending on the embodiment of the sampling frequency converter, an input clock frequency f_i , a multiple thereof *i.e.* clock frequency $N.f_i$, as well as an output clock frequency f_o , is necessary, or an input clock frequency f_i , an output clock frequency f_o , and a multiple thereof, *i.e.* clock frequency $M.f_o$. The embodiment 40 shown in Fig. 4 comprises a single (crystal) oscillator 41 whose output
 20 signal is applied with the frequency f_{osc} to two frequency dividers 43 and 45. The two frequency dividers 43 and 45 are adjustable as regards their dividend *i* and *ii* respectively, where $n \leq i \leq n+x$ and $m \leq ii \leq m+y$, where n , m , x and y are positive integers. The adjustment, in this case the division by either n or $n+x$ and either m or $m+y$ by the frequency dividers 43 and 45 respectively, is determined by the
 25 output signal of the Σ - Δ converters 47 and 51 respectively, which thereto receive an input signal ϕ_1 and ϕ_2 respectively. The output signals of the frequency dividers 43 and 45 have a frequency $N.f_i$ and $M.f_o$, respectively, so that the following holds: $f_{osc} = i.N.f_i = ii.M.f_o$. The output signals $N.f_i$ and $M.f_o$ are divided by further frequency dividers 49 and 53 respectively, by a dividend N and M respectively, so that output signals are
 30 obtained having the respective desired frequency f_i and f_o . It should be observed that also the dividends N and M , although being positive integers in this example, need not of necessity be integers considering the above. It should be noted that a sampling frequency converter has been described in a prepublished European Patent Application

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CLAIMS:

1. Discrete-time signal processing system comprising a signal sampling circuit and a sampling signal generator whose sampling frequency is adjustable, the sampling signal generator including an oscillator for generating a signal which has a fixed frequency, and a frequency divider, characterized in that the frequency divider is switchable between at least two states, in a first state the dividend of the frequency divider being n ($n = \text{integer}$) and in a second state the dividend being k , where $k \geq n+x$, where x is an integer and ≥ 1 , and in that a control input of the frequency divider for switching the frequency divider from one state to the other is connected to an output of a sigma-delta modulator ($\Sigma\text{-}\Delta$ modulator) which is supplied with a control signal for realising an effective dividend m , where $n \leq m \leq k$.
2. Discrete-time signal processing system as claimed in Claim 1, characterized in that a phase detector is provided which generates the control signal and has two inputs, the first and the second input respectively, receiving a signal related to the signal produced by the frequency divider and to the signal to be sampled by the sampling circuit respectively.
3. Discrete-time signal processing system as claimed in Claim 1 or 2, characterized in that an analog filter is inserted between the output of the frequency divider and a control input of the sampling circuit.
4. Discrete-time signal processing system as claimed in Claim 1, 2 or 3, characterized in that a decimation filter is connected to the output of the sampling circuit.
5. Discrete-time signal processing system as claimed in Claim 1, 2, 3 or 4, characterized in that a clock input of the sigma-delta modulator is connected either to the output of the frequency divider or to the output of the analog filter.
6. Discrete-time signal processing system as claimed in one of the preceding Claims, characterized in that the dividend n is greater than 3 and smaller than 129.
7. Discrete-time signal processing system as claimed in Claim 6, characterized in that the dividend n is greater than 31 and smaller than 65.



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8. Discrete-time signal processing system as claimed in Claim 3, characterized in that the analog filter is a bandpass filter.
9. Discrete-time signal processing system as claimed in Claim 3, characterized in that the analog filter comprises a phase locked loop.

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