ABSTRACT

SELF-ALIGNED PRECISE HIGH SHEET RHO RESISTOR FOR MIXED-SIGNAL APPLICATION

A new method is provided for the creation of a resistive load in a semiconductor device whereby the semiconductor device further contains gate electrodes and a capacitor. Field isolation regions separate the active areas; a thin layer of gate oxide is created over these active regions. A first layer of dielectric is deposited, used for the gate electrode, for the bottom plate of the adjacent capacitor and for the resistor of high ohmic value. The gate poly is doped (in the first layer of dielectric); optionally the bottom plate of the capacitor can be doped. A second dielectric layer is deposited for the dielectric of the capacitor; a third layer of dielectric is deposited, patterned and etched to form the capacitor top plate. The capacitor (dielectric and bottom plate), poly gates and the load resistor are patterned; the LDD regions for the transistors are created. The (gate, capacitor, resistor) spacers are formed, during and as part of the etch of the gate spacers a resistive spacer (called spacer since it serves to space or separate the two contact points of the resistor) is formed. The source/drain implants for the gate electrodes are performed thereby concurrently performing (self-aligned, due to the resistor spacer) implants for the contact regions of the resistor. All contacts (gate poly, source/drain and two contact points on the resistor) are salicided to achieve lower contact resistance.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)