A CLOCK AND DATA RECOVERY CIRCUIT

Abstract

A clock and data recovery (CDR) circuit for recovering a clock signal from a non-return to zero data signal and re-timing the data signal is disclosed. The CDR circuit comprises a phase detector (PD) and a quadrature phase (QP) detector. A frequency detector (FD) is coupled to the PD and the QP detector and detects frequency difference between the PD's output signal and the QP detector's output signal and provides a FD output signal. A summer coupled to the PD and the FD for summing the PD output signal and the FD output signal and providing a summer output signal. A voltage-controlled oscillator (VCO) receives a direct current signal and provides a recovered clock signal. A polyphase filter is coupled respectively to the VCO for receiving the recovered clock signal therefrom, the PD for providing a first phase reference signal thereto, and the QP detector signal for providing a second reference phase signal thereto. A re-timer is coupled to the polyphase filter and provides a re-timed data signal, wherein the CDR circuit is on-chip and the polyphase filter converts the clock signal into the first phase reference and second phase reference signals.

Fig. 4

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