

GATE STACK FOR FIELD EFFECT TRANSISTORS

FIELD OF THE INVENTION

[0001] The present invention relates to a gate stack for field effect transistors. More specifically, the present invention relates to a gate stack having a gate dielectric which transitions through a gradient to an adhesion layer, the gradient reducing stress at the interface between the semiconductor channel of the transistor and the gate dielectric.

BACKGROUND OF THE INVENTION

[0002] Field effect transistors (FETs), such as thin film transistors (TFTs) and other devices, are well known and are widely employed in VLSI chips, displays and other semiconductor devices. In order to increase circuit densities and reduce power requirements, much research and effort has been, and continues to be, devoted to decreasing the size of such transistors. However, as the size of semiconductor devices, such as TFTs, is reduced, manufacturing and performance issues can be exacerbated and/or new problems and faults can be introduced.

SUMMARY OF THE INVENTION

[0003] It is an object of the present invention to provide a novel gate stack for semiconductor devices which obviates or mitigates a disadvantage of the prior art.

[0004] According to a first aspect of the present invention, there is provided a field effect transistor comprising: a source; a drain; a semiconductor extending between the source and the drain; a gate located over the semiconductor; and a gate stack formed between the semiconductor material and the gate, the gate stack including a dielectric layer abutting the semiconductor material, and a diffusion barrier layer abutting the gate, the gate stack including a gradient region between the dielectric layer and the diffusion barrier wherein the stoichiometry of the materials in the gradient region changes from the stoichiometry of the dielectric material to the stoichiometry of the diffusion barrier.

[0005] Preferably, the materials in the gradient region have stoichiometric ratios in the form of XO_iN_j where X is the base material, O_i is the oxygen content and N_j is the nitrogen content.

[0006] In another aspect of the present invention, there is provided a gate stack for use in a field effect transistor having a source, a drain a semiconductor connecting the source and the drain and having a gate located over the semiconductor, comprising: a dielectric material abutting

the semiconductor; a diffusion barrier abutting the gate; and a gradient material between the dielectric material and the diffusion barrier, the gradient region comprising a graded transition between the dielectric material and the diffusion barrier to reduce stressed between the dielectric material and the diffusion barrier.

[0007] The present invention provides a gate stack for a field effect transistor to reduce net charge in the dielectric material of the gate stack adjacent the semiconductor material of the transistor. The gate stack includes a gradient region between the dielectric layer abutting the semiconductor material and the diffusion barrier abutting the gate material, wherein the stoichiometry of the materials in the gradient region changes from the stoichiometry of the dielectric material to the stoichiometry of the diffusion barrier while avoiding abrupt changes in stoichiometry.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Preferred embodiments of the present invention will now be described, by way of example only, with reference to the attached Figures, wherein:

Figure 1 shows a schematic view of a prior art thin film transistor;

Figure 2 shows a schematic representation of a thin film transistor in accordance with an aspect of the present invention;

Figure 3 shows an expanded view of a gate stack of the transistor of Figure 2; and

Figure 4 shows a schematic representation of another thin film transistor in accordance with an aspect of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0009] A prior art TFT is indicated generally at 20 in Figure 1. TFT 20 includes a source 24 and a drain 28 which are formed on a suitable substrate (not shown). A semiconductor material 32, such as a metal oxide, is formed between source 24 and drain 28 and a gate dielectric material 36 is formed over semiconductor material 32. A gate 40, typically a metal, is then formed over gate dielectric material 36. As is well understood, when a voltage is applied to gate 40, a conductive channel can form through semiconductor material 32, between source 24 and drain 28, allowing current to flow therebetween.

[0010] As mentioned above, as semiconductor devices such as TFT 20 are fabricated in smaller sizes, a variety of challenges can arise. For example, dielectric material 36 can be

subject to mechanical stresses due to the different thermal expansion rates of the dielectric, semiconductor and gate metal materials during the process of annealing of TFT 20. These stresses can result in interstitial faults, vacancies and/or discontinuities in dielectric material 36 which can produce a net charge in dielectric material 36, in particular at the interface between dielectric material 36 and semiconductor material 32. The presence of such a net charge at the gate of TFT 20 is problematic as it reduces the performance of TFT 20.

[0011] Figure 2 shows a TFT 100 in accordance with an aspect of the present invention. Similar to TFT 20 described above, TFT 100 includes a source 104 and a drain 108, each of which is formed on a suitable substrate (not shown), and a semiconductor material 112 that is formed between source 104 and drain 108.

[0012] A gate dielectric stack 116 is then formed over semiconductor material 112 and a gate 120, typically a metal, is formed over gate stack 116. Stack 116 is shown in more detail in Figure 3 and, as can be seen in the Figure, stack 116 includes a layer 124 of a dielectric material, such as an oxide, and a layer 128 of a suitable diffusion barrier material (to inhibit infusion of the gate metal into the stack 116), such as a nitride.

[0013] Stack 116 further includes a gradient region 132 located between dielectric layer 124 and diffusion barrier layer 128 and gradient region 132 provides a graded transition between the material of dielectric layer 124 and the material of diffusion barrier layer 128.

[0014] As an example, if stack 116 is being formed with an Atomic Layer Deposition (ALD) process, and dielectric layer 124 is an oxide such as hafnium oxide (HfO_2) and diffusion barrier layer 128 is a nitride such as hafnium nitride (HfN), then gradient region 132 will be formed with multiple ALD cycles of different mixtures of hafnium, oxygen, and nitrogen. Specifically, the deposited layers of gradient region 132 will have stoichiometric ratios of the form of HfO_iN_j , where i and j indicate the average ratio of each of oxygen and nitrogen, respectively, in the deposited layer and in general, the stoichiometric ratios will be in the form of XO_iN_j where X is the base material such as hafnium, zirconium, etc.

[0015] For example, the portion of gradient region 132 formed in the first several cycles of ALD processing and abutting dielectric layer 124 can have a stoichiometry of $\text{HfO}_{1.9}\text{N}_{0.1}$ (i.e., $i = 1.9$ and $j = 0.1$) and the portion on top of it, formed by the next several cycles of ALD processing can have a stoichiometric ratio of $\text{HfO}_{1.7}\text{N}_{0.3}$ (i.e., $i = 1.7$ and $j = 0.3$) and so on until the portion of

gradient region 132 formed by the final few cycles of ALD processing and abutting diffusion barrier layer 128 can have a stoichiometry of $\text{HfO}_{0.1}\text{N}_{0.9}$ (i.e., $i = 0.1$ and $j = 0.9$).

[0016] It should now be apparent to those of skill in the art that the specific stoichiometric ratios of each cycle(s) of gradient region 132 are not particularly limited and it is merely required that the formed layers provide a reasonable gradient from the composition of dielectric layer 124 to the composition of diffusion barrier layer 128. Preferably the gradient in gradient region 132 from the stoichiometry of dielectric layer 124 to the stoichiometry of diffusion barrier layer 128 is monotonic, but it will be apparent to those of skill in the art that ALD processes may not be able to achieve a totally monotonic gradient and minor variations in the stoichiometry of the deposited layers are easily tolerated while avoiding abrupt changes in stoichiometry.

[0017] It will also be apparent to those of skill in the art that Figure 3 is not drawn to scale and gradient region 132 may be much thinner than illustrated, relative to dielectric layer 124 and/or diffusion barrier layer 128.

[0018] In one example of a complete gate stack 116, dielectric layer 124 can have a thickness of less than 10 nanometers (nm), and preferably between from about 7.5 nm to about 5 nm, diffusion barrier layer 128 can have a thickness of 5 nm or less, and preferably from about 3.5 nm to 2 nm, and gradient region 132 can have a thickness of from about 1 nm to about 2 nm.

[0019] In a presently preferred aspect of the present invention, semiconductor material 112 is tin oxide (SnO_2), dielectric material layer 124 is hafnium oxide (HfO_2) and diffusion barrier layer is hafnium nitride (HfN), with gradient region 132 have stoichiometry ratios of the form HfO_iN_j . However, the present invention is not so limited and different semiconductor materials such as indium gallium zinc oxide (IGZO), zinc oxide and others can be employed. Further, dielectric material 124 is not limited to hafnium oxide and instead can be a variety of materials, for example, zirconium oxide (ZrO_2) and diffusion barrier material 128 can be zirconium nitride (ZrN) and gradient region 132 can have stoichiometry ratios of the form ZrO_iN_j .

[0020] As will be apparent to those of skill in the art, the present invention is not limited to use with a tin oxide semiconductor and a variety of other semiconductor materials, such as zinc oxide and indium gallium zinc oxide (IGZO), can be usefully employed.

[0021] The provision of gradient region 132 between dielectric layer 124 and diffusion barrier layer 128 reduces the mechanical stresses which may otherwise result from annealing processing of transistor 100 and other causes of net charge in dielectric layer 124.

[0022] The gate stack 116 may further be configured to tune the threshold voltage of the TFT 100. Properties of the gate stack 116, such as the relative thicknesses of the dielectric layer 124, gradient region 132, and diffusion barrier 128, may be selected to set a desired threshold voltage.

[0023] Further, when diffusion barrier 128 is a nitride, it can also serve as an adhesion layer for the metal of gate 120.

[0024] In still further examples, when the diffusion barrier 128 is a nitride with sufficient electrical conductivity, such as hafnium nitride, a separate gate 120 may be omitted and the diffusion barrier 128 may act as the gate. In such examples, the diffusion barrier 128 may serve to inhibit infusion of metal or other species from other sources into the stack 116.

[0025] Figure 4 shows another example TFT 200 according to the present invention. The TFT 200 includes a source 212, drain 214, and gate 216. Features and aspects of the TFT 200 may be used with the TFT 100 and vice versa.

[0026] The TFT 200 is formed with a planar substrate 220. The substrate 220 may be disposed over another layer of TFTs, whether manufactured in accordance with the present invention or by another technique, or over a layer of complementary metal–oxide–semiconductor (CMOS) devices or other front end of line (FEOL) devices. In some embodiments, the TFT 200 may be manufactured using back end of line (BEOL) and/or middle of line (MOL) processes.

[0027] Examples of materials for the substrate 220 include silicon dioxide; silicon nitride; glass; fluorosilicate glass (FSG); a silicon wafer whose surface is processed with wet thermal oxide (WTO) or similar treatment; carbon doped oxide (CDO); organic polymers such as perfluorocyclobutane or polytetrafluoroethylene; organosilicates such as silsesquioxane, siloxane, organosilicate glass; flexible polymer; plastic; *etc.* Suitable combinations of such materials may also be used.

[0028] In this example, the substrate 220 is a {100} p-type boron-doped silicon wafer (0.01 – 0.02 Ω -cm) with about 500 nm of grown WTO, on which a thin layer (about 7 – 8 nm) of silicon dioxide is formed. An adhesion layer 222 of titanium nitride (about 0.5 nm) is formed over the silicon dioxide.

[0029] The source 212 is formed of a body of source material 230 disposed on the substrate 20.

[0030] Examples of source materials include various metals or other conductors, such as nickel, tungsten, ruthenium, molybdenum, copper, cobalt, titanium nitride, *etc.* Further examples of source materials include heavily doped n-type materials, degenerate n-type silicon, and III-V compound semiconductors with high conductivity with predominately n-type or electron transport, *etc.*

[0031] In this example, the body of source material 230 is ruthenium that is formed by sputtering to a thickness of about 25 nm.

[0032] The drain 214 is formed of a body of drain material 230 and has the same or similar material and/or structure as the source 212. In other examples, the drain 214 has a material and/or structure different to the source 212.

[0033] The adhesion layer 222 promotes the adhesion of the bodies of source and drain material 230, 232 to the substrate 220. In other examples, the adhesion layer 222 may be omitted if the source/drain material has suitable adhesion without it.

[0034] The TFT 200 further includes a body of channel material 250 disposed between the source 212 and drain 214. In this example, the body of channel material 250 is disposed partially over the bodies of source and drain material 230, 232 and over the substrate 220 between the bodies of source and drain material 230, 232. The channel material is a layer tin oxide (SnO_2) that may have a thickness of about 5 nm to about 10 nm. In this example, the layer of tin oxide is about 7 nm thick.

[0035] The TFT 200 further includes a gate dielectric stack 116, as discussed above, which is disposed over the body of channel material 250.

[0036] The TFT 200 further includes a body of gate material 254 (also termed "gate metal") disposed over the gate dielectric material 254. The gate material is a conductor. Examples of gate materials include tungsten, titanium, titanium nitride, molybdenum, gold, platinum, aluminum, nickel, copper, chromium, hafnium, indium, manganese, iron, vanadium, zinc, tantalum, or alloys/combinations thereof. Suitable combinations of such materials may also be used. In this example, the body of gate material 254 is a layer of tungsten about 30 nm thick.

[0037] The TFT 200 further includes a source electrode 260 as part of the source 212 and a drain electrode 262 as part of the drain 214. The source electrode 260 is in electrical contact with the body of source material 230 to provide current to the body of source material 230. Likewise, the drain electrode 262 is in electrical contact with the body of drain material 232 to receive

current to the body of source drain 232. Examples of materials for electrodes 260, 262 include the gate materials listed above.

[0038] In various examples, the body of source material 230 may optionally be subject to inline treatment, such as plasma treatment, anneal treatment, chemical or electro-chemical treatment, or similar. Different types of treatment may be combined. A treatment may be repeated two or more times.

[0039] The treatment may form a p-type or n-type source-channel interface 240 at the body of source material 230 and between the body of source material 230 and channel material 250. The source-channel interface 240 may tune the threshold voltage at which TFT 200 turns on, making the transistor operate in enhancement or depletion mode, to reduce leakage current through TFT 200 in the off state. The source-channel interface 240 may create a repository of complimentary excess positive or negative charge that functions to deplete the channel in at least the region of the body of channel material 250 adjacent the body of source material 230. In this manner, the source-channel interface 240 serves as a voltage-controlled electron transport barrier, resulting in substantially less current flow through body of channel material 250 when TFT 200 is in an off state. Further, the source-channel interface 240 may also serve to reduce stress induced leakage currents ("SILC") in TFT 200 by inhibiting the formation of interlayer stress-induced flaws between the body of channel material 250 and the body of source material 230. A drain-channel interface 242 may be similarly formed and may have similar characteristics, but it is contemplated that the source-channel interface provides 240 a significant benefit without the drain-channel interface 242 and may provide most or all of the benefit.

[0040] In this example, the bodies of source and drain material 230, 232 are treated with oxygen plasma to form a layer of oxidized material that are the source and drain channel interfaces 240, 242.

[0041] As will now be apparent, the present invention provides a gate stack for a field effect transistor to reduce net charge in the dielectric material of the gate stack adjacent the semiconductor material of the transistor. The gate stack includes a gradient region between the dielectric layer abutting the semiconductor material and the diffusion barrier abutting the gate material, wherein the stoichiometry of the materials in the gradient region changes from the stoichiometry of the dielectric material to the stoichiometry of the diffusion barrier while avoiding

abrupt changes in stoichiometry. In addition, the gate stack may be tailored to tune the threshold voltage of the transistor.

[0042] The above-described embodiments and aspects of the invention are intended to be examples of the present invention and alterations and modifications may be effected thereto, by those of skill in the art, without departing from the scope of the invention which is defined solely by the claims appended hereto.

We claim:

1. A field effect transistor comprising:
 - a source;
 - a drain;
 - a semiconductor extending between the source and the drain;
 - a gate located over the semiconductor; and
 - a gate stack formed between the semiconductor material and the gate, the gate stack including a dielectric layer abutting the semiconductor material, and a diffusion barrier layer abutting the gate, the gate stack including a gradient region between the dielectric layer and the diffusion barrier wherein the stoichiometry of the materials in the gradient region changes from the stoichiometry of the dielectric material to the stoichiometry of the diffusion barrier.
2. The transistor of claim 1 wherein the change in stoichiometry in the gradient region is substantially monotonic.
3. The transistor of claim 1 wherein the diffusion barrier also serves as an adhesion layer for the gate.
4. The transistor of claim 1 wherein the materials in the gradient region have stoichiometric ratios in the form of XO_iN_j where X is the base material, O_i is the oxygen content and N_j is the nitrogen content.
5. The transistor of claim 4 wherein the base material X is hafnium.
6. The transistor of claim 4 wherein the base material X is zirconium.
7. The transistor of claim 1 wherein the semiconductor is tin oxide.
8. The transistor of claim 1 wherein the semiconductor is IGZO.

9. A gate stack for use in a field effect transistor having a source, a drain a semiconductor connecting the source and the drain and having a gate located over the semiconductor, comprising:
- a dielectric material abutting the semiconductor;
 - a diffusion barrier abutting the gate; and
 - a gradient material between the dielectric material and the diffusion barrier, the gradient region comprising a graded transition between the dielectric material and the diffusion barrier to reduce stress between the dielectric material and the diffusion barrier.
10. The gate stack of claim 9 where the dielectric material has the form of XO_i , the diffusion barrier has the form XN_j and the gradient material has the form XO_iN_j , where i decreases and j increases in the gradient region, from the region adjacent the dielectric material to the region adjacent the diffusion barrier.
11. The gate stack of claim 10 wherein X is hafnium.
12. The gate stack of claim 11 wherein the diffusion barrier also acts as an adhesion layer for the gate.