ABSTRACT

METHOD OF FABRICATION OF A RAISED SOURCE/DRAIN TRANSISTOR

A method of fabricating a transistor, comprising the following steps. A silicon semiconductor substrate having a pad oxide portion within an active area is provided. A polysilicon layer is deposited over the silicon semiconductor substrate and over the pad oxide portion. A pad oxide layer is deposited over the polysilicon layer. Shallow isolation trench regions are formed on either side of the active area. The pad oxide layer is removed. The polysilicon layer is etched and removed over the pad oxide portion leaving polysilicon portions between the pad oxide portion and the shallow isolation trench regions. The pad oxide portion is replaced with a gate oxide portion. A gate conductor, having exposed side walls, is formed over the gate oxide portion and between the polysilicon portions. Sidewall spacers are formed on the exposed side walls of the gate conductor with the sidewall spacers contacting the polysilicon portions. Source/drain regions are formed in the active area under the sidewall spacers and under the polysilicon portions. A salicide portion is formed over the gate conductor and salicide portions are formed over the polysilicon portions, whereby the formation of the salicide layers over the polysilicon portions consumes a portion of the polysilicon portions leaving the remainder of the polysilicon layers to form shallow source/drain junctions underneath the polysilicon portion salicide portions.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)