

CLAIMS:

1. A method for fabricating a multi-color light emitting pixel unit, comprising:
 - forming a stack structure on a substrate, the stack structure comprising a first metal layer, a first type of light emitting layer, a second metal layer, and a second type of light emitting layer in an order from bottom to top;
 - patterning the second type of light emitting layer and the second metal layer until a portion of the first type of light emitting layer is exposed; and
 - selectively etching the stack structure to form a first light emitting transistor and a second light emitting transistor, the first light emitting transistor including the first metal layer and the first type of light emitting layer, and the second light emitting transistor including the first metal layer, the first type of light emitting layer, the second metal layer, and the second type of light emitting layer.
2. The method of claim 1, wherein the forming the stack structure on the substrate comprises:
 - forming the first metal layer and the first type of light emitting layer on the substrate from bottom to top of the substrate;
 - forming a first metal bonding layer on top of the first type of light emitting layer;
 - forming the second type of light emitting layer and a second metal bonding layer on a first base from bottom to top of the first base;
 - bonding the first metal bonding layer and the second metal bonding layer to form the second metal layer; and
 - removing the first base.
3. The method of claim 2, wherein the forming the first metal layer and the first type of light emitting layer on the substrate from bottom to top of the substrate comprises:
 - forming a third metal bonding layer on the substrate;
 - forming the first type of light emitting layer and a fourth metal bonding layer on a second base from bottom to top of the first base;
 - bonding the third metal bonding layer and the fourth metal bonding layer to form the first metal layer; and
 - removing the second base.
4. The method of claim 2, further comprising:
 - before forming the first metal bonding layer on top of the first type of light emitting layer, thinning the first type of light emitting layer.
5. The method of claim 2, further comprising:
 - thinning the second type of light emitting layer.
6. The method of claim 2, further comprising:
 - forming micro-gap structures in at least one of the first type of light emitting layer or the second type of light emitting layer.

7. The method of claim 2, further comprising:
forming micro-gap structures in both of the first type of light emitting layer and the second type of light emitting layer,
- 5 wherein the micro-gap structures in the first type of light emitting layer are staggered relative to the micro-gap structures in the second type of light emitting layer.
8. The method of claim 1, further comprising:
electrically connecting the first metal layer and the second metal layer in the second light emitting transistor.
- 10 9. The method of claim 8, wherein the electrically connecting the first metal layer and the second metal layer in the second light emitting transistor comprises:
removing a portion of the second type of light emitting layer in the second light emitting transistor, so as to expose a top portion of the second metal layer in the second light emitting transistor;
and
- 15 forming an electrical connector on the exposed top portion and a side wall of the second metal layer in the second light emitting transistor, and on side walls of the first type of light emitting layer and the first metal layer in the second light emitting transistor.
10. The method of claim 1, further comprising:
forming a top electrode layer on top of the first light emitting transistor and the second light
- 20 emitting transistor.
11. The method of claim 1, wherein the forming the top electrode on top of the first light emitting transistor and the second light emitting transistor comprises:
forming an isolation layer covering the first light emitting transistor and the second light emitting transistor;
- 25 forming a first opening and a second opening in the isolation layer, the first opening exposing a portion of the first type of light emitting layer in the first light emitting transistor, and the second opening exposing a portion of the second type of light emitting layer in the second light emitting transistor; and
forming the top electrode layer on the substrate, the top electrode layer contacting the first type of light emitting layer in the first light emitting transistor via the first opening and contacting the second type
- 30 of light emitting layer in the second light emitting transistor via the second opening.
12. The method of claim 1, wherein the stack structure further comprises a third metal layer formed on top of the second type of light emitting layer, and a third type of light emitting layer formed on top of the third metal layer,
the method further comprising patterning the third type of light emitting layer and the third metal
- 35 layer until a portion of the second type of light emitting layer is exposed, and
the selectively etching the stack structure further comprising selectively etching the stack structure to form the first light emitting transistor, the second light emitting transistor, and a third light

emitting transistor, the third light emitting transistor including the first metal layer, the first type of light emitting layer, the second metal layer, the second type of light emitting layer, the third metal layer, and the third type of light emitting layer.

5 13. The method of claim 12, wherein the forming the stack structure on the substrate comprises:
forming the first metal layer, the first type of light emitting layer, the second metal layer, the second type of light emitting layer on the substrate from bottom to top;

forming a first metal bonding layer on the second type of light emitting layer;

forming the third type of light emitting layer and a second metal bonding layer on a base from bottom to top of the base;

10 bonding the first metal bonding layer and the second metal layer to form the third metal layer;
and

removing the base.

14. The method of claim 12, further comprising:

15 thinning at least one of the first type of light emitting layer, the second type of light emitting layer, or the third type of light emitting layer.

15. The method of claim 12, further comprising:

forming micro-gap structures in at least one of the first type of light emitting layer, the second type of light emitting layer, or the third type of light emitting layer.

16. The method of claim 12, further comprising:

20 forming micro-gap structures in all of the first type of light emitting layer, the second type of light emitting layer, and the third type of light emitting layer,

wherein the micro-gap structures in the first type of light emitting layer are staggered relative to the micro-gap structures in the second type of light emitting layer, and

25 wherein the micro-gap structures in the second type of light emitting layer are staggered relative to the micro-gap structures in the third type of light emitting layer.

17. The method of claim 12, further comprising:

electrically connecting the first metal layer and the second metal layer in the second light emitting transistor, and electrically connecting the first metal layer, the second metal layer, and the third metal layer in the third light emitting transistor.

30 18. The method of claim 17, wherein the electrically connecting the first metal layer and the second metal layer in the second light emitting transistor, and electrically connecting the first metal layer, the second metal layer, and the third metal layer in the third light emitting transistor comprises:

removing a portion of the second type of light emitting layer in the second light emitting transistor, so as to expose a top portion of the second metal layer in the second light emitting transistor;

35 removing a portion of the third type of light emitting layer in the third light emitting transistor, so as to expose a top portion of the third metal layer in the third light emitting transistor;

forming a first electrical connector on the exposed top and a side wall of the second metal layer in

the second light emitting transistor, and on side walls of the first type of light emitting layer and the first metal layer in the second light emitting transistor; and

- 5 forming a second electrical connector on the exposed top and a side wall of the third metal layer in the third light emitting transistor, and on side walls of the second type of light emitting layer, the second metal layer, the first type of light emitting layer, and the first metal layer in the third light emitting transistor.

19. The method of claim 12, further comprising:

forming a top electrode layer on top of the first light emitting transistor, the second light emitting transistor, and the third light emitting transistor.

- 10 20. The method of claim 19, wherein the forming a top electrode layer on top of the first light emitting transistor, the second light emitting transistor, and the third light emitting transistor comprises:

forming an isolation layer covering the first light emitting transistor, the second light emitting transistor, and the third light emitting transistor;

- 15 forming a first opening, a second opening, and a third opening in the isolation layer, the first opening exposing a portion of the first type of light emitting layer in the first light emitting transistor, the second opening exposing a portion of the second type of light emitting layer in the second light emitting transistor, and the third opening exposing a portion of the third type of light emitting layer in the third light emitting transistor; and

- 20 forming the top electrode layer on the substrate, the top electrode layer contacting the first type of light emitting layer in the first light emitting transistor via the first opening, contacting the second type of light emitting layer in the second light emitting transistor via the second opening, and contacting the third type of light emitting layer in the third light emitting transistor via the third opening.