CORRECTED VERSION*

PCT

WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : H01L 21/00 | A2

(11) International Publication Number: WO 00/13211

(43) International Publication Date: 9 March 2000 (09.03.00)

(21) International Application Number: PCT/US99/19958

(22) International Filing Date: 31 August 1999 (31.08.99)

(30) Priority Data:
60/098,902 2 September 1998 (02.09.98) US

(71) Applicant: MEMC ELECTRONIC MATERIALS, INC. [US/US]; 501 Pearl Drive, P.O. Box 8, St. Peters, MO 63376 (US).

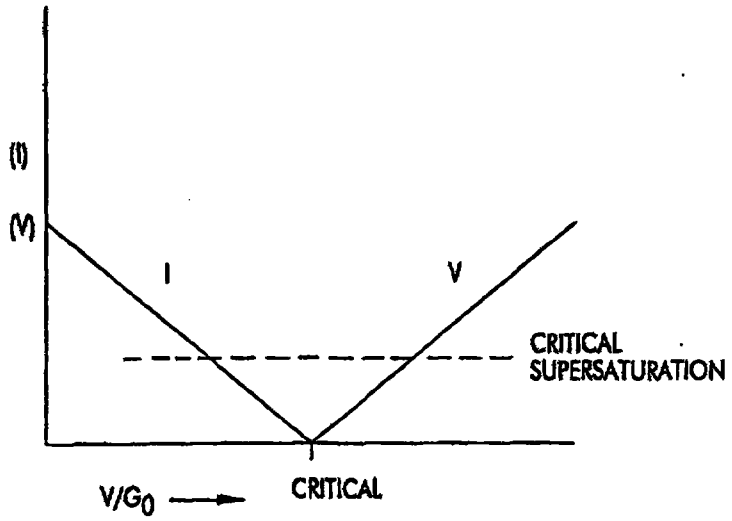
(72) Inventor: FALSTER, Robert, J.; Via Caradosso, 11, I-20123 Milano (IT).

(74) Agents: HEILEK, Edward, J. et al.; Senniger, Powers, Leavitt & Roedel, 16th floor, One Metropolitan Square, St. Louis, MO 63102 (US).

(81) Designated States: CN, JP, KR, SG, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
Without international search report and to be republished upon receipt of that report.

(54) Title: SILICON ON INSULATOR STRUCTURE FROM LOW DEFECT DENSITY SINGLE CRYSTAL SILICON



(57) Abstract

The present invention relates to a silicon on insulator ("SOI") structure having a low defect density device layer and, optionally, a handle wafer having improved gettering capabilities. The device layer comprises a central axis, a circumferential edge, a radius extending from the central axis to the circumferential edge, and a first axially symmetric region which is substantially free of agglomerated intrinsic point defects. Additionally, the present invention is directed to such a SOI structure which has a Czochralski single crystal silicon handle wafer which is capable of forming an ideal, non-uniform depth distribution of oxygen precipitates upon being subjected to the heat treatment cycles of essentially any arbitrary electronic device manufacturing process.

*(Referred to in PCT Gazette No. 22/2000, Section II)