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PROCESSOR ARCHITECTURE

ABSTRACT OF THE DISCLOSURE

A processing system comprises a multiport memory module having N ports, N data communication buses, and N hardware acceleration modules that communicate with a respective one of the N ports on a respective one of the N data communication buses. A first one of the N hardware acceleration modules performs a first processing task on data and transmits the data to the multiport memory module on a first one of the N data communication buses. A second one of the N hardware acceleration modules receives the data from the multiport memory module on a second one of the N data communication buses and performs a second processing task on the data. N is an integer greater than one.

FIG. 5