

TECHNIQUES TO IMPLEMENT TWO-DIMENSIONAL COMPRESSION

RELATED APPLICATION

5 This patent application is related to concurrently filed US Patent Application Serial No. _____, titled "Techniques to Implement One-Dimensional Compression," by Acharya, (attorney docket no. 042390.P9921), assigned to the assignee of the present invention and herein incorporated by reference.

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BACKGROUND

 The present disclosure is related to two-dimensional image compression, such as for bi-level image compression.

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 As is well-known, a facsimile machine scans a document line by line and converts each line to alternating black and white dots. The resulting document image is referred to as bi-level because each pixel is represented by a single bit and its value may be either 0 to represent a black dot, or 1 to represent a white dot or pixel. A combination of
20 run-length encoding and modified Huffman coding has been found suitable to compress such bi-level images. The International Telecommunications Union (ITU, formerly known as Consultative Committee on International Telephone and Telegraph - CCITT) has, therefore, provided a number of standards or specifications suitable to compressing such bi-level facsimile images. See, for example, Hunter, et. al., International Digital Facsimile
25 Coding Standards, Proceedings of the IEEE Vol. 68, No. 7, July 1980, pages 854-857. The CCITT Group 4 is one such standard and applied to digital facsimile or "fax"

machines. The recommendations for Group 4 includes a two dimensional coding scheme. In the two dimensional scheme , the coding of each scan line is performed based, at least in part on the previous scan line, referred to as a reference scan line. Although this standard was recommended for facsimile machines, the approach is also
5 suitable for coding bi-level document images in various other applications, such as, for example, in photocopying machines, scanners, etc.

In photocopying or facsimile systems, the performance of the system may be measured in terms of the number of pages copied per minute. It is difficult to specify
10 copying time per page because this time may vary with the content of the page. However, improving the encoding rate to achieve higher pages per minute is desirable in order to improve performance.

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BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter regarded as the invention is particularly pointed out and
20 distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects, features, and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanying drawings in which:

25 FIG. 1 is a schematic diagram illustrating an embodiment of a circuit to implement two-dimensional compression in accordance with the present invention;

FIG. 2 is a schematic diagram illustrating a portion of the embodiment of FIG. 1 in more detail;

5 FIG. 3 is a table illustrating codes employed for one-dimensional coding applied to bi-level image compression;

FIG. 4 is a schematic diagram of a portion of a reference scan line and a portion of a scan line to be coded; to illustrate definitions employed in CCITT Group 4 bi-level
10 image compression; and

FIG. 5 is a flowchart illustrating implementation of CCITT Group 4 bi-level image compression, using the definitions illustrated in FIG. 4

15 DETAILED DESCRIPTION

In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the invention. However, it will be understood by those skilled in the art that the present invention may be practiced without
20 these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in detail so as not to obscure the present invention.

As previously described, the ITU has provided a specification or standard known as CCITT Group 4 that is employed to compress bi-level facsimile images (hereinafter
25 also referred to as "G4"). Although this standard was recommended for facsimile machines, the approach is also suitable for coding bi-level document imaging

applications, such as in photocopying machines, scanners, etc. One issue that has led to compliance with this standard is the timing and synchronization of information to meet communications requirements through the telecommunications channel. Despite this issue, improving the encoding rate to improve the performance of a photocopying system in terms of the number of pages copied is desirable. The encoding rate may be improved, for example, by implementing high speed circuits designed to exploit features of the compression approach employed, as described in more detail hereinafter.

FIG. 3 is a table illustrating variable length binary codes that may be employed when complying with the one-dimensional mode in the CCITT Group 3 standard for bi-level image compression (hereinafter also referred to as "G3"). When one dimensional compression coding is applied in a manner to comply with the aforementioned standard, a scan line is compressed by coding the length of each one of alternating 'runs' of black or white pixels using a pre-specified static Huffman code. Separate code tables are used for black and white runs because the respective statistical distributions are different. Each code table may represent a run-length of up to 1,728 pixels, the maximum length of a scan line in the bi-level image. The first 64 entries of the code table is a Huffman code of run-length 0 to 63, respectively. The 64 codes are referred to in this context as termination codes (TC). A binary code of a run-length (L) bigger than 63 is represented using two parts or two codes, a makeup code (MUC) and a termination code (TC). The run length (L) is represented by

$$L = 64 \cdot N + K,$$

the code for L is the MUC to represent $64 \cdot N$, followed by the TC to represent K. There are 27 entries for the MUCs to represent 64, 128, 192, 256, ..., 1728, respectively (27 multiples of 64), in the code table followed by the first 64 codes for the TC. Hence, the

code table has a total of 91 entries for each color, assuming that 1728 is the maximum length permitted in the CCITT Group 3 standard. As will be explained in more detail hereinafter, G4 two-dimensional image compression employs aspects of G3 one-dimensional image compression, particularly when a mode, referred to as "horizontal
5 mode" is employed.

FIG. 4 is a schematic diagram employed to illustrates commonly used definitions that apply to the CCITT Group 4 standard for two-dimensional bi-level image compression. As illustrated in FIG. 4, five positions, denoted a0, a1, a2, b1, and b2, are
10 shown. These designations, as employed in the flowchart of FIG. 5, described in more detail below, have the following interpretation when employed in this context:

a0 indicates position of the first pixel of a new code word in the coding line, and may be black or white, as shown in FIG. 4;

15 a1 indicates position of the first pixel to the right of a0 in the coding line with a different color, as shown in FIG. 4;

a2 indicates position of the first pixel to the right of a1 in the coding line with a different color, as shown in FIG 4;

b1 indicates position of the first pixel in the reference line to the right of a0 with a
20 different color, as shown in FIG. 4; and

b2 indicates position of the first pixel in the reference line to the right of b1 with a different color, as shown in FIG. 4.

FIG. 5 is a flow chart 500 illustrating the coding approach implemented by the G4
25 standard, in which the current scan line or row of a binary image, referred to as the coding line in this context, is compared with the immediately preceding scan line or row of

the binary image, referred to as the reference line in this context. It is assumed, for convenience, when applying this approach, that at the beginning of coding the reference line comprises all white pixels, although the invention is not limited in scope in this respect. After coding the first scan line, that line becomes the reference line, and the
 5 next scan line becomes the coding line. This continues until the entire image has been encoded.

As FIG. 5 illustrates, there are three primary modes that may be employed when coding a scan line. In this context, they are referred to, respectively, as pass mode,
 10 vertical mode, and horizontal mode. Using the definitions provided above, as illustrated in flow chart 500 by diamond 510, pass mode applies if the position of b2 is to the left of the position of a1. When this mode occurs, a fixed code word "0001" is produced to indicate pass mode. Furthermore, as indicated by block 520, the position of a0 is changed to the current position of b2. As illustrated by diamond 530, vertical mode
 15 applies if the distance between a1 and b1 is less than or equal to three. If this mode applies, then a code word is produced to indicate the location of a1 with respect to b1. Therefore, the following seven codes are possible in this mode:

- V(0) = "1" indicates that a1=b1 in terms of position;
- 20 V(-1) = "011" indicates the pixel a1 is to the right of pixel b1 by 1 pixel;
- V(-2) = "000011" indicates the pixel a1 is to the right of pixel b1 by 2 pixels;
- V(-3) = "0000011" indicates the pixel a1 is to the right of pixel b1 by 3 pixels;
- V(1) = "010" indicates the pixel a1 is to the left of pixel b1 by 1 pixel;
- V(2) = "000010" indicates the pixel a1 is to the left of pixel b1 by 2 pixels;
- 25 V(3) = "0000010" indicates the pixel a1 is to the left of pixel b1 by 3 pixels.

The third and last mode, horizontal mode, illustrated by diamond 540, applies otherwise, which, in this context, means the distance between a1 and b1 is more than 3 and b2 is to the right of a1. If this mode applies, a fixed code word "001" is produced. This is then followed by a code word to indicate the distance between pixel locations a0 and a1, and, 5 then another code word to indicate the distance between pixel locations a1 and a2. As noted previously, in this context, the code words for the CCITT Group 3 one-dimensional compression standard, such as those illustrated in FIG. 3, are employed to generate the codes for the run length between pixel locations a0 and a1 and for the run length between pixel locations a1 and a2.

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FIG. 1 is a schematic diagram illustrating an embodiment of a circuit to implement two dimensional compression in accordance with the present invention. Although the invention is not restricted in scope in this respect, embodiment 100 is illustrated as implemented on an integrated circuit (IC) chip. As illustrated in FIG. 1, embodiment 100 15 includes digital logic circuitry, including, in this particular embodiment, registers, buffers, and digital memories. For example, although the invention is not limited in scope in this respect, 110 comprises a FIFO buffer; 120, 130, 140, 150, and 160 comprise registers; 185 comprises a multiplexer (MUX); and 195 comprises a digital delay element. Likewise, other examples of the digital logic circuitry include XOR gate 170, toggle switch 20 180, and binary counter 190. It will, of course, be appreciated that the invention is not limited in scope to this particular digital logic circuitry and digital memories or to this particular configuration of such components. Nonetheless, as shall be explained in more detail hereinafter, in this embodiment, the digital memories and digital logic circuitry are coupled so as to implement two dimensional compression of a bit stream to be applied to 25 the digital logic circuitry and digital memories.

It is noted that a host of two-dimensional compression processes may be implemented in this particular embodiment in accordance with the invention or in other embodiments in accordance with the invention. Nonetheless, this particular embodiment has the capability to comply with the two-dimensional coding scheme of the CCITT Group 4, bi-level compression standard. Again, although the invention is not limited in scope in this respect, digital read only memories may be employed, for example, to generate the appropriate code words in accordance with the CCITT Group 3 one-dimensional coding scheme, as may occur when horizontal mode applies. Although the invention is not limited in scope in this respect, one approach for implementing this code scheme that may be employed is described in the aforementioned US Patent Application Serial No. _____ (attorney docket 042390.P9921). Of course, alternative approaches may also be employed and still fall within the scope of the present invention.

Referring now to FIG. 1, when a bit stream is applied to this particular embodiment of a circuit to two-dimensional compression, here embodiment 100, the following operation occurs. On each successive pulse of a clock, such as an external clock, here, designated clock 115, the next successive bit of the bit stream is applied to buffer 125. It is assumed, in this particular embodiment, clock 115 comprises an externally derived clock, although, of course, the invention is not necessarily limited in scope in this respect. As clock 115 applies successive pulses, the bit of the bit stream is applied to XOR circuit 170. Likewise, however, the bits are also applied to delay element 195. Therefore, in this embodiment, XOR circuit 170 is employed to compare two consecutive bits of a bit stream, the current bit and the previous bit delayed by one clock cycle through delay element 195, which, in this particular embodiment, comprises a flip-flop, although, of course, the invention is not limited in scope in this respect.

In this embodiment, if the two bits of the bit stream compared by XOR circuit 170 are identical, circuit 170 produces a "0" output signal. However, once an input bit is received having a binary value the opposite of the immediately previous bit, the circuit provides a "1" output signal. Therefore, 170, in this particular embodiment, signals the
5 end of a run of pixels of a particular color, here, either black or white. The output signal of 170 is applied to toggle switch 180. In this particular embodiment, although the invention is not limited in scope in this respect, the switch is implemented also using a flip-flop, referred to as a Toggle or T flip-flop. The output signal of 180 is toggled when an output signal from 170 applied to 180 comprises a "1." In this particular embodiment,
10 170 and 180 are initialized to "1" to indicate that initially the runs comprise white pixels, although, this is merely a convention employed for convenience, and an alternative embodiment having a different initialization may be employed. Therefore, when toggle switch 180 toggles to "0," this indicates the end of a run of white pixels and the beginning of a run of black pixels. The output signals of toggle switch 180 remain "0" until the end
15 of the run of black pixels is detected, as indicated by the output signal of 170, in which case toggle switch 180 toggles back to "1." Therefore, in this embodiment, in addition to signaling the end of a run of pixels of a particular color, toggle switch 180 also signals the color of the run, in this embodiment, 0 for a black run, and 1 for a white run, although, of course, the invention is not limited in scope in this respect.

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In this particular embodiment, binary counter 190 comprises a binary up counter, although, of course, the invention is not limited in scope in this respect. Counter 190, as illustrated in FIG. 1, counts the length of the run of a particular color. At the end of the run, that is, in this embodiment, when the output signal of 170 is "1," counter 190 is reset
25 to "0." When the run ends, the length of the run is the output signal of counter 190, which, in this particular embodiment, is loaded into register 120 by application of the

output signal of XOR circuit 170 to register 120. This, then, indicates the position of a2 in the scan line, which is loaded into register 120, while at the same time, again signaled by the output signal of XOR circuit 170, the previous contents of register 120 are loaded into register 130, indicating the position of a1 in the scan line.

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As FIG. 1 illustrates, register 140 stores the current position of a0; however, as illustrated by the flow chart in FIG. 5, this may comprise any one of the values a1, a2, and b2, depending upon the mode applicable. In FIG. 1, MUX 185 implements this aspect of the mode selection technique, depending, in this embodiment, on the specific values of control signals SEL(0) and SEL(1) applied to the MUX. FIG. 1 also illustrates that these control signals are generated by circuit C, designated 175 in FIG. 1. This specific circuit is described in more detail hereinafter and is illustrated in more detail in FIG. 2.

One aspect of this particular embodiment of the invention is the use of FIFO buffer 110. This conserves resources in terms of circuit complexity, memory, and speed because, instead of storing an entire reference scan line, specific position locations, such as b1 and b2, are stored. Therefore, at the beginning of encoding the coding line, the FIFO stores the positions of the end of successive color runs in the current reference scan line. As encoding takes place, counter 190, as previously described, indicates the position of the end of a color run in the coding line once circuit 170 produces a "1" output signal. When this occurs, as illustrated in FIG. 1, for this embodiment, the value of the counter is "pushed" into FIFO 110 using control signal "PUSH," which, in this particular embodiment, is the output signal produced by circuit 170. Thus, another position of the end of a color run in the coding line is stored when successive bits from the coding line being input to be coded change state. With this approach, the first two values or

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elements stored in FIFO 110 at any particular time comprise two consecutive positions of two consecutive ends of color runs in the reference line. Likewise, FIFO buffer 110 is advanced when a value is loaded into register 140. As described in more detail below, this generally signals that a code word to be output is generated. Again, as illustrated in FIG. 1, control signal "POP" is applied and the first entry of FIFO 110 is loaded into register 160, indicating the value of b2. Likewise, the previous content of register 160 is loaded into register 150, indicating the current value of b1.

A truth table for control signals SEL(0) and SEL(1), for this embodiment, and the output signal produced by MUX 185 when these control signals are applied, is illustrated in FIG. 1. FIG. 2 illustrates the process and logic through which these signals are produced and its relationship to the three modes of operation discussed previously in connection with the flow chart in FIG. 5. FIG. 2 specifically illustrates schematically 175, that is, here, circuit C, for this particular embodiment. Circuit C, therefore, supplies the control signals employed to implement the flow chart shown in FIG. 5.

As shown in FIG. 5, the value of b2 is assigned to a0 when $b2 < a1$. In FIG. 2, subtractor circuit 205 computes $(a1 - b2)$. Therefore, the sign bit of the difference being a 0 value indicates that SEL(0)=SEL(1)=0, and, therefore, b2 is selected as the output signal of MUX 185. Position b2 is loaded into register 140 in FIG. 1 and application of control signals SEL(0) and SEL(1) to MUX 220 in FIG. 2 produces the code word for pass mode. It is noted that the generation of the code words, indicated in FIG. 2, may be accomplished any one of a variety of ways. One convenient approach would employ digital read-only memories in a table look-up capacity.

Referring again to FIG. 2, the output signal of absolute difference circuit 230 computes the value of $|a1-b1|$. The condition where this value exceeds three is detected by a logical OR operation applied to all but the least significant two bits of the output signal of circuit 230. Taking its complement produces the control signal $SEL(0)=0$,
5 while $SEL(1)=1$. As indicated by the truth table in FIG. 1, this results in $a2$ being loaded into register 140. Horizontal mode is being employed, and, therefore, the previous description of the CCITT Group 3 one-dimensional compression standard applies. Furthermore, as previously indicated, although the invention is not limited in scope in this respect, the approach employed in the aforementioned patent application
10 _____(attorney docket 042390.P9921) may be used to implement the desired code words.

Otherwise, $SEL(0)=1$ and $SEL(1)=0$ and the value of $a1$ is loaded into register 140. Therefore, a code word corresponding to the relative positions of $a1$ and $b1$, for
15 vertical mode, is produced. Again, one convenient technique would employ digital read-only-memories in a table look-up capacity, so that, for example, depending on the difference of $a1$ and $b1$, the desired code word is generated. Of course, a host of techniques are possible to generate the desired code words and the invention is not limited to a particular approach.

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It is noted that FIG. 2 illustrates schematically that the appropriate signals may be provided to portions of 175, or circuit C, to generate the appropriate or applicable code words for pass mode, vertical mode, and horizontal mode, so that MUX 220 may supply the appropriate or applicable code wording for outputting and packing, etc. For example,
25 as illustrated in FIG. 2, signals $a0$, $a1$, $a2$, $b1$, $b2$, and P are provided to 175. As previously discussed, $a1$, $b1$, and $b2$ may be employed to generate control signals

SEL(0) and SEL(1). In horizontal mode, the code word generated is a concatenation of three codes, a fixed code "001", followed by a binary code word to indicate the run length (a1-a0) of color P, followed by a binary code word to indicate the run length of (a2-a1) of color complement of P. Likewise, in vertical mode, the code word generated is selected
5 from the codes described previously regarding the value of (a1-b1), which may be obtained for example, from circuit 230, and the sign of (a1-b1). In pass mode, as previously described, a fixed binary code word "0001" is produced. It is, of course, appreciated that this is just one particular embodiment of the present invention. The invention is not limited in scope to these details, such as, for example, if a two-
10 dimensional compression approach other than G4 were employed.

Although the invention is not limited in scope in this respect, one advantage of the embodiment illustrated in FIGs. 1 and 2 is that a two-dimensional compression process, in this embodiment the CCITT Group 4 bi-level compression process, has been
15 implemented without employing any arithmetic operations. In this context, arithmetic operations are distinguished from digital logic operations. Arithmetic operations typically involve a higher level of circuit complexity to implement in order to perform, for example, carries as well as other more complex operations. Therefore, not employing arithmetic operations provides a number of advantages. It allows the two dimensional
20 compression process to be implemented with a lower complexity circuit architecture, which has the associated advantages of lower power and lower cost. In addition, although this invention is not limited in scope in this respect, this particular embodiment should also achieve a higher encoding rate, which should result in higher pages per minute of performance, as previously described. A reason this particular embodiment
25 should result in faster encoding is because, typically, the implementation of arithmetic operations will introduce additional delay not present for the embodiment illustrated in

FIGs. 1 and 2. Therefore, this particular embodiment of a circuit to implement two-dimensional compression provides a number of advantages over alternative approaches, such as, for example, approaches employing a general purpose microprocessor to implement such compression processes.

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While certain features of the invention have been illustrated and detailed herein, many modifications, substitutions, changes and equivalents will now occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.

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Claims:

1. An integrated circuit comprising:
digital logic circuitry and digital memories;
said digital logic circuitry and digital memories being coupled so as to implement
5 two dimensional compression of successive scan lines to be applied to said digital
logic circuitry and digital memories.
2. The integrated circuit of claim 1, wherein a circuit configuration of said digital logic
circuitry and digital memories is coupled to implement said two dimensional
10 compression of successive scan lines without performing arithmetic operations.
3. The integrated circuit of claim 1, wherein said two dimensional compression to be
implemented complies with the CCITT Group 4 bi-level image compression
standard.
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4. The integrated circuit of claim 3, wherein said digital logic includes a FIFO buffer
coupled so as to store respective positions of the end of successive color runs in
the current reference scan line.
- 20 5. The integrated circuit of claim 4, wherein said FIFO buffer is coupled so that a
position of the end of a color run is stored when successive input bits from a scan
line to be coded change state.
6. The integrated circuit of claim 5, wherein the digital logic circuitry is coupled to
25 detect the change in state using a binary delay element and a logical exclusive
OR (XOR) circuit.

7. The integrated circuit of claim 5, wherein the FIFO buffer is coupled so that the position of the end of a color run is applied to the FIFO buffer by a binary counter.

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8. The integrated circuit of claim 5, wherein said FIFO buffer is coupled so that the position of the end of a color run is output of said FIFO buffer when a code to be output is generated.

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9. The integrated circuit of claim 2, wherein said FIFO buffer is coupled so that a position of the end of a color run is stored when successive input bits from a scan line to be coded change state.

- 15 10. The integrated circuit of claim 8, wherein the FIFO buffer is coupled so that the position of the end of a color run is applied to the FIFO buffer by a binary counter.

11. A method of implementing the compression of a two dimensional bit stream comprising:

- 20 storing respective positions of the end of successive color runs in the current reference scan line; and
comparing selected ones of those stored positions with selected ones of positions of the end of successive color runs in the scan line being coded.

12. The method of claim 11, wherein the position of the end of a color run in a scan line is stored when successive input bits from a scan line to be coded change state.
- 5 13. The method of claim 12, wherein the position of the end of a color run in a scan line is stored using an first in, first out (FIFO) convention.
14. The method of claim 13, wherein the position of the end of a color run is determined using a counter.
- 10 15. A document processing system comprising:
system components to perform bi-level compression of a document to be processed;
at least one of said system components including: digital logic circuitry and digital
15 memories coupled so as to implement two dimensional compression of
successive scan lines representing contents of the document to be processed.
16. The document processing system of claim 15, wherein said two dimensional
compression to be implemented complies with the CCITT Group 4 bi-level
20 compression standard.
17. The document processing system of claim 16, wherein the digital logic circuitry
includes a binary counter and a toggle switch;
said binary counter being coupled so as to count the length of a run; and
25 said toggle switch being coupled so as to signal the end and color of a run.