IN THE CLAIMS

We claim:

1. A method of forming a semiconductor package comprising:

providing a carrier having a conductive surface;

forming a first dielectric layer on the conductive surface of the carrier, the first dielectric layer having a die cavity exposing a die region on the conductive surface;

forming a layer of adhesive on the die region of the conductive surface;

attaching a die onto the layer of adhesive, the die having a back side secured to the layer of adhesive, and a front side having a plurality of die pads;

depositing a second dielectric layer onto the first dielectric layer and the die;

forming a plurality of die interconnects on the plurality of die pads at the front side of the die; and

removing the carrier to expose the layer of adhesive.

2. The method of claim 1, wherein forming the first dielectric layer further comprises:

forming a plurality of pad openings in the first dielectric layer, the plurality of pad openings exposing a plurality of pad regions on the conductive surface;

forming a plurality of package pads on the plurality of pad regions of the conductive surface; and

forming a plurality of package interconnects on the plurality of package pads.

3. The method of claim 2, wherein the first dielectric layer is a photo-definable dielectric material.

4. The method of claim 3, wherein the first dielectric layer is formed by:

laminating the photo-definable dielectric material onto the conductive surface; and

exposing the first dielectric layer to a radiation source and developing the first dielectric layer to define the die cavity and the plurality of pad openings in the first dielectric layer.

5. The method of claim 2, wherein forming the first dielectric layer comprises:

depositing the first dielectric layer on the conductive surface; and

defining the die cavity and the plurality of pad openings in the first dielectric layer.

6. The method of claim 5, wherein the die cavity and the plurality of pad openings are defined by an etching process.

7. The method of claim 5, wherein the die cavity and the plurality of pad openings are defined by a laser or mechanical drilling process.

8. The method of claim 2, wherein the plurality of package pads are formed by electrolytically plating the plurality of pad regions.

9. The method of claim 1, wherein the layer of adhesive is sprayed or screen printed onto the die region.

10. The method of claim 1, wherein forming the plurality of die interconnects comprises:

forming a first plurality of via openings in the second dielectric layer, the first plurality of via openings exposing the plurality of die pads at the front side of the die;

forming a metal layer into the first plurality of via openings and onto the plurality of die pads; and

etching the metal layer to form the plurality of die interconnects.

11. The method of claim 2, wherein forming the plurality of package interconnects comprises:

forming a second plurality of via openings in the dielectric layer, the second plurality of via openings exposing the plurality of package pads;

forming a metal layer into the second plurality of via openings and onto the plurality of package pads; and

etching the metal layer to form the plurality of package interconnects.

12. The method of claim 2, further comprising:

depositing a third dielectric layer onto the second dielectric layer; and

forming a plurality of interconnects on the plurality of die interconnects or on the plurality of package interconnects.

13. The method of claim 2, further comprising:

forming a solder resist layer over the second dielectric layer; and

forming a plurality of solder bumps, wherein the plurality of solder bumps are electrically coupled to the plurality of die interconnects or to the plurality of package interconnects.

14. A semiconductor package comprising:

a first package comprising:

a first dielectric layer having a top surface, and a cavity extended through the first dielectric layer;

a layer of adhesive formed in the cavity of the first dielectric layer, the layer of adhesive having an upper surface and a lower surface, wherein the upper surface is substantially coplanar to the top surface of the first dielectric layer;

a first die formed in the cavity, the first die having a front side and a back side, wherein the front side includes a plurality of die pads, and wherein the back side is adhered to the lower surface of the layer of adhesive;

a second dielectric layer formed over the bottom surface of the first dielectric layer and over the front side of the first die; and

a plurality of die interconnects electrically coupled to the plurality of die pads on the front side of the first die.

15. The semiconductor package of claim 14, further comprising:

a plurality of package pads formed in the first dielectric layer, wherein the plurality of package pads each comprises an exposed surface that is substantially coplanar to the top surface of the first dielectric layer; and

a plurality of package interconnects electrically coupled to the plurality of package pads.

16. The semiconductor package of claim 15, further comprising:

a second die adhered to the upper surface of the layer of adhesive in the first package; and

a plurality of wire-bonding interconnects that electrically couple the second die to the plurality of package pads of the first package.

17. The semiconductor package of claim 15, further comprising:

a second package comprising:

a third die; and

a plurality of interconnects that electrically couple the third die to the plurality of package pads in the first package.

18. The semiconductor package of claim 15, wherein the plurality of package pads comprise a composition of gold, palladium and nickel.

19. The semiconductor device of claim 14, further comprising:

a first plurality of solder bumps electrically coupled to the plurality of die interconnects.

20. The semiconductor device of claim 15, further comprising:

a second plurality of solder bumps electrically coupled to the plurality of package interconnects.

21. The semiconductor device of claim 14, further comprising a system comprising:

a bus is communicatively coupled to the structure; and

a DRAM communicatively coupled to the bus.

We claim:

1. A semiconductor package comprising:

a first package comprising:

a first dielectric layer having a top surface, and a cavity extended through the first dielectric layer;

a layer of adhesive formed in the cavity of the first dielectric layer, the layer of adhesive having an upper surface and a lower surface, wherein the upper surface is substantially coplanar to the top surface of the first dielectric layer;

a first die formed in the cavity, the first die having a front side, sidewalls, and a back side, wherein the front side includes a plurality of die pads, and wherein the back side is adhered to the lower surface of the layer of adhesive;

a second dielectric layer formed over a bottom surface of the first dielectric layer, extending into the cavity adjacent the die sidewalls, and over the front side of the first die;

a plurality of die interconnects electrically coupled to the plurality of die pads on the front side of the first die;

a plurality of package pads formed in the first dielectric layer, wherein the plurality of package pads each comprises an exposed surface that is substantially coplanar to the top surface of the first dielectric layer;

an additional die attached to the upper surface of the adhesive layer, wherein the additional die is in electrical contact with at least one of the package pads; and

a second package stacked over the additional die and attached to at least one of the package pads with a solder bump extending between the package and the at least one package pad.

2. The semiconductor package of claim 1, further comprising:

a plurality of package interconnects electrically coupled to the plurality of package pads.

3. The semiconductor package of claim 2, the second package further comprising:

a second die; and

a plurality of interconnects that electrically couple the second die to the plurality of package pads in the first package.

4. The semiconductor package of claim 1, wherein the plurality of package pads comprise a composition of gold, palladium and nickel.

5. The semiconductor device of claim 1, further comprising:

a first plurality of solder bumps electrically coupled to the plurality of die interconnects.

6. The semiconductor device of claim 2, further comprising:

a plurality of solder bumps electrically coupled to the plurality of package interconnects.

7. A system comprising:

a semiconductor device comprising:

a first package comprising:

a first dielectric layer having a top surface, and a cavity extended through the first dielectric layer;

a layer of adhesive formed in the cavity of the first dielectric layer, the layer of adhesive having an upper surface and a lower surface, wherein the upper surface is substantially coplanar to the top surface of the first dielectric layer;

a first die formed in the cavity, the first die having a front side, sidewalls, and a back side, wherein the front side includes a plurality of die pads, and wherein the back side is adhered to the lower surface of the layer of adhesive;

a second dielectric layer formed over a bottom surface of the first dielectric layer, extending into the cavity adjacent the die sidewalls, and over the front side of the first die;

a plurality of die interconnects electrically coupled to the plurality of die pads on the front side of the first die;

a plurality of package pads formed in the first dielectric layer, wherein the plurality of package pads each comprises an exposed surface that is substantially coplanar to the top surface of the first dielectric layer;

an additional die attached to the upper surface of the adhesive layer, wherein the additional die is in electrical contact with at least one of the package pads; and

a package stacked over the additional die and attached to at least one of the package pads with a solder bump extending between the package and the at least one package pad;

a bus is communicatively coupled to the first package; and

a DRAM communicatively coupled to the bus.