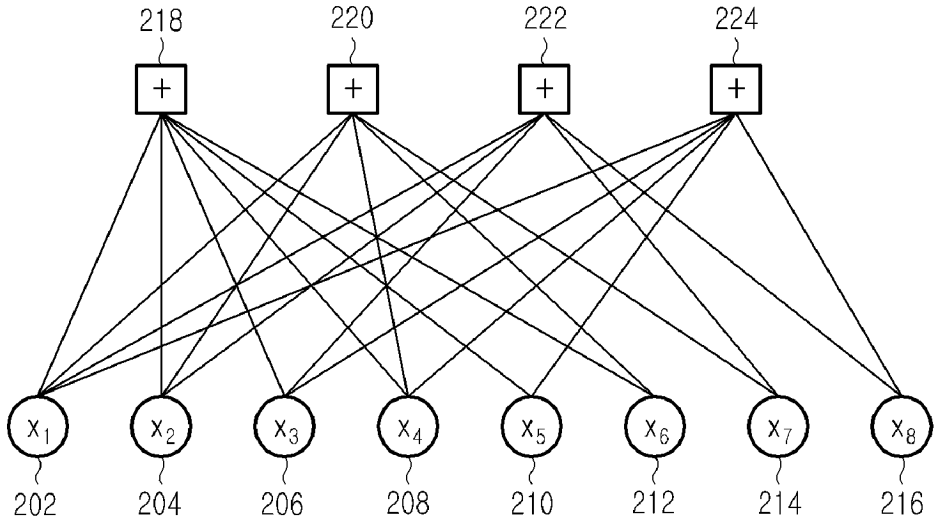
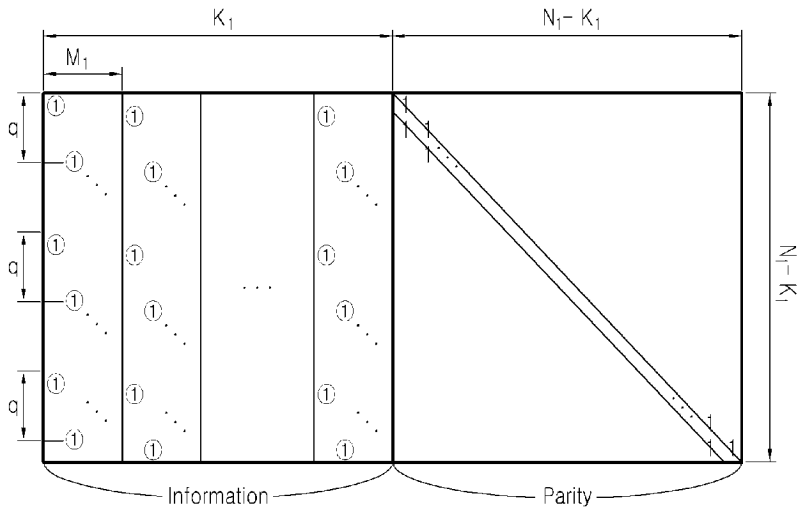
[Fig. 1]

$$H_1 = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 1 & 1 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 \\ 1 & 0 & 1 & 1 & 1 & 0 & 0 & 1 \end{bmatrix}$$

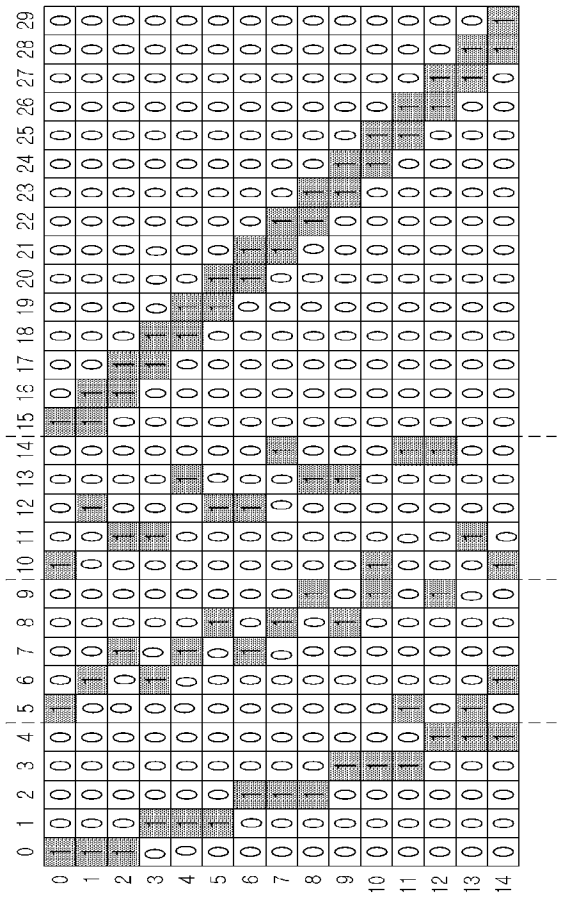
[Fig. 2]



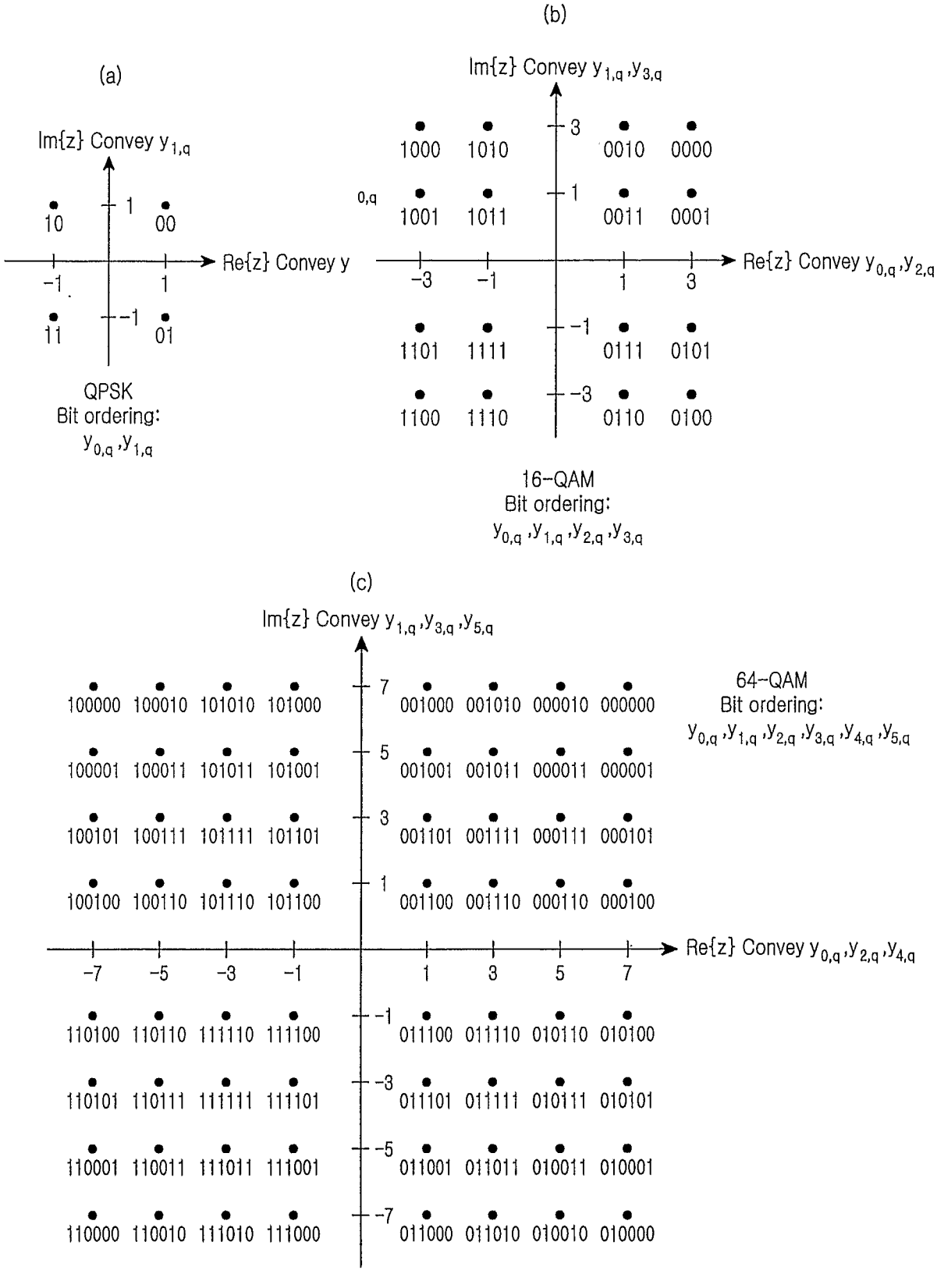
[Fig. 3]



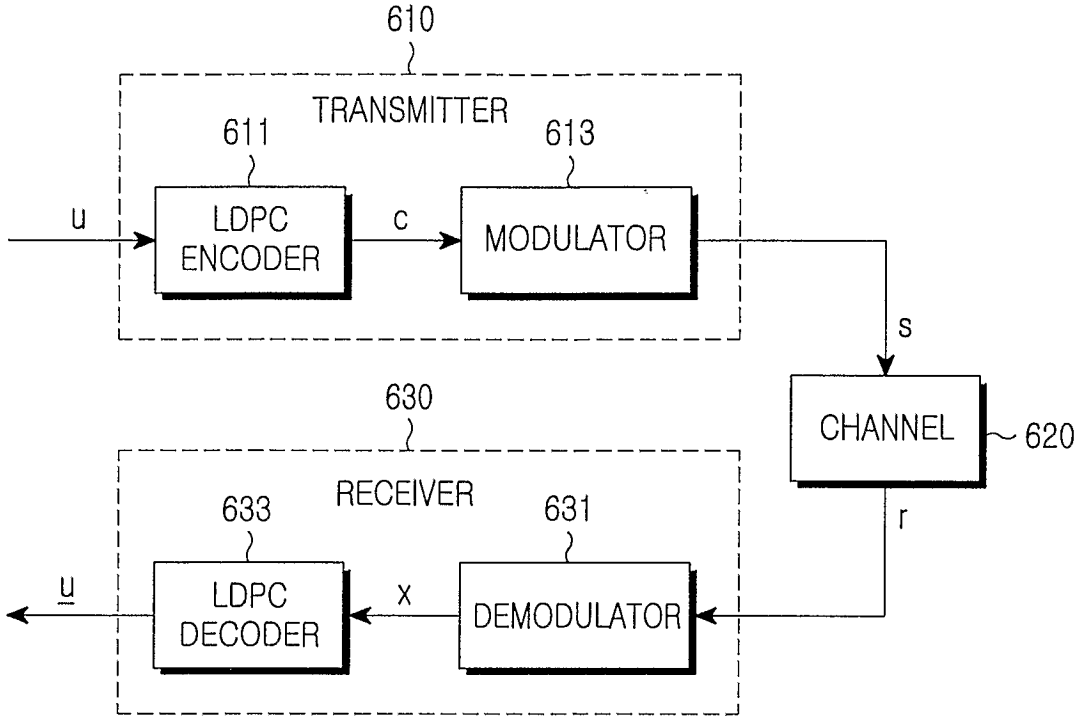
[Fig. 4]



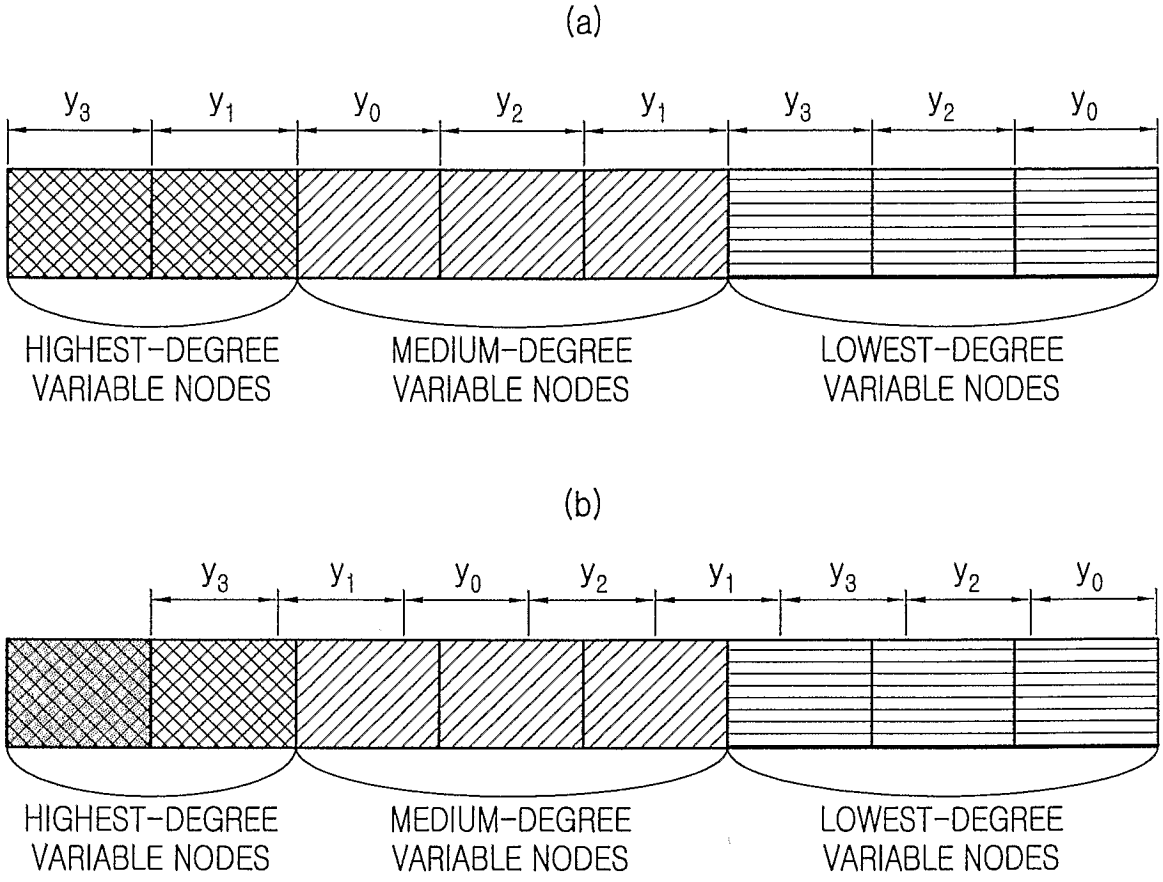
[Figure 5]


(a)
Im{z} Convey $y_{1,q}$
Re{z} Convey y
10
00
11
01
QPSK
Bit ordering:
$y_{0,q}$,$y_{1,q}$
(b)
Im{z} Convey $y_{1,q}$,$y_{3,q}$
Re{z} Convey $y_{0,q}$,$y_{2,q}$
1000 1010 0010 0000
1001 1011 0011 0001
1101 1111 0111 0101
1100 1110 0110 0100
16-QAM
Bit ordering:
$y_{0,q}$,$y_{1,q}$,$y_{2,q}$,$y_{3,q}$
(c)
Im{z} Convey $y_{1,q}$,$y_{3,q}$,$y_{5,q}$
Re{z} Convey $y_{0,q}$,$y_{2,q}$,$y_{4,q}$
100000 100010 101010 101000 001000 001010 000010 000000
100001 100011 101011 101001 001001 001011 000011 000001
100101 100111 101111 101101 001101 001111 000111 000101
100100 100110 101110 101100 001100 001110 000110 000100
110100 110110 111110 111100 011100 011110 010110 010100
110101 110111 111111 111101 011101 011111 010111 010101
110001 110011 111011 111001 011001 011011 010011 010001
110000 110010 111010 111000 011000 011010 010010 010000
64-QAM
Bit ordering:
$y_{0,q}$,$y_{1,q}$,$y_{2,q}$,$y_{3,q}$,$y_{4,q}$,$y_{5,q}$

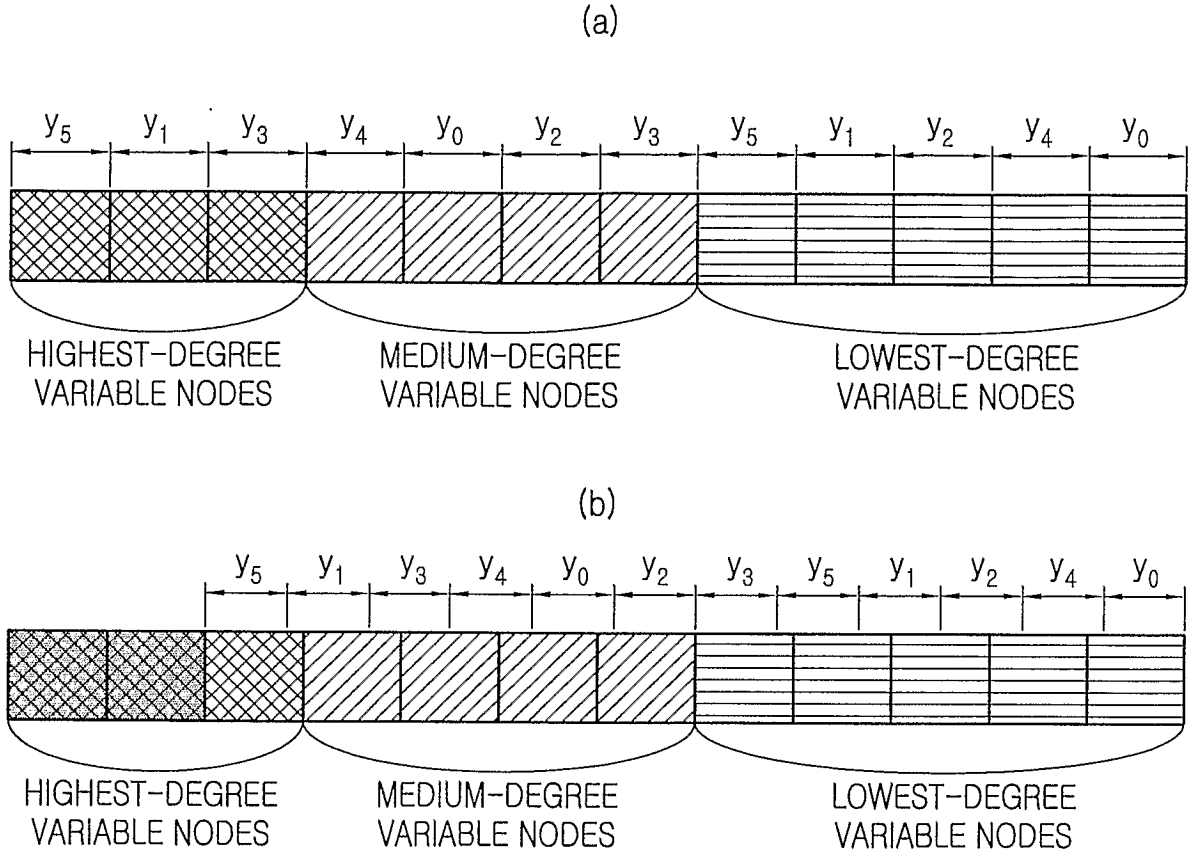
[Figure 6]


610
TRANSMITTER
611
613
u
LDPC ENCODER
c
MODULATOR
s
CHANNEL
620
630
RECEIVER
633
631
u
LDPC DECODER
x
DEMODULATOR
r

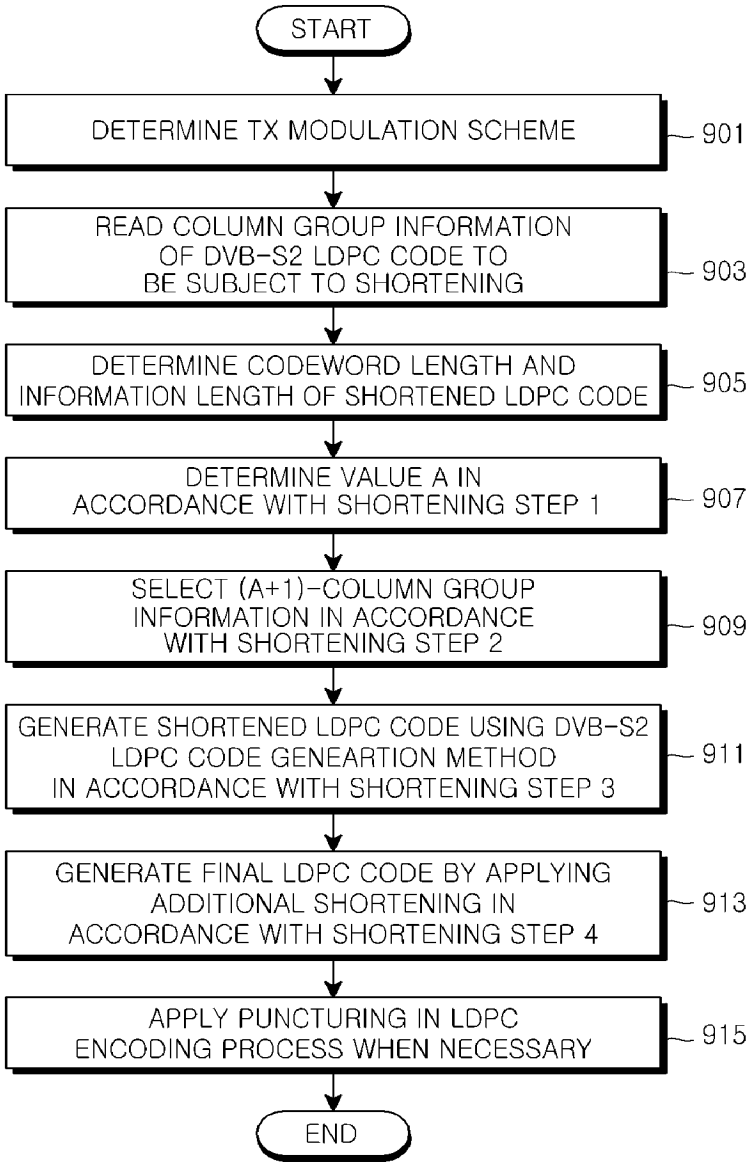
[Figure 7]


(a)
y_3 y_1 y_0 y_2 y_1 y_3 y_2 y_0
HIGHEST-DEGREE VARIABLE NODES
MEDIUM-DEGREE VARIABLE NODES
LOWEST-DEGREE VARIABLE NODES
(b)
y_3 y_1 y_0 y_2 y_1 y_3 y_2 y_0
HIGHEST-DEGREE VARIABLE NODES
MEDIUM-DEGREE VARIABLE NODES
LOWEST-DEGREE VARIABLE NODES

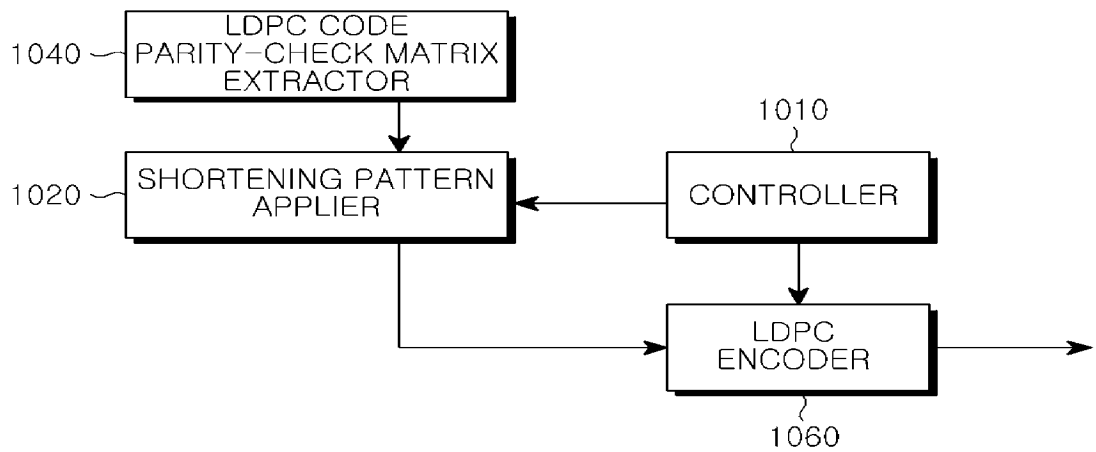
[Figure 8]


(a)
y5 y1 y3 y4 y0 y2 y3 y5 y1 y2 y4 y0
HIGHEST-DEGREE VARIABLE NODES
MEDIUM-DEGREE VARIABLE NODES
LOWEST-DEGREE VARIABLE NODES
(b)
y5 y1 y3 y4 y0 y2 y3 y5 y1 y2 y4 y0
HIGHEST-DEGREE VARIABLE NODES
MEDIUM-DEGREE VARIABLE NODES
LOWEST-DEGREE VARIABLE NODES

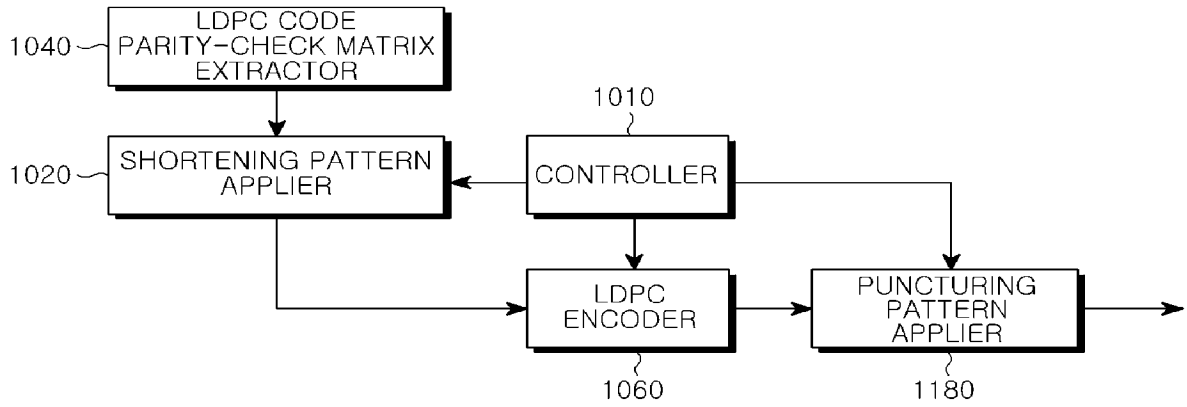
[Fig. 9]


START
DETERMINE TX MODULATION SCHEME
901
READ COLUMN GROUP INFORMATION OF DVB-S2 LDPC CODE TO BE SUBJECT TO SHORTENING
903
DETERMINE CODEWORD LENGTH AND INFORMATION LENGTH OF SHORTENED LDPC CODE
905
DETERMINE VALUE A IN ACCORDANCE WITH SHORTENING STEP 1
907
SELECT (A+1)-COLUMN GROUP INFORMATION IN ACCORDANCE WITH SHORTENING STEP 2
909
GENERATE SHORTENED LDPC CODE USING DVB-S2 LDPC CODE GENEARTION METHOD IN ACCORDANCE WITH SHORTENING STEP 3
911
GENERATE FINAL LDPC CODE BY APPLYING ADDITIONAL SHORTENING IN ACCORDANCE WITH SHORTENING STEP 4
913
APPLY PUNCTURING IN LDPC ENCODING PROCESS WHEN NECESSARY
915
END

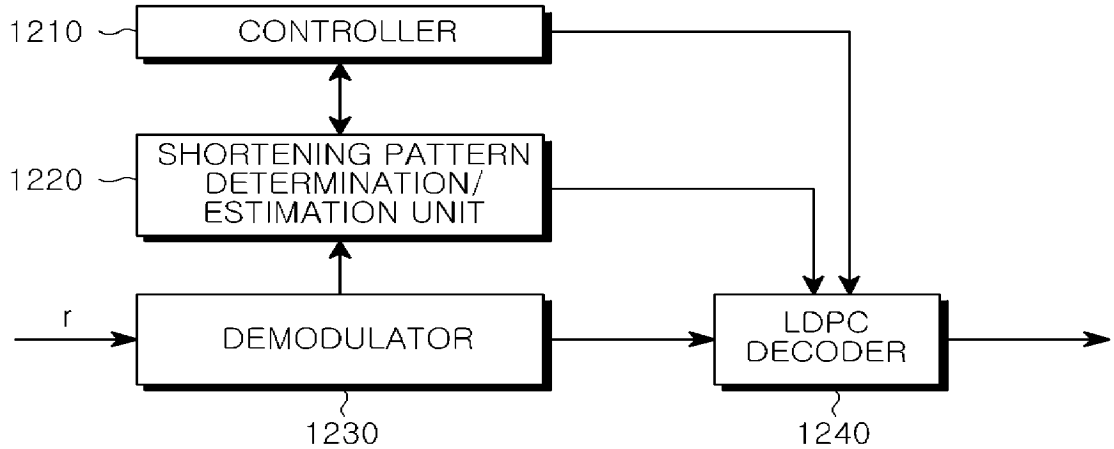
[Fig. 10]


1040
LDPC CODE PARITY-CHECK MATRIX EXTRACTOR
1010
1020
SHORTENING PATTERN APPLIER
CONTROLLER
LDPC ENCODER
1060

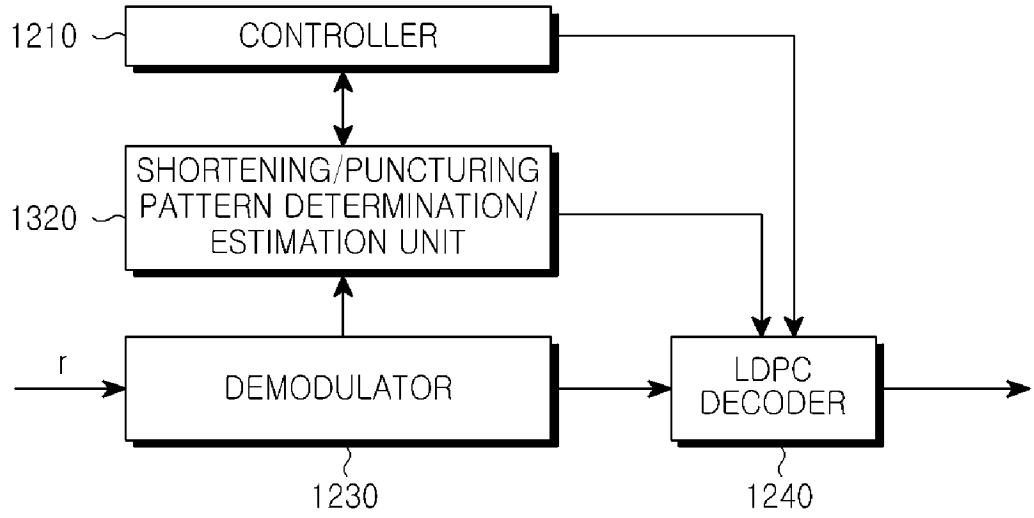
[Fig. 11]



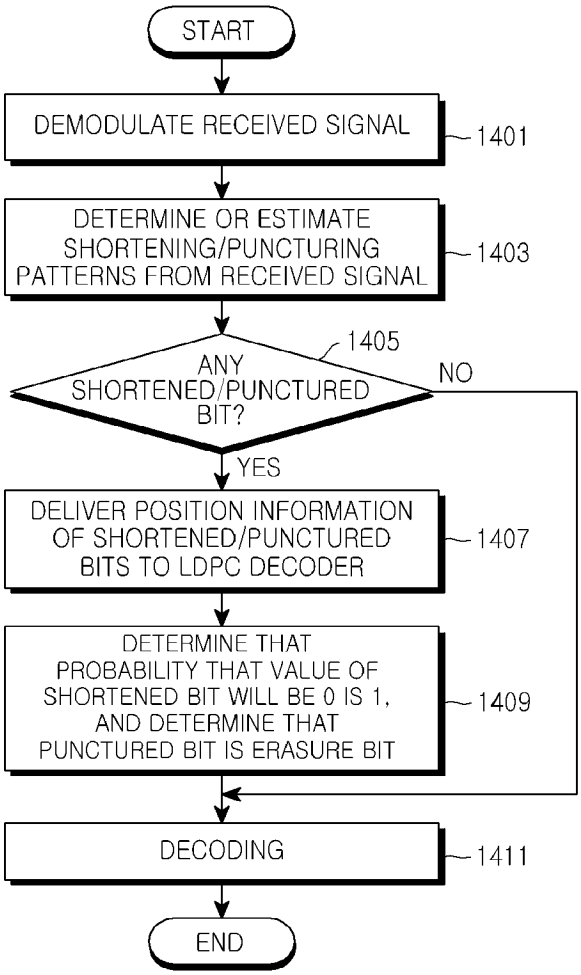
[Fig. 12]



[Fig. 13]



[Fig. 14]


START
DEMODULATE RECEIVED SIGNAL
1401
DETERMINE OR ESTIMATE SHORTENING/PUNCTURING PATTERNS FROM RECEIVED SIGNAL
1403
1405
ANY SHORTENED/PUNCTURED BIT?
NO
YES
DELIVER POSITION INFORMATION OF SHORTENED/PUNCTURED BITS TO LDPC DECODER
1407
DETERMINE THAT PROBABILITY THAT VALUE OF SHORTENED BIT WILL BE 0 IS 1, AND DETERMINE THAT PUNCTURED BIT IS ERASURE BIT
1409
DECODING
1411
END